

# RF-3466A UNIVERSAL HF MODEM

## INSTALLATION AND OPERATION MANUAL

Copyright © 1988  
By Harris Corporation  
All Rights Reserved



Equipment manufactured by Harris Corporation, RF Communications Group meets stringent quality and safety standards. However, high voltages are present in many radio products, and only a skilled technician should attempt to remove outer covers and make adjustments or repairs. All personnel who operate and maintain the equipment should be familiar with this page as a safety preparedness measure. Although this procedure is reproduced as a service to the personnel involved with this equipment, Harris Corporation assumes no liability regarding any injuries incurred during the operation and repair of such equipment, or the administration of this suggested procedure.

**ELECTRICAL SHOCK: EMERGENCY PROCEDURE**

The victim will appear unconscious and may not be breathing. If the victim is still in contact with the voltage source, disconnect the power source in a manner safe to you, or remove the victim from the source with an insulated aid (wooden pole or rope). Next, determine if the victim is breathing and has a pulse. If there is a pulse but no breathing, administer artificial respiration. If there is no pulse and no breathing, perform CPR (if you have been trained to do so). If you have not been trained to perform CPR, administer artificial respiration anyway. Never give fluids to an unconscious person.

**WHEN BREATHING STOPS**



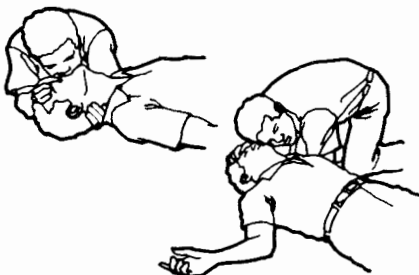
**FIRST**, send someone to get a **DOCTOR**.  
**THEN**, administer first aid to restore breathing (artificial respiration):

**1 IF A VICTIM APPEARS TO BE UNCONSCIOUS**  
TAP VICTIM ON THE SHOULDER AND SHOUT, "ARE YOU OKAY?"



**2 IF THERE IS NO RESPONSE**  
TILT THE VICTIM'S HEAD, CHIN POINTING UP. Place one hand under the victim's neck and gently lift. At the same time, push with the other hand on the victim's forehead. This will move the tongue away from the back of the throat to open the airway.

**IMMEDIATELY LOOK, LISTEN, AND FEEL FOR AIR.**  
While maintaining the backward head tilt position, place your cheek and ear close to the victim's mouth and nose. Look for the chest to rise and fall while you listen and feel for the return of air. Check for about five seconds.



**3 IF THE VICTIM IS NOT BREATHING**  
GIVE FOUR QUICK BREATHS.

Maintain the backward head tilt, pinch the victim's nose with the hand that is on the victim's forehead to prevent leakage of air, open your mouth wide, take a deep breath, seal your mouth around the victim's mouth, and blow into the victim's mouth with four quick but full breaths just as fast as you can. When blowing, use only enough time between breaths to lift your head slightly for better inhalation.

If you do not get an air exchange when you blow, it may help to reposition the head and try again.

AGAIN, LOOK, LISTEN, AND FEEL FOR AIR EXCHANGE.



**4 IF THERE IS STILL NO BREATHING**  
CHANGE RATE TO ONE BREATH EVERY FIVE SECONDS.

For more information about these and other life-saving techniques, contact your Red Cross chapter for training. "When Breathing Stops" reproduced with permission from an American Red Cross Poster.

**TABLE OF CONTENTS**

<b>Paragraph</b>		<b>Page</b>
	Specifications . . . . .	xi
	About This Manual . . . . .	xv
 <b>SECTION 1 - INTRODUCTION</b>		
1.1	Purpose of Manual . . . . .	1-1
1.2	Scope . . . . .	1-1
1.3	General Description . . . . .	1-1
1.4	Radio Equipment Interface Criteria . . . . .	1-3
1.5	Data Terminal Equipment Interface Criteria . . . . .	1-3
1.5.1	39 Tone General Considerations . . . . .	1-4
1.5.2	39 Tone Synchronous Operation . . . . .	1-4
1.5.3	39 Tone Asynchronous Operation . . . . .	1-5
1.5.4	FSK General Considerations . . . . .	1-5
1.5.5	FSK Synchronous Operation . . . . .	1-5
1.5.6	FSK Asynchronous Operation . . . . .	1-5
1.6	Remote Control . . . . .	1-5
1.7	Glossary of Terms and Abbreviations . . . . .	1-6
1.8	Optional Equipment . . . . .	1-6
 <b>SECTION 2 - INSTALLATION</b>		
2.1	General Information . . . . .	2-1
2.1.1	Tools and Equipment . . . . .	2-1
2.1.2	Size . . . . .	2-1
2.1.3	Power . . . . .	2-1
2.2	Unpacking . . . . .	2-1
2.3	Ancillary Kit . . . . .	2-3
2.4	Mounting Options . . . . .	2-3
2.5	Power Connections . . . . .	2-3
2.6	Rear Panel Connections . . . . .	2-5
2.7	System Interconnections . . . . .	2-9
2.8	Initial Setup and Checkout . . . . .	2-9
2.8.1	RS-232 or MIL-STD-188C Select . . . . .	2-9
2.8.2	Audio Output Level Adjustment Procedure . . . . .	2-9
2.8.3	Frequency Standard . . . . .	2-17
2.8.4	Switch and Jumper Configuration . . . . .	2-17
 <b>SECTION 3 - OPERATION</b>		
3.1	Introduction . . . . .	3-1
3.2	Controls and Indicators . . . . .	3-1
3.2.1	Send . . . . .	3-2
3.2.2	Signal Presence A and B . . . . .	3-4
3.2.3	Data Sync . . . . .	3-4
3.3	Manual Operation . . . . .	3-4
3.3.1	Selecting an Operating Mode . . . . .	3-4

TABLE OF CONTENTS (Cont.)

Paragraph		Page
<b>SECTION 3 - OPERATION (Cont.)</b>		
3.3.2	Selecting Operating Parameters . . . . .	3-5
3.3.3	Changing Operating Parameters . . . . .	3-5
3.3.4	Saving Selections as a Preset . . . . .	3-5
3.4	Preset Operation . . . . .	3-5
3.4.1	Entering the Preset Mode . . . . .	3-6
3.4.2	Selecting a Preset . . . . .	3-6
3.4.3	Reviewing the Operating Parameters of a Preset . . . . .	3-6
3.4.4	Temporary Alteration of a Preset's Parameters . . . . .	3-6
3.4.5	Deleting a Preset . . . . .	3-7
3.4.6	Exiting Preset Mode . . . . .	3-7
3.5	Metering . . . . .	3-7
3.6	Self-Test . . . . .	3-7
3.6.1	Self-Test on Power Up . . . . .	3-8
3.6.2	Using the TEST Button for Self-Test . . . . .	3-8
3.6.3	Testing the Front Panel Controls . . . . .	3-8
3.7	Remote Control Operation . . . . .	3-8
3.8	Functional Descriptions . . . . .	3-8
3.8.1	Main Set Up Mode . . . . .	3-9
3.8.2	39-Tone Mode . . . . .	3-10
3.8.3	Robust Serial Mode (Option) . . . . .	3-11
3.8.4	FSK Mode . . . . .	3-13
3.8.5	39 Tone/FSK Mode . . . . .	3-13
3.8.6	Robust Serial/FSK Mode . . . . .	3-18
3.9	Parameter Descriptions . . . . .	3-21
3.9.1	Remote Identification . . . . .	3-21
3.9.2	Remote Rate . . . . .	3-21
3.9.3	Power Up Bit . . . . .	3-21
3.9.4	Halt On Fault . . . . .	3-21
3.9.5	Loopback . . . . .	3-21
3.9.6	Clock . . . . .	3-21
3.9.7	39 Tone Mode Interleaving Factor . . . . .	3-22
3.9.8	Synchronous or Asynchronous DTE . . . . .	3-23
3.9.9	Channel Diversity . . . . .	3-23
3.9.10	Duplex . . . . .	3-23
3.9.11	Key Delay . . . . .	3-23
3.9.12	Clipping . . . . .	3-24
3.9.13	Time/Frequency Diversity . . . . .	3-24
3.9.14	Doppler Track . . . . .	3-24
3.9.15	Acquisition . . . . .	3-24
3.9.16	DTE Baud Rate . . . . .	3-24
3.9.17	DTE Echo/No Echo . . . . .	3-24
3.9.18	Asynchronous EOM . . . . .	3-25
3.9.19	Flow . . . . .	3-25
3.9.20	Interleaving Factor (Robust Serial Option) . . . . .	3-25
3.9.21	FSK Rx Rate . . . . .	3-25
3.9.22	Tx Mark, Tx Center . . . . .	3-25
3.9.23	Tx Space, Tx Shift . . . . .	3-26

TABLE OF CONTENTS (Cont.)

Paragraph		Page
<b>SECTION 3 - OPERATION (Cont.)</b>		
3.9.24	Rx Mark, Rx Center . . . . .	3-26
3.9.25	Rx Space, Rx Shift . . . . .	3-26
3.9.26	FSK Channel . . . . .	3-26
3.9.27	FSK Tx Rate . . . . .	3-26
3.9.28	Threshold Tracking . . . . .	3-27
3.9.29	Modulator Output . . . . .	3-27
3.9.30	Polarity . . . . .	3-27
3.9.31	Mark Hold . . . . .	3-27
3.9.32	Tune . . . . .	3-27
3.9.33	Track Tune . . . . .	3-27
3.9.34	Mod AB Sum . . . . .	3-28
3.9.35	DTE Rx Clock . . . . .	3-28
3.9.36	B Analog In . . . . .	3-28
3.9.37	39-Tone Modem Rate . . . . .	3-28
<b>SECTION 4 - THEORY OF OPERATION</b>		
4.1	Introduction . . . . .	4-1
4.2	39-Tone Theory of Operation . . . . .	4-1
4.2.1	Modulation . . . . .	4-1
4.2.2	Demodulation . . . . .	4-2
4.2.3	Frequency and Frame Synchronization . . . . .	4-2
4.2.3.1	Enhanced Acquisition . . . . .	4-11
4.2.4	Forward Error Correction (FEC) Code . . . . .	4-13
4.2.5	Interleaving . . . . .	4-14
4.2.6	Diversity . . . . .	4-16
4.2.7	Signal Clipping . . . . .	4-16
4.2.8	Keyline Control . . . . .	4-17
4.3	Binary FSK Theory of Operation . . . . .	4-17
4.4	Major Assemblies . . . . .	4-17
4.4.1	Analog I/O PWB Assembly A1 . . . . .	4-17
4.4.1.1	Digital-to-Analog Conversion . . . . .	4-17
4.4.1.2	Analog-to-Digital Conversion . . . . .	4-17
4.4.2	Signal Processor PWB Assembly A2 . . . . .	4-20
4.4.3	MOD/DEMODO PWB Assembly A4 . . . . .	4-21
4.4.4	FSK PWB Assembly A5 . . . . .	4-21
4.4.4.1	FSK PWB Transmit Data Signal Flow . . . . .	4-21
4.4.4.2	FSK PWB Receive Data Signal Flow . . . . .	4-27
4.4.5	FEC I/O PWB Assembly A6 . . . . .	4-27
4.4.6	Decoder Assembly A7 . . . . .	4-32
4.4.7	Digital I/O PWB Assembly A8 . . . . .	4-32
4.4.8	Ac Power Supply Assembly A9 . . . . .	4-32
4.4.9	Interconnect PWB Assembly A10 . . . . .	4-37
4.4.10	Front Panel Assembly A11 . . . . .	4-37
4.4.10.1	Logic/Clock Assembly A11A1 . . . . .	4-37
4.4.10.2	Switch Assembly A11A2 . . . . .	4-38
4.4.11	Rear Panel Assembly A12 . . . . .	4-38
4.4.11.1	Rear Panel Filter Assembly . . . . .	4-38
4.4.11.2	Fan Speed Control . . . . .	4-38

**TABLE OF CONTENTS (Cont.)**

Paragraph		Page
<b>SECTION 5 - MAINTENANCE</b>		
5.1	Introduction . . . . .	5-1
5.1.1	Protection of Static Sensitive Devices . . . . .	5-1
5.2	Required Periodic Maintenance . . . . .	5-2
5.2.1	Air Filter Removal and Cleaning . . . . .	5-2
5.2.1.1	Procedure . . . . .	5-2
5.2.2	Alignment Procedure 9600 Hz-PLL . . . . .	5-2
5.3	BIT/BITE Description and Use . . . . .	5-2
5.4	Troubleshooting Guidelines . . . . .	5-3
5.4.1	General . . . . .	5-3
5.4.2	Power Supply/Rear Panel/Fan . . . . .	5-3
5.4.3	Front Panel . . . . .	5-7
5.5	Replacement Procedures . . . . .	5-7
5.5.1	General . . . . .	5-7
5.5.2	Front Panel PWB (A11) Removal and Replacement Procedure . . . . .	5-8
5.5.2.1	Front Panel Assembly Removal . . . . .	5-8
5.5.2.2	A11A1 PWB Removal and Replacement Procedure . . . . .	5-8
5.5.2.3	A11A2 PWB Removal and Replacement Procedure . . . . .	5-8
5.5.2.4	A11A3 PWB Removal and Replacement Procedure . . . . .	5-8
5.5.2.5	Front Panel Assembly Installation . . . . .	5-10
5.5.3	Rear Panel Filter Assembly Removal and Replacement . . . . .	5-10
5.5.4	Cooling Fan Removal and Replacement . . . . .	5-11
5.5.5	Fan Speed Control PWB Assembly Removal and Replacement . . . . .	5-11
5.5.6	Power Supply Removal and Replacement . . . . .	5-12

**SECTION 6 - PARTS LISTS, COMPONENT LOCATION DIAGRAMS, AND SCHEMATIC DIAGRAMS**

6.1	Introduction . . . . .	6-1
-----	------------------------	-----

**ROBUST SERIAL TONE OPTION**

**GLOSSARY**

**LIST OF FIGURES**

Figure		Page
Frontispiece	RF-3466A Universal HF Modem	
1-1	RF-3466A Universal HF Modem Applications . . . . .	1-2
2-1	RF-3466A Dimensions . . . . .	2-2
2-2	Slide Mount Bracket Kit . . . . .	2-4
2-3	Ac Power Supply Voltage Selection Switch . . . . .	2-5
2-4	Rear Panel Connectors . . . . .	2-6
2-5	Asynchronous and Synchronous Data Terminal Equipment Diagram . . . . .	2-10
2-6	Transceiver Operation and Frequency Diversity Diagram . . . . .	2-11
2-7	Dual Independent FSK or Simultaneous FSK and 39-Tone Mode . . . . .	2-12

LIST OF FIGURES (Cont.)

Figure		Page
2-8	Test Point and Potentiometer Locations . . . . .	2-16
3-1	RF-3466A Front Panel Controls . . . . .	3-1
3-2	RF-3466A Front Panel Indicators . . . . .	3-3
4-1	RF-3466A Simplified Block Diagram . . . . .	4-3
4-2	39-Tone Modulation and Demodulation Functions . . . . .	4-5
4-3	TDQPSK Fundamentals . . . . .	4-7
4-4	Vector Representation of Phase Shift . . . . .	4-10
4-5	Frequency Correction . . . . .	4-11
4-6	Frame Boundaries . . . . .	4-12
4-7	Interleaving Matrix . . . . .	4-15
4-8	Analog I/O PWB Assembly Block Diagram . . . . .	4-19
4-9	Signal Processor PWB Assembly Block Diagram A2 . . . . .	4-20
4-10	MOD/DEMOD PWB Assembly Block Diagram . . . . .	4-22
4-11	FSK PWB (P/N 10133-2500) Block Diagram . . . . .	4-23
4-12	FSK PWB Transmit Signal Flow . . . . .	4-25
4-13	FSK PWB Receive Signal Flow . . . . .	4-29
4-14	FEC I/O PWB Assembly Block Diagram . . . . .	4-31
4-15	Decoder Block Diagram . . . . .	4-33
4-16	Digital I/O PWB Assembly Block Diagram . . . . .	4-34
4-17	Power Supply Assembly Block Diagram . . . . .	4-35
4-18	Front Panel Assembly Block Diagram . . . . .	4-39
4-19	Rear Panel Filter Assembly A12A1 Block Diagram . . . . .	4-41
4-20	Fan Speed Control Block Diagram . . . . .	4-43
5-1	BIT Memory Check . . . . .	5-4
5-2	BIT Signal Processing Tests . . . . .	5-5
5-3	RF-3466A Assembly Locations . . . . .	5-6
5-4	Front Panel PWB Cable Connections . . . . .	5-9
5-5	Filter Assembly Location and Removal . . . . .	5-10
5-6	Fan Speed Control PWB Removal and Replacement . . . . .	5-13
5-7	Power Supply Removal and Replacement . . . . .	5-14
6-1	Main Chassis Interconnection Schematic Diagram (10133-3501) . . . . .	6-3
6-2	Analog I/O PWB Assembly A1 Component Locations (10133-2150) . . . . .	6-11
6-3	Analog I/O PWB Assembly A1 Schematic Diagram (10133-2151) . . . . .	6-13
6-4	Signal Processor PWB Assembly A2 Component Locations (10133-2200) . . . . .	6-20
6-5	Signal Processor PWB Assembly A2 Schematic Diagram (10133-2201) . . . . .	6-21
6-6	MOD/DEMOD A4 and FEC I/O A6 PWB Assembly Component Locations (10133-2400-01/02) . . . . .	6-32
6-7	MOD/DEMOD PWB Assembly A4 Schematic Diagram (10133-2401-01) . . . . .	6-33
6-8	A5 FSK PWB Assembly Component Location Diagram (10133-2500) . . . . .	6-45
6-9	A5 FSK PWB Assembly Schematic Diagram (10133-2501) . . . . .	6-47
6-10	MOD/DEMOD A4 and FEC I/O PWB Assembly Component Locations (10133-2400-01/-02) . . . . .	6-66
6-11	FEC I/O PWB Assembly A6 Schematic Diagram (10133-2401-02) . . . . .	6-67
6-12	Decoder PWB Assembly A7 (10133-2450) . . . . .	6-76
6-13	Decoder PWB Assembly A7 Schematic Diagram (10133-2451) . . . . .	6-77
6-14	Digital I/O PWB Assembly A8 Component Locations (10133-2800) . . . . .	6-88
6-15	Digital I/O PWB Assembly A8 Schematic Diagram (10133-2801) . . . . .	6-89
6-16	Power Supply Assembly Component Locations (10133-1200) . . . . .	6-100

LIST OF FIGURES (Cont.)

Figure		Page
6-17	Power Supply PWB Assembly A9A1 Component Locations (10133-1220)	6-104
6-18	Power Supply PWB Assembly A9A1 Schematic Diagram (10133-1221)	6-105
6-19	EMI Filter PWB Assembly A9A2A1 Component Locations (10133-1300-01/-02)	6-109
6-20	EMI Filter PWB Assembly A9A2A1 Schematic Diagram (10133-1301)	6-111
6-21	Interconnect PWB Assembly A10 Component Locations (10133-2900)	6-114
6-22	Interconnect PWB Assembly A10 Schematic Diagram (10133-2901)	6-115
6-23	Logic/Clock PWB Assembly A11A1 Component Locations (10133-1850)	6-123
6-24	Logic/Clock PWB Assembly A11A1 Schematic Diagram (10133-1851)	6-125
6-25	Front Panel Switch PWB Assembly A11A2 (10133-1840)	6-133
6-26	Front Panel Switch PWB Assembly A11A2 Schematic Diagram (10133-1841)	6-135
6-27	Rear Panel Filter PWB Assembly No. 1 A12A1A1 Component Locations (10133-1080)	6-140
6-28	Rear Panel Filter PWB Assembly No. 1 A12A1A1 Schematic Diagram (10133-1081)	6-141
6-29	Rear Panel Filter PWB Assembly No. 2 A12A1A2 Component Locations (10133-1070)	6-147
6-30	Rear Panel Filter PWB Assembly No. 2 A12A1A2 Schematic Diagram (10133-1071)	6-149
6-31	Rear Panel Filter PWB Assembly No. 3 A12A1A3 Component Locations (10133-1160)	6-152
6-32	Rear Panel Filter PWB Assembly No. 3 A12A1A3 Schematic Diagram (10133-1161)	6-153
6-33	Fan Speed Control PWB Assembly A12A2 Component Locations (10133-1090)	6-156
6-34	Fan Speed Control PWB Assembly A12A2 Schematic Diagram (10133-1091)	6-157

LIST OF TABLES

Table		Page
1-1	Radio Equipment Requirements	1-4
1-2	Remotely Controllable Operating Parameters	1-6
1-3	Optional Equipment	1-7
2-1	Ancillary Kit (10133-3021)	2-3
2-2	Rear Panel Connectors	2-5
2-3	Data Terminal Connector J1 Pin Identification	2-6
2-4	Connector J3 Pin Identification	2-7
2-5	Connector J4 Pin Identification	2-8
2-6	Remote Connector J5 Pin Identification	2-8
2-7	Power Connector J6 Pin Identification	2-8
2-8	Selected Operating Parameters for Main Set Up Mode	2-13
2-9	Selected Operating Parameters for 39-Tone Mode	2-13

**LIST OF TABLES (Cont.)**

Table		Page
2-10	Selected Operating Parameters for 39-Tone Mode (if DTE is Asynchronous)	2-14
2-11	Selected Operating Parameters for Robust Serial Option	2-14
2-12	Selected Operating Parameters for Robust Serial Mode Option (if DTE is Asynchronous)	2-14
2-13	Selected Operating Parameters for FSK Mode	2-15
2-14	Switch and Jumper Configurations	2-17
3-1	RF-3466A Front Panel Controls	3-2
3-2	RF-3466A Front Panel Indicators	3-3
3-3	Main Set Up Mode (Available Only in Program Mode)	3-9
3-4	39-Tone Mode (Manual Mode Selections)	3-10
3-5	39-Tone Mode (Program Mode Selections)	3-10
3-6	39-Tone Mode (Program Selections if DTE is Asynchronous)	3-11
3-7	Robust Serial Mode (Manual Mode Selections)	3-11
3-8	Robust Serial Mode (Program Mode Selections)	3-12
3-9	Robust Serial Mode (Program Selections if DTE is Asynchronous)	3-12
3-10	FSK Mode (Manual Mode Selections)	3-14
3-11	FSK Mode (Program Mode Selections)	3-14
3-12	39-Tone/FSK Mode (Manual Mode Selections)	3-16
3-13	39-Tone/FSK Mode (Program Mode Selections)	3-16
3-14	39-Tone/FSK Mode (Program Selections if DTE is Asynchronous)	3-17
3-15	Robust Serial/FSK Mode (Manual Mode Selections)	3-18
3-16	Robust Serial/FSK Mode (Program Mode Selections)	3-19
3-17	Robust Serial/FSK Mode (Program Selections if DTE is Asynchronous)	3-20
3-18	Modem Startup and Throughput Delays (Short or Long Mode) in Seconds (Delays Assume a Keyline Delay Setting of 45 ms)	3-22
3-19	Modem Startup and Throughput Delays (ALTERNATE Short or Long Mode) in Seconds (Delays Assume a Keyline Delay Setting of 45 ms)	3-23
4-1	39-Tone Library	4-8
4-2	Normal/Enhanced Acquisition Preambles	4-13
4-3	Diversity Factors	4-16
4-4	Major Assemblies	4-18
6-1	Main Chassis Assembly (10133-3500) Parts List	6-1
6-2	Analog I/O PWB Assembly A1 (10133-2150) Parts List	6-7
6-3	Signal Processor PWB Assembly A2 (10133-2200) Parts List	6-17
6-4	MOD/DEMODO PWB Assembly A4 (10133-2400-011) Parts List	6-29
6-5	A5 FSK PWB Assembly Parts List (10133-2500-01)	6-39
6-6	FEC I/O PWB Assembly A6 (10133-2400-021) Parts List	6-63
6-7	Decoder PWB Assembly A7 (10133-2450-04) Parts List	6-73
6-8	Digital I/O PWB Assembly A8 (10133-2800-01) Parts List	6-85
6-9	Power Supply Assembly A9 (10133-1200) Parts List	6-99
6-10	Power Supply PWB Assembly A9A1 (10133-1220) Parts List	6-101
6-11	EMI Filter PWB Assembly A9A2 A1 (10133-1300-01/-02) Parts List	6-107
6-12	Interconnect PWB Assembly A10 (10133-2900-01) Parts List	6-113
6-13	Front Panel Assembly A11 (10133-1800) Parts List	6-119
6-14	Front Panel Logic/Clock PWB Assembly A11A1 (10133-1850) Parts List	6-119
6-15	Front Panel Switch Assembly (10133-1840) Parts List	6-122
6-16	Rear Panel Assembly A12 (10133-1009) Parts List	6-137
6-17	Rear Panel Assembly A12A1 (10133-1150) Parts List	6-137

LIST OF TABLES (Cont.)

Table		Page
6-18	Rear Panel Filter PWB Assembly No. 1 A12A1A1 (10133-1080) Parts List	6-138
6-19	Rear Panel Filter PWB Assembly No. 2 A12A1A2 (10133-1070) Parts List	6-145
6-20	Rear Panel Filter PWB Assembly No. 3 A12A1A3 (10133-1060) Parts List	6-151
6-21	Fan Speed Control PWB Assembly A12A2 (10133-1090) Parts List	6-155

**SPECIFICATIONS FOR RF-3466A UNIVERSAL HF MODEM**

**ELECTRICAL**

**39 Tone Mode**

<b>Data Rates (bps):</b>	2400, 1200, 600, 150, 75
<b>Duplex:</b>	Full-duplex, half-duplex
<b>FEC Coding:</b>	(14, 10, 2) Reed-Solomon Code at 2400 bps; (7, 3, 2) Reed-Solomon Code at lower rates; Soft Decision Decoding
<b>Interleaving Delays:</b>	Four choices are available at each baud rate, determined by the interleaving selected
<b>Tone Library:</b>	39 tones, 675-2812.5 Hz, 56.25 Hz spacing, plus one doppler tone 393.75 Hz
<b>Diversity:</b>	In-band at 600 bps and lower data rates; out-of-band dual channel at all rates
<b>Modulation:</b>	TDPSK; IFFT tone generation
<b>Demodulation:</b>	128 point FFT
<b>Guard Time:</b>	4.72 ms
<b>Integration Time:</b>	17.77 ms
<b>Symbol Rate:</b>	44.44 frames/second
<b>Sampling Frequency:</b>	7200 Hz
<b>Preamble:</b>	<p>Normal Synchronization: Phase 1 (doppler), 4 tones (787, 1462, 2137, 2812 Hz) sent for 315 ms; followed by phase 2 (sync), 3 bi-phase modulated tones (1125, 1800, 2475 Hz) sent for 180 ms; followed by phase 3 (reference), 39 tones sent for 22.5 ms.</p> <p>Enhanced Synchronization: Phase 1 (doppler), 4 tones (787, 1462, 2137, 2812 Hz) sent for 1.305 seconds; followed by phase 2 (sync), 3 bi-phase modulated tones (1125, 1800, 2475 Hz) sent for 0.608 seconds; followed by phase 3 (reference), 39 tones sent for 0.27 seconds.</p>

**SPECIFICATIONS FOR RF-3466A UNIVERSAL HF MODEM (Cont.)**

**ELECTRICAL (Cont.)**

**39 Tone Mode**

<b>Doppler Correction:</b>	Normal Acquisition Mode: $\pm 75$ Hz Enhanced Acquisition Mode: $\pm 20$ Hz Tracking up to 3.5 Hz per second, manual disable.
<b>Synchronization:</b>	To within $\pm 1.2$ ms in acquisition; tracking up to 1.2 ms per second.
<b>Channel Bandwidth:</b>	3000 Hz nominal
<b>Dynamic Range:</b>	30 dB

**Binary FSK Mode**

<b>Data Rates:</b>	45 to 1200 bps, in 1 baud increments; (1200 not recommended for HF)
<b>Signaling:</b>	Phase continuous binary FSK
<b>Tone Selection:</b>	0 to 3400 Hz, 1/2 Hz resolution
<b>Duplex:</b>	Full-duplex
<b>Channels:</b>	Two independent modulators and demodulators
<b>Diversity:</b>	Selectable for dual-diversity, with equal-gain combining
<b>Dual-Mode:</b>	One FSK channel may operate simultaneously with the 39 tone waveform (non-diversity) or the optional Robust Serial Tone Waveform
<b>Clock Regeneration:</b>	Recovered receive data clock for synchronous operation (available for one of the two independent FSK channels).
<b>Data Sense:</b>	Normal or Inverted
<b>Mark Hold:</b>	On, Off, Auto
<b>MD-522 Interoperability:</b>	MD-522 non-voice modes supported: 2805 Hz $\pm 42.5$ Hz or 2000 Hz $\pm 42.5$ Hz; Frequency diversity: 2805 Hz $\pm 42.5$ Hz plus 425 Hz $\pm 42.5$ Hz

**SPECIFICATIONS FOR RF-3466A UNIVERSAL HF MODEM (Cont.)**

**ELECTRICAL (Cont.)**

**Robust Serial Tone Mode (Option)**

<b>Data Rate:</b>	75 bps
<b>FEC Coding:</b>	Half-rate convolutional code; Viterbi soft-decision decoding
<b>Interleaving:</b>	Convolutional interleaver; 4 selections of end-to-end delay
<b>Modulation:</b>	8-ary PSK modulation of a single tone (spread-spectrum signaling)
<b>Demodulation:</b>	Correlation process
<b>Diversity:</b>	Combines multipath signal components to achieve a net diversity gain
<b>Multipath:</b>	Tolerates 11 ms of multipath spread
<b>Fading:</b>	Insensitive to rapid fades
<b>Interference:</b>	Techniques to reduce sensitivity to certain classes of interference
<b>Channel Bandwidth:</b>	3000 Hz nominal
<b>INTERFACE</b>	
<b>Data:</b>	RS-232C, MIL-188C, or MIL-188-100; synchronous or asynchronous
<b>Input Audio:</b>	+ 5 to -25 dBm; 600 ohms balanced (-10 dBm typical)
<b>Dynamic Range:</b>	30 dB
<b>Output Audio:</b>	+ 6 to -16 dBm; 600 ohms balanced
<b>Radio Keyline:</b>	Open collector, 100 V, 50 mA
<b>Remote Control:</b>	RS-422; Harris-defined, proprietary protocol
<b>External Standard:</b>	Frequency - 1.0 MHz; Impedance - 50 ohms; Level - 0.7 to 2 V <sub>rms</sub>

**SPECIFICATIONS FOR RF-3466A UNIVERSAL HF MODEM (Cont.)**

**Robust Serial Tone Mode (Option)**

**ENVIRONMENTAL**

**Temperature:** 0 to 50°C operating; -20 to 85°C storage

**Humidity:** 0 to 95%, noncondensing

**RFI:** Compatible with HF receiving and transmitting environment

**MECHANICAL**

**Size:** 7.0 H x 19 W x 18.0 D in.  
(17.8 H x 48.3 W x 47.7 D cm)

**Weight:** 28 lbs. (12.7 kg)

**POWER**

**Source:** 90-150/150-300 Vac selectable, single phase, 47-440 Hz (20-32 Vdc or 10-16 Vdc optional)

**Dissipation:** 80 watts

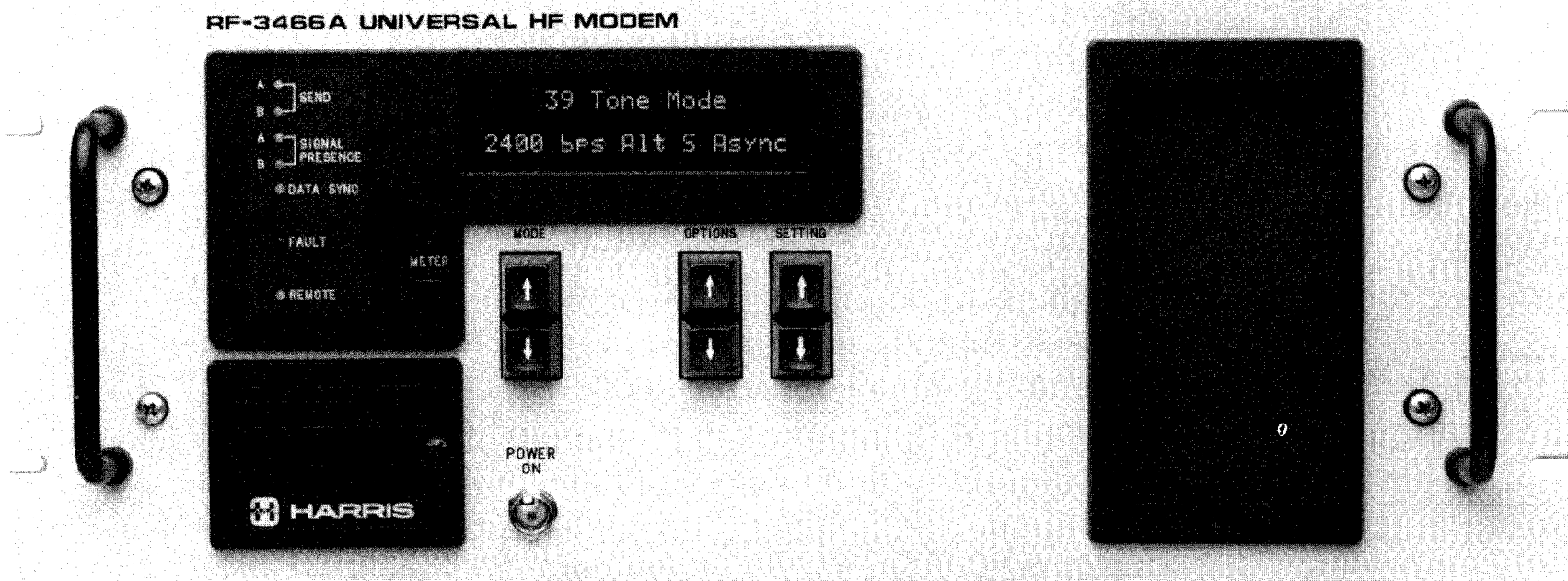
### ABOUT THIS MANUAL

The RF-346A Universal HF Modem Instruction Manual is divided into six sections. The first five sections contain information that will help the user understand, install, operate, and maintain the RF-3466A Universal HF Modem. Section 6 contains parts lists, component location drawings, and schematic diagrams for the major assemblies of the modem. A glossary follows the last tab section of this manual.

# **RF-3466A**

## **UNIVERSAL HF MODEM**

INSTALLATION AND OPERATION MANUAL



RF-3466A Universal HF Modem

## **SECTION 1**

### **INTRODUCTION**

#### **1.1 PURPOSE OF MANUAL**

This manual contains information necessary to install, program, operate, maintain, and repair the RF-3466A Universal HF Modem.

#### **1.2 SCOPE**

This manual is intended to give the technician and operator all the information needed to install, program, operate, and maintain the RF-3466A Universal HF Modem. The functions of each of the main assemblies are described through the use of functional block diagrams and text. In addition, the maintenance procedures supply all the information required to locate and replace faulty assemblies. However, detailed descriptions of individual components, such as specialized microprocessors, and advanced mathematical functions, such as fast Fourier transform, are beyond the scope of this manual.

#### **1.3 GENERAL DESCRIPTION**

The Harris RF-3466A Universal HF Modem is designed to combat the complexities of ionospheric propagation which limit the rates at which data may be passed over an HF radio link. In the high-rate mode, a channel transmission rate of 3466 bits per second, achieved by time differential phase shift keying (TDPSK) of 39 tones, is combined with a Forward Error Correcting code to produce data rates ranging from 2400 to 75 bits per second. In the FSK mode, the RF-3466A can operate with any binary FSK modem, from rates of 45 to 1200 bps. An optional robust serial tone mode provides reliable 75 bps communications at negative signal-to-noise ratios in channels which are severely stressed by fading, multipath spread, and interference.

The versatility and speed of the RF-3466A make it suitable for a variety of applications, including:

- Narrow-Band Secure Voice
- High-Speed Burst Data
- Digital Facsimile
- Slow-Scan Television
- Multi-Data-Rate Operation
- HF, Microwave, Land-Line

Figure 1-1 is a block diagram illustrating possible applications of the modem in an integrated communications system, including transmission of low-speed teletype, high-speed data, digital facsimile, or narrow-band secure voice. It can support either synchronous or asynchronous data terminal equipment, and can support dual-channel diversity (space, frequency, polarization).

The architecture of the RF-3466A is based on the TMS320 family of digital signal processors and 80186 microprocessor. The unit is, in essence, a general-purpose signal processor with input/output capabilities, and provides for waveform/feature expansion by PROM substitution. Extensive built-in-test functions are included.

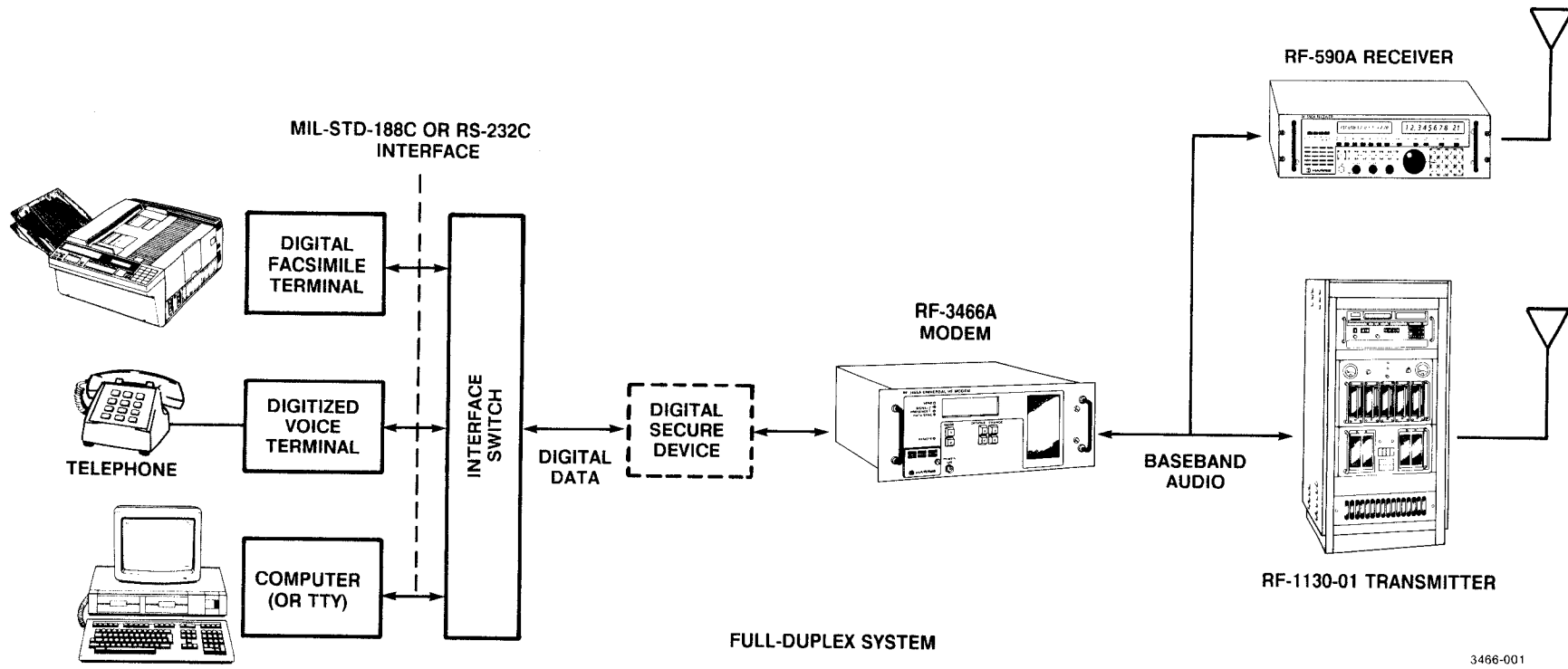


Figure 1-1. RF-3466A Universal HF Modem Applications

The high rate mode utilizes time-differential QPSK modulation of 39 tones, for a resultant channel rate of 3466 bps. Reed-Solomon coding and soft decision decoding, coupled with selectable time interleaving, provide for robust performance under marginal HF channel conditions. At rates of 600 bps and below, in-band time/frequency diversity gives added protection in selective fading and low signal-to-noise ratio (SNR). The waveform incorporates fast synchronization techniques and allows for rapid recovery from deep fades.

The modem also includes an FSK mode of operation for compatibility with virtually all types of binary FSK modulator/demodulators. User selection of mark/space frequency, over the range of 0 to 3400 Hz (1/2 Hz resolution), are accommodated. The design utilizes two completely independent FSK modulators and demodulators with independent mark/space/rate selections for each channel. The two mod/demod channels can also be configured for dual-channel diversity operation with equal-gain combining, for enhanced performance over the switched diversity technique offered by most other FSK modems. The binary FSK waveform is implemented with digital signal processing techniques throughout, resulting in low parts count and minimal user alignment.

A dual-mode configuration is provided whereby the modem offers both 39-tone and binary FSK operation simultaneously. Setup parameters for each mode/channel are completely independent, as is the data source for each channel. One possible application for this capability would be to allocate the 39-tone channel for HF traffic and the FSK channel for a land-line orderwire. Dual-channel diversity is not selectable in the dual-mode configuration. With the RF-3466A-05 option installed, a dual-mode configuration is also supported for simultaneous FSK and Robust Serial Tone operation.

#### **1.4 RADIO EQUIPMENT INTERFACE CRITERIA**

The RF-3466A is compatible with most commercial HF-SSB radio equipment including the Harris RF-1310 Exciter and RF-590 Receiver. However, certain criteria to be considered when selecting HF-SSB equipment to interface with the RF-3466A include:

- Envelope Delay Distortion
- Amplitude Distortion
- Intermodulation Distortion
- Synthesizer Phase Noise
- Synthesizer Frequency Deviation
- Transient Response Time (AGC and ALC)
- Interface Compatibility

Acceptable limits for these criteria are listed in table 1-1.

#### **1.5 DATA TERMINAL EQUIPMENT INTERFACE CRITERIA**

The RF-3466A has been designed to comply with EIA interface standard RS-232C and MIL-STD-188 interface standard. The RF-3466A can be configured for synchronous or asynchronous operation. Some operating criteria should be considered when selecting data terminal equipment to interface with the RF-3466A.

Table 1-1. Radio Equipment Requirements

Consideration	Limitation or Deviation
Envelope Delay Distortion	Less than 1 millisecond total for transmitter and receiver between 675 Hz and 2812 Hz.
Amplitude Distortion	Amplitude ripple between 300 Hz and 3000 Hz should not exceed 2 dB.
Intermodulation Distortion	Third order intermodulation distortion products should be at least 35 dB below PEP.
Synthesizer Phase Noise	Should not be great enough to degrade error rate, in back-to-back operation.
Synthesizer Frequency Deviation	$\pm 1$ part in $10^6$ (Normal Synchronization) $\pm 3$ parts in $10^7$ (Enhanced Synchronization) (Also, see section 3.9.15)
Receiver AGC	Decay time should be 1 second or longer when RF-3466 AGC is enabled.
Audio Interface	600-ohm balanced transmit and receive audio ports at + 5 dBm maximum, -25 dBm minimum.
Keyline and Muting	Up to 50 mA from current-limited source with maximum open-circuit output of 100 volts.

1.5.1 39 Tone General Considerations

- The RF-3466A requires the DTE to supply a Request-to-Send (RTS) to initiate transmission. If the DTE does not support RTS signaling, an external means of generating RTS must be provided.
- The RF-3466A will return a Clear-to-Send (CTS) signal to the DTE when it is ready to receive data. Any data sent by the DTE prior to CTS being asserted will be ignored.
- The DTE should drop the RTS between messages to ensure that a preamble is sent at the beginning of a new message.
- The Receive Line Signal Detect (RLSD) signal is active when the demodulator of the receiving modem is synchronized with the sending modem.
- Half-duplex may be selected at any data rate.

1.5.2 39 Tone Synchronous Operation

- TX clock and RX clock signals will be generated by the RF-3466A. The RF-3466A can also be configured to accept a TX clock from the DTE in 39-tone and optional robust serial tone modes.
- Clear-to-Send (CTS) will remain active until the RTS is dropped.
- Modem baud rate is internally set to 2400 bps for voice mode operation.

### 1.5.3 39 Tone Asynchronous Operation

- The RF-3466A and DTE use their own internal TX and RX data clocks.
- Sending and receiving DTEs must be set at same baud rate, character length, parity, and number of stop bits.
- CTS is dropped whenever the modem's input data buffer is full, if the DTE character length is 5 or 6 bits, or if the character length is 7 or 8 bits and XON/XOFF is disabled. CTS is reissued when the modem is ready to accept more data from the sending DTE. The CTS signal is dropped in response to the RTS signal being dropped.
- XON/XOFF control-character handshake is supported for character length of seven or eight bits, if this feature is enabled via the appropriate front panel setting (section 3). When enabled, XOFF is issued by the RF-3466A in response to a RTS. XON is issued when the RF-3466A is ready to accept data from the sending DTE. XOFF is reissued if the modem's input data buffer is full. This occurs if the baud rate of the transmitting modem is slower than the DTE.
- The CTS and/or XON/XOFF flow control features will normally occur only if the DTE rate exceeds the modem's front panel selected data rate.
- The RF-3466A supports echo back to the DTE.

### 1.5.4 FSK General Considerations

An RTS signal from the DTE causes the modem to issue a keyline to the transmitter. When the FSK modulator is set to ON the transmit audio signal from the modem is always present at the rear panel interface. In this case some transmit data could be lost due to the keyline delay of the transmitter. When the FSK modulator is set to SWITCHED the transmit audio is delayed by one second after the DTE issues the RTS signal. This in effect provides a keyline delay of one second to allow the transmitter sufficient time to key.

The RF-3466A will return a Clear-To-Send (CTS) signal to the DTE when it is ready to receive data. Any data sent by the DTE prior to CTS being asserted will be ignored.

The Receive Line Signal Detect (RLSD) signal is active when the demodulator of the receiving modem is receiving a valid signal from the transmitting modem.

### 1.5.5 FSK Synchronous Operation

TX clock and RX clock signals will be generated by the RF-3466A. Clear-To-Send (CTS) will remain active until RTS is removed.

### 1.5.6 FSK Asynchronous Operation

The RF-3466A and the DTE use their own internal TX and RX data clocks. Sending and receiving DTEs must be set at the same baud rate, character length, parity, and number of stop bits.

## 1.6 REMOTE CONTROL

The RF-3466A can be controlled from a remote location. The operating parameters that can be changed by the remote control are listed in table 1-2.

Transmissions can be initiated and terminated from the remote location. The RF-3466A is capable of reporting current operational and front panel LED status in response to polls from the remote control unit. The remote control interface is designed to EIA standard RS-422 and accepts a Harris-defined proprietary protocol.

**Table 1-2. Remotely Controllable Operating Parameters**

<b>39-Tone Mode</b>	
Data Rate	Interleaving
Channel Diversity	Sync/Async
Doppler Tracking (enable/disable)	
Self-test	
Full/Half-duplex	
<b>Binary FSK Mode</b>	
Modulator/demodulator mark/space tone frequencies	
Modulator/demodulator on/off control	
Modulator/demodulator data polarity	
Modulator transmit clock rate	
Demodulator threshold tracker on/off	
Demodulator Auto Mark Hold on/off	
Demodulator diversity on/off	
Demodulator baud rate	
Test routines	

**1.7 GLOSSARY OF TERMS AND ABBREVIATIONS**

Refer to the glossary section at the back of the manual for a list of terms, abbreviations, and acronyms.

**1.8 OPTIONAL EQUIPMENT**

Table 1-3 includes RF-3466A optional equipment information.

Table 1-3. Optional Equipment

Nomenclature	Description	Part Number	Manual/Supplement
RF-3466A-05	Robust 75 bps Serial Tone Option	10133-0090	SU-10133-0045
RF-3466-01	Rack Mount Kit.	10133-0050	10133-3020 (section 2)
RF-3466-02	Desktop Case.	1920-0400	10133-3020 (section 2)
RF-3466-03	Stack Mount Kit.	10133-0055	10133-3020 (section 2)
Extender PWB	Used to extend PWB assemblies above the chassis for troubleshooting.	10133-2050	N/A
12 Volt DC Power Supply Kit	Includes Power Supply and line cord.	10133-1270	SU-10133-0030
24 Volt DC Power Supply Kit	Includes Power Supply and line cord.	10133-1250	SU-10133-0030
RSK	Running Spares Kit.	1001-0542	N/A
SSK	Site Spares Kit.	1001-0647	N/A
RF-3502-08	Communications Terminal.	N/A	6919-6525
RF-3566-10 Series	Portable Personal Computer Terminal.	N/A	N/A
RF-3566-20 Series	Desk-top Personal Computer Terminal.	N/A	N/A
RF-3566-30	High speed ARQ. Requires RF-3566-10/20 series computer terminal.	N/A	N/A
RF-3567	Hard copy printer for RF-3566-10/20.	N/A	N/A
RF-3568-01	Digital Facsimile terminal. Requires RF-3566-30.	N/A	N/A
RF-3568-02	Digital Facsimile terminal.	N/A	N/A

## **SECTION 2**

### **INSTALLATION**

#### **2.1 GENERAL INFORMATION**

The RF-3466A provides an interface between a digital data source and an HF transceiver system. The unit can be configured for on-site or remote control use. This chapter describes general installation considerations and procedures. Actual installation procedures will depend upon the particular application. Items to consider when planning installation include: size and weight of the unit, availability of power, proximity of the modem to other equipment, accessibility of controls and indicators, and air flow.

Installation will include:

- Connecting the modem to a power source.
- Connecting cables to the rear panel.
- Selecting Internal, External 1 MHz, or External DTE frequency standard.
- Checking and adjusting audio output level.

##### **2.1.1 Tools and Equipment**

The following tools and test equipment are recommended to install and set-up the modem:

- True RMS Voltmeter such as the Fluke #8060A or HP3400A
- Standard Electronic/Technician Tools
- RS-232 Interface breakout box such as the Blackbox #SAM232-55 for troubleshooting RS-232 interface lines.

##### **2.1.2 Size**

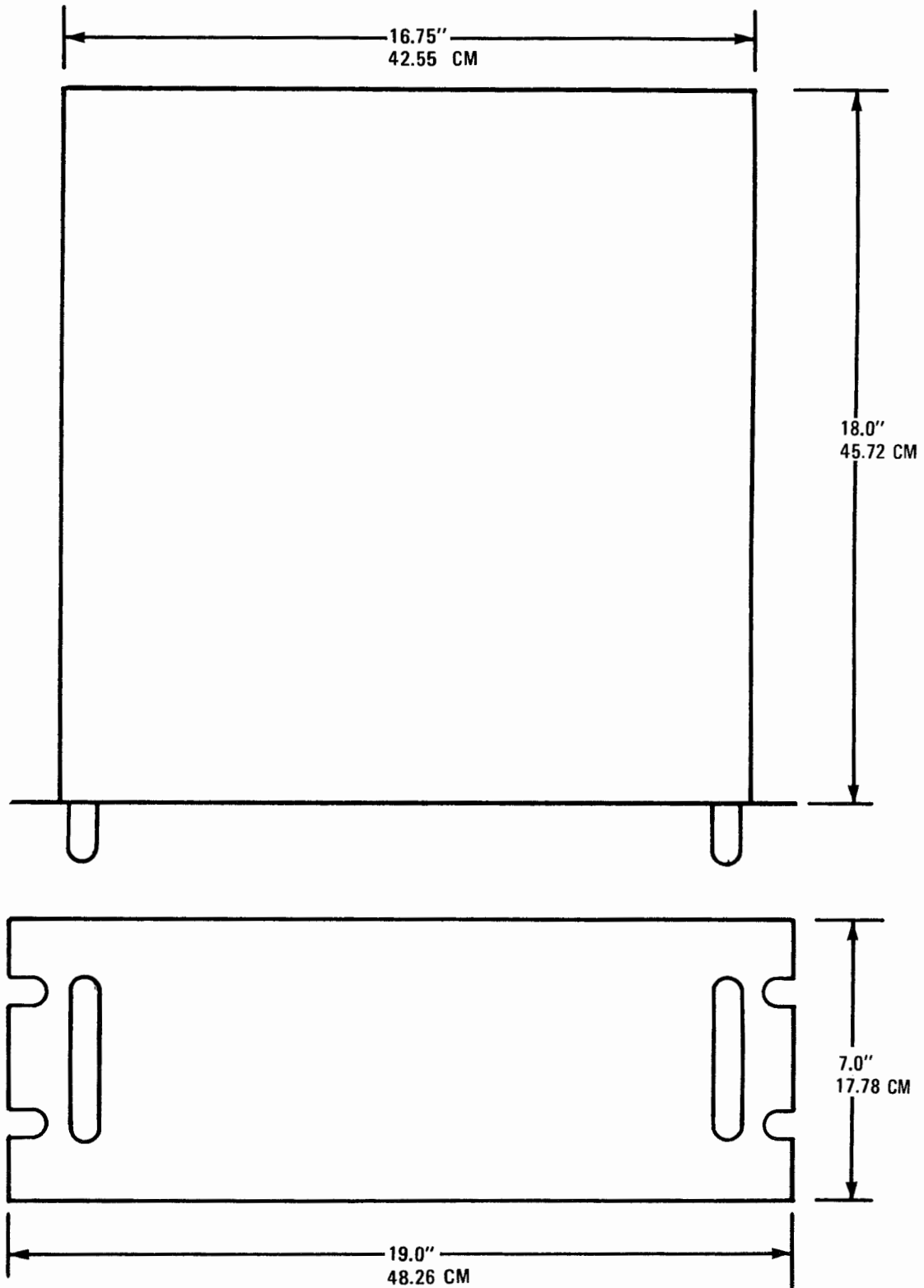
The modem's dimensions are shown in figure 2-1. The unit weighs 35 lbs. (15.9 kg).

##### **2.1.3 Power**

The RF-3466A requires a 90-150/150-300 Vac, 47-440 Hz, single-phase power source. The RF-3466A can, if required, be equipped to run from a 20 to 32 Vdc source, or 10 to 16 Vdc source (optional power supplies required). Maximum power dissipation is 80 watts.

#### **2.2 UNPACKING**

Carefully remove unit from shipping container and retain carton for repacking if necessary. Inspect for damage and check packing list to account for all equipment on the list. Notify carrier if unit is damaged or items are missing.



HSM-004

Figure 2-1. RF-3466A Dimensions

**2.3 ANCILLARY KIT**

Table 2-1 shows the items that are supplied with the RF-3466A Ancillary Kit (10133-3021).

**Table 2-1. Ancillary Kit (10133-3021)**

Quantity	Part Number	Description
5	F-0011	Fuse, 1-1/2 Amp, QA
5	F-0013	Fuse, 3.0 Amp, QA
1	J-0092	Connector, D, 15 Pin, Female
1	J22-0014-001	Connector, D, 9 Pin, Male
1	J22-0037-001	Connector, D, 25 Pin, Male
10	J45-0018-012	Connector, Pin
1	J55-0002-003	Connector Housing, 25 Pin
2	J55-0002-004	Connector Housing, 15 Pin
1	J55-0002-005	Connector Housing, 9 Pin
1	P-0096	Connector, D, 15 Pin, Male
1	10133-0015	Cable, Ac Power
1	10133-0019	Firmware Configuration

**2.4 MOUNTING OPTIONS**

The RF-3466A Universal HF Modem may be stack-mounted (P/N 10133-0055), or rack mounted (P/N 10133-0050). The rack mount kit includes the slide mounting bracket and all screws and washers needed for installation (figure 2-2).

**2.5 POWER CONNECTIONS**

**WARNING**

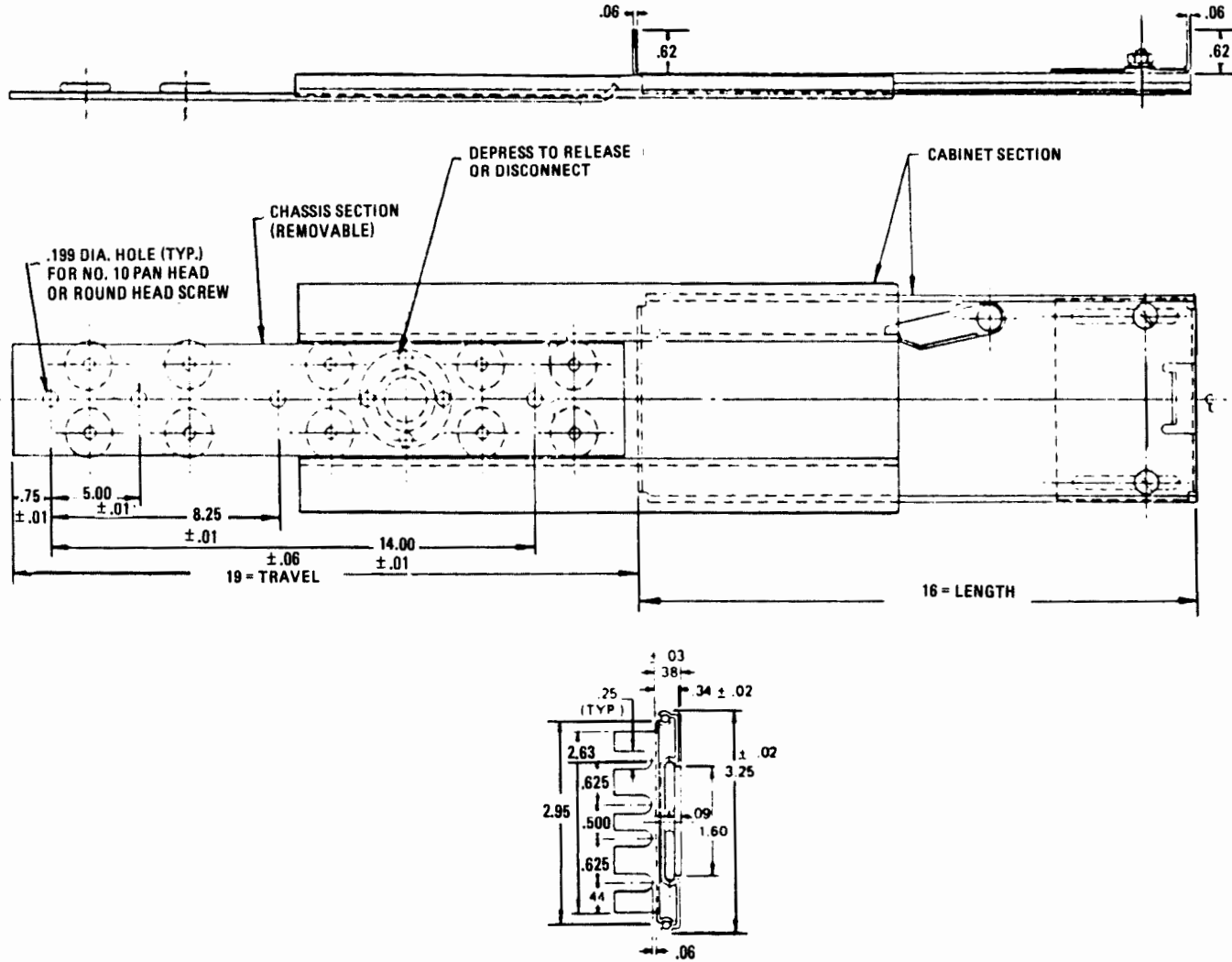
Do not energize this equipment unless the frame and all exposed metal parts are grounded.

If S1 is in the wrong position, severe damage to equipment and personal injury can occur.

Switch S1 on the Ac power supply must be set to the proper line voltage position before energizing. (See figure 2-3.)

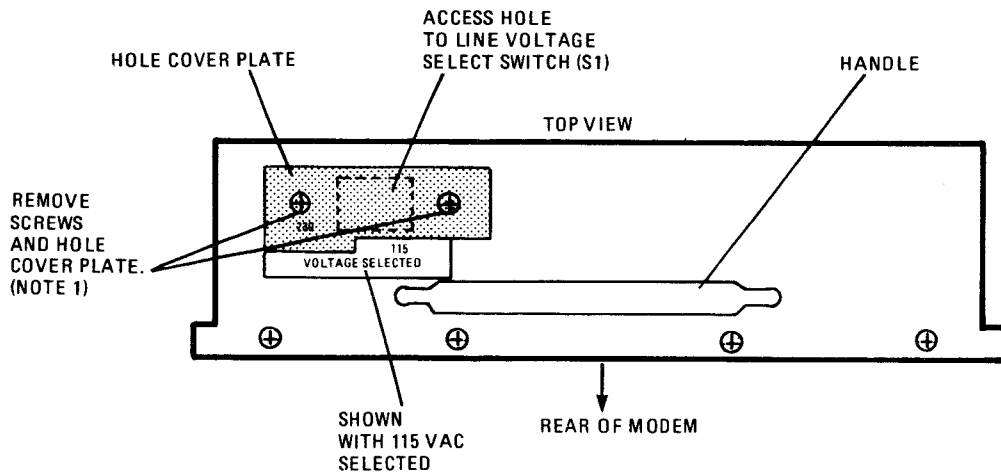
The RF-3466A Universal HF Modem can be powered by 115 Vac or 230 Vac line voltage. The installation kit includes line cords for connections to 115 Vac sources. Line cords for 230 Vac must be individually constructed for the particular applications. The line cord for the selected line voltage plugs into the power connector on the rear panel.

Removal and replacement procedures for the power supply are described in section 5.



HSM-005

Figure 2-2. Slide Mount Bracket Kit



**NOTES:**

- 1.) AFTER SETTING LINE VOLTAGE SELECT SWITCH (S1) REPLACE HOLE COVER PLATE SUCH THAT NOTCH IN PLATE LEAVES ONLY THE VOLTAGE SELECTED EXPOSED (230 OR 115 VAC).

HSM-043

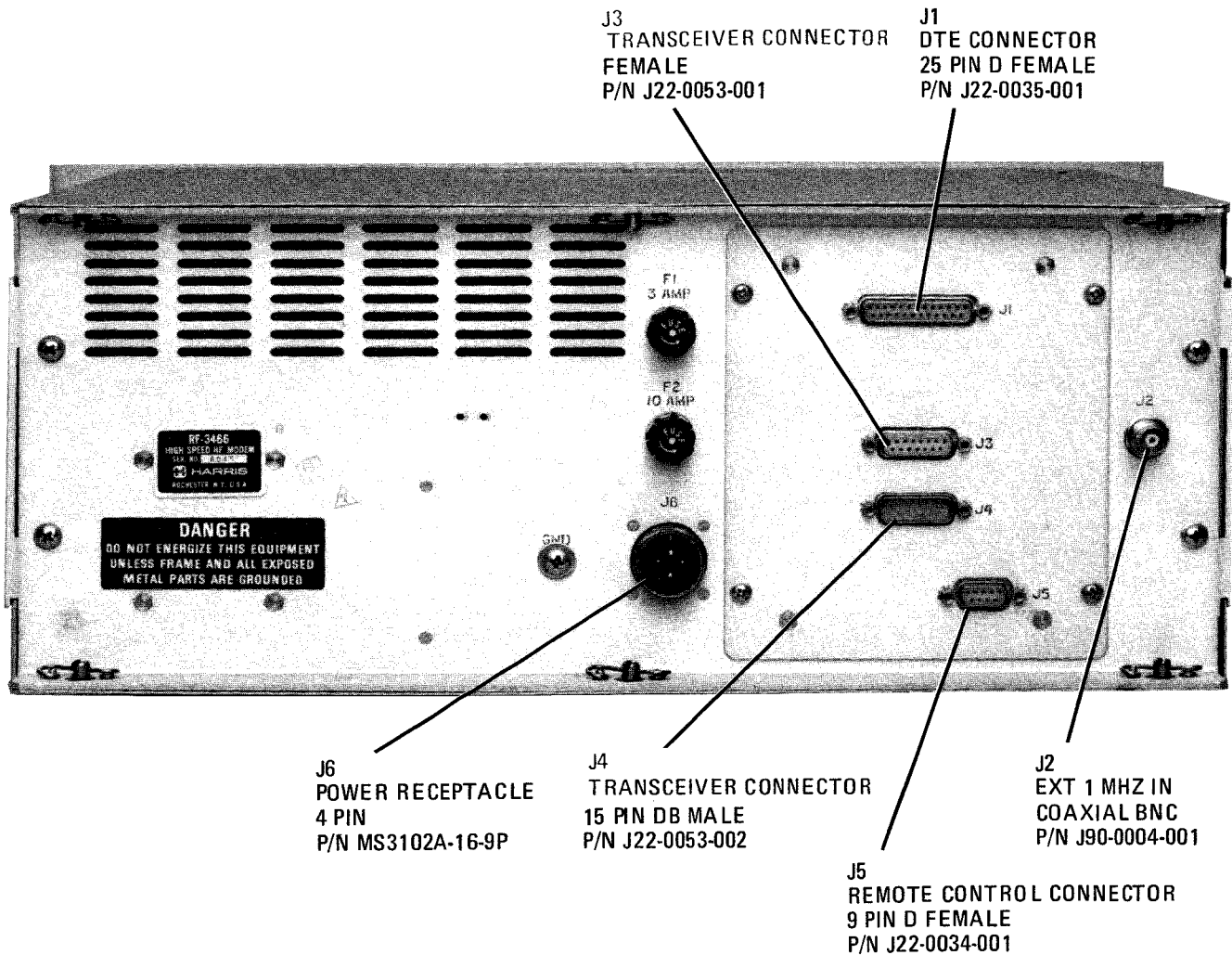
**Figure 2-3. Ac Power Supply Voltage Selection Switch**

**2.6 REAR PANEL CONNECTIONS**

All input, output, and power connections are on the rear panel. The rear panel connectors are listed in table 2-2 and identified in figure 2-4. Connector pin outs are listed in tables 2-3 through 2-7.

**Table 2-2. Rear Panel Connectors**

Connector Designated	Function	Type	Part No.
J1	DTE Connector	25 Pin, Female D	J22-0035-001
J2	Ext. 1 MHz Input	Coaxial BNC	J90-0004-001
J3	Transceiver Connector	15 Pin, Female D	J22-0053-001
J4	Transceiver Connector	15 Pin, Male D	J22-0053-002
J5	Remote Connector	9 Pin, Female D	J22-0034-001
J6	Power Input	4 Pin, Box Receptacle	MS3102A-16-9P



HSM-006P(A)

Figure 2-4. Rear Panel Connectors

Table 2-3. Data Terminal Connector J1 Pin Identification

Pin	Signal Name	Description/Remarks
1	Protective Ground	
2	TXD	Serial data from DTE
3	RXD	Serial data to DTE
4	RTS	Request-to-Send
5	CTS	Clear-to-Send
6	DSR	Data Set (Modem) Ready
7	Signal Ground	

Table 2-3. Data Terminal Connector J1 Pin Identification (Cont.)

Pin	Signal Name	Description/Remarks
8	RLSD	Modem has received signal and achieved data sync
11	SEC RXC	Secondary receive clock generated by RF-3466A
12	SEC RLSD	Secondary receive signal detect
13	SEC CTS	Secondary clear-to-send
14	SEC TXD	Serial data from DTE #2
15	TXC	Clock is generated by RF-3466A
16	SEC RXD	Serial data to DTE #2
17	RXC	Clock is generated by RF-3466A
18	SEC TXC	Secondary transmit clock generated by RF-3466A
19	SEC RTS	Request to Send from DTE #2
20	DTR	Data Terminal Ready
21	Not Used	Not Used
22	Not Used	Not Used
23	Not Used	Not Used
24	EXT TXC	Clock is generated by DTE #1
25	AUX IN 1	Not Used

Table 2-4. Connector J3 Pin Identification

Pin	Signal Name	Description/Remarks
1	AUDIO A OUT +	Channel A audio to XMTR
2	AUDIO A OUT -	Channel A audio to XMTR
3	RX MUTE A	
4	RX MUTE B	
5	AUDIO B OUT +	Channel B audio to XMTR
6	AUDIO B OUT -	Channel B audio to XMTR
7,8	FILT TX SPARE	Not Used
9	AUDIO A IN +	Channel A audio from RCVR
10	AUDIO A IN -	Channel A audio from RCVR
11	FILT TX SPARE	
12	KEYLINE A	
13	KEYLINE B	
14	KEYLINE COMMON	
15	MUTE COMMON	

Table 2-5. Connector J4 Pin Identification

Pin	Signal Name	Description/Remarks
1	AUDIO A IN +	Channel A audio from RCVR
2	AUDIO A IN -	Channel A audio from RCVR
3	RX SPARE	Not Used
4	RX SPARE	Not Used
5	AUDIO B IN +	Channel B audio from RCVR
6	AUDIO B IN -	Channel B audio from RCVR
7	SPARE	Not Used
8	RX MUTE A	
9	RX MUTE B	
10	RX MUTE COMMON	
11	AUDIO B OUT -	Channel B audio to XMTR
12	AUDIO B OUT +	Channel B audio to XMTR
13	KEYLINE B	
14	KEYLINE COMMON	
15	Not Used	

Table 2-6. Remote Connector J5 Pin Identification

Pin	Signal Name	Description/Remarks
1	GND	
2	Not connected	
3	422 OUT +	RS-422 Data Stream (+)
4	422 IN +	RS-422 Data Stream (+)
5	GND	
6	422 IN -	RS-422 Data Stream (-)
7	Not connected	
8	Not connected	
9	422 OUT -	RS-422 Data Stream (-)

Table 2-7. Power Connector J6 Pin Identification

Pin	Signal Name	Description/Remarks
A	Chassis Ground	
B	115 Vac/230 Vac	Hot
C	+ 24 Vdc	Not used for ac operation
D	115 Vac/230 Vac Return	Neutral

## 2.7 SYSTEM INTERCONNECTIONS

The RF-3466A can be used in several system configurations. Figure 2-5 illustrates typical configurations used for asynchronous and synchronous data terminal equipment. Figure 2-6 shows a diagram of typical configurations for transceiver operation and frequency diversity installations. Figure 2-7 diagrams a typical configuration for dual independent FSK or simultaneous FSK and 39 tone modes.

## 2.8 INITIAL SETUP AND CHECKOUT

At the time of installation, parameters for the modem's data interfaces must be selected and output audio level must be readjusted if a level other than 0 dBm is required. Interface parameters for the DTE and remote control unit, as well as other operating parameters, are selected at the front panel. All front panel settings are described in section 3. When the modem is shipped from the factory; however, it contains selected operating parameters for all modes of operation. These are shown in tables 2-8 through 2-13.

### 2.8.1 RS-232 or MIL-STD-188C Select

The modem is compatible with EIA interface standard RS-232C or the military interface standard MIL-STD-188C. Switch S-1, on the Filter Number One PWB Assembly (P/N 10133-1080), is used to select either interface standard. When using the MIL-STD-188C standard, switch S2 on the same assembly selects the logic polarity. The modem is normally configured for EIA RS-232C operation.

### 2.8.2 Audio Output Level Adjustment Procedure

#### CAUTION

DO NOT attempt to adjust R45 on the Analog I/O PWB. Adjustment of this potentiometer requires precision instruments and special procedures.

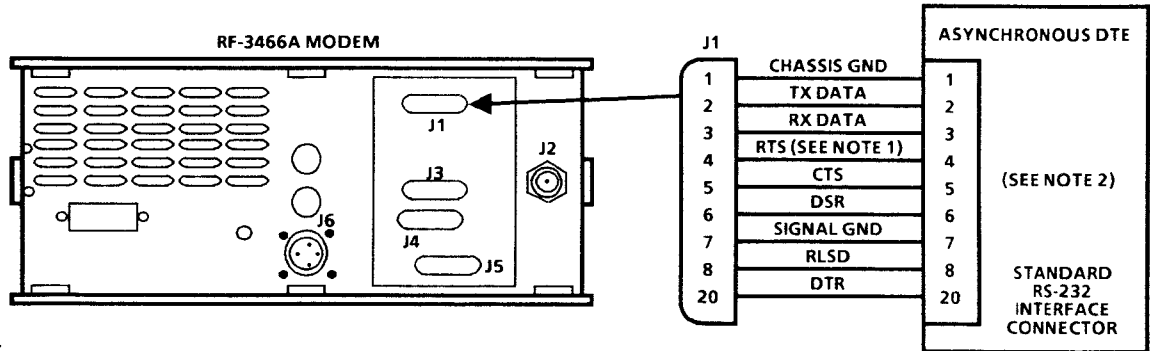
- a. Terminate both the AUDIO A OUT and AUDIO B OUT with 600-ohm loads. (This can be achieved by connecting modem to transmitter inputs.) Remove unit top cover.

#### NOTE

Refer to figure 2-8 for test point and potentiometer locations.

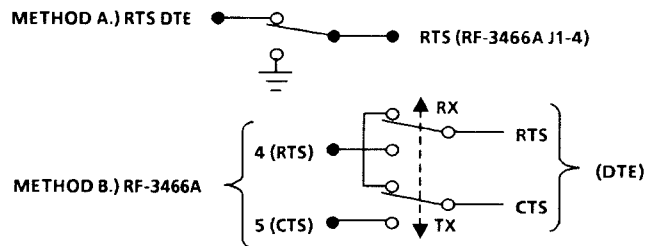
- b. At the rear panel, place a jumper between J1-4 (RTS) and J1-6 (DSR).
- c. Use a true RMS-reading meter (HP-3400A or equivalent) capable of measuring a 0-dBm (0.775  $V_{rms}$ ) signal and monitor the AUDIO A OUT signal between TP1 and TP2 on the Rear Panel Filter No. 2 PWB.
- d. Adjust R22 on the Analog I/O board until the AUDIO A OUT signal level measures whatever signal level is desired, from -16 dBm to +6 dBm.
- e. Measure the AUDIO B OUT signal level between TP3 and TP4 on the Rear Panel Filter No. 2 PWB. The signal level should measure within  $\pm 0.5$  dB of that measured at AUDIO A OUT. If not, readjust R22, and recheck the AUDIO A OUT signal level.
- f. Remove the jumper from J1-4 and J1-6 on the rear panel.

**A. TYPICAL MODEM-TO-ASYNCHRONOUS DTE INTERCONNECTIONS**

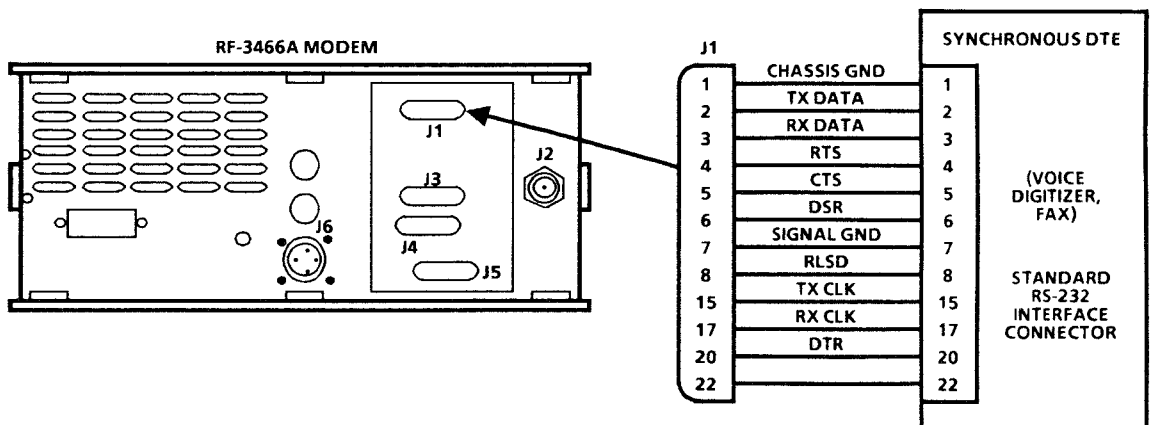


**NOTES:**

- 1.) IF THE DTE CONTINUOUSLY KEEPS RTS SIGNAL APPLIED THEN A TOGGLE SWITCH WILL BE REQUIRED TO BREAK RTS IN (RTS SIGNAL CAUSES RF-3466A TO KEY RADIO). TWO METHODS CAN BE USED TO WIRE THE SWITCH AS SHOWN: METHOD B.) IS REQUIRED ONLY IF THE DTE WILL NOT RECEIVE USING METHOD A.). THIS MAY BE THE CASE FOR TERMINAL EMULATOR PROGRAMS WHICH NEED TO HAVE A FULL DUPLEX LINK ESTABLISHED IN ORDER TO RECEIVE DATA.
- 2.) RF-3466A INTERNAL DIP SWITCHES MUST BE SET TO MATCH DTE CONFIGURATION.



**B. TYPICAL MODEM-TO-SYNCHRONOUS DTE INTERCONNECTIONS**



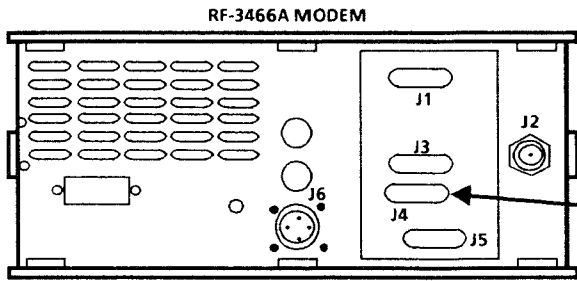
**NOTES:**

- 1.) THE RF-3466A MUST BE SET TO SYNC
- 2.) RF-3466A MUST BE SET TO FULL DUPLEX IF BOTH DTE AND RADIO ARE FULL DUPLEX. SET TO HALF-DUPLEX IF EITHER DTE OR RADIO IS HALF DUPLEX.
- 3.) BOTH TX CLK AND RX CLK ARE SUPPLIED BY THE RF-3466A TO THE DTE.

\*3466A-002

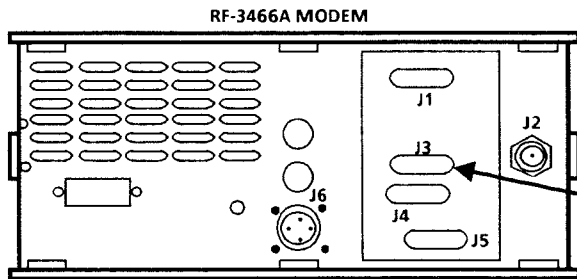
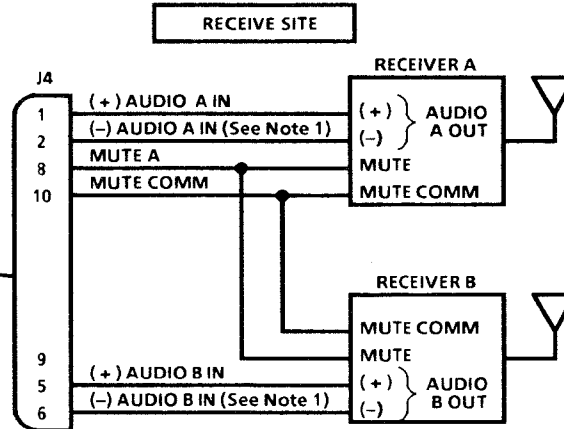
**Figure 2-5. Asynchronous and Synchronous Data Terminal Equipment Diagram**

FREQUENCY DIVERSITY OPERATION



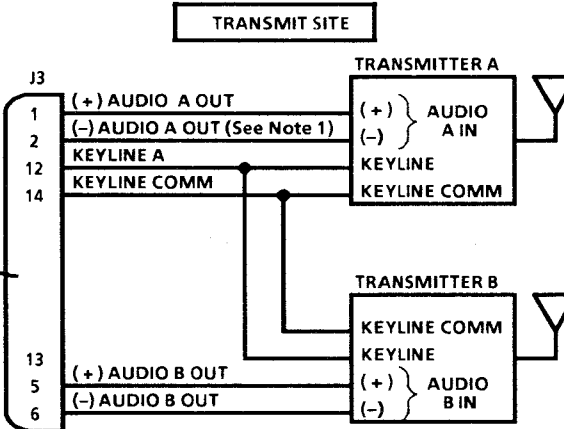
NOTES:

1.) AUDIO IN AND OUT SHOULD BE TWISTED PAIRS.

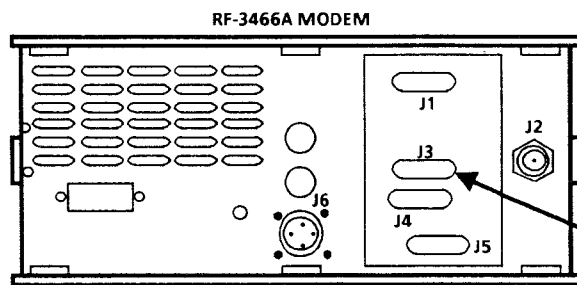


NOTES:

1.) AUDIO IN AND OUT SHOULD BE TWISTED PAIRS.

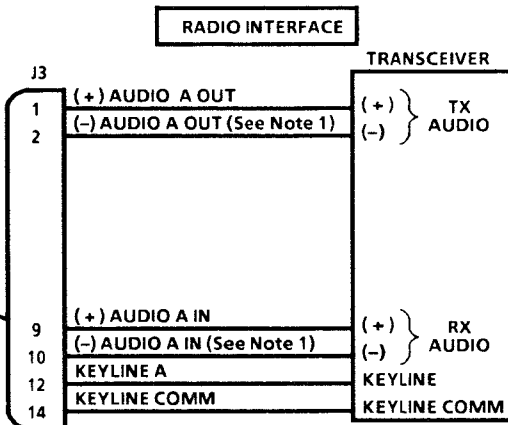


TRANSCEIVER OPERATION



NOTES:

1.) AUDIO IN AND OUT SHOULD BE TWISTED PAIRS.



\*3466A-003

Figure 2-6. Transceiver Operation and Frequency Diversity Diagram

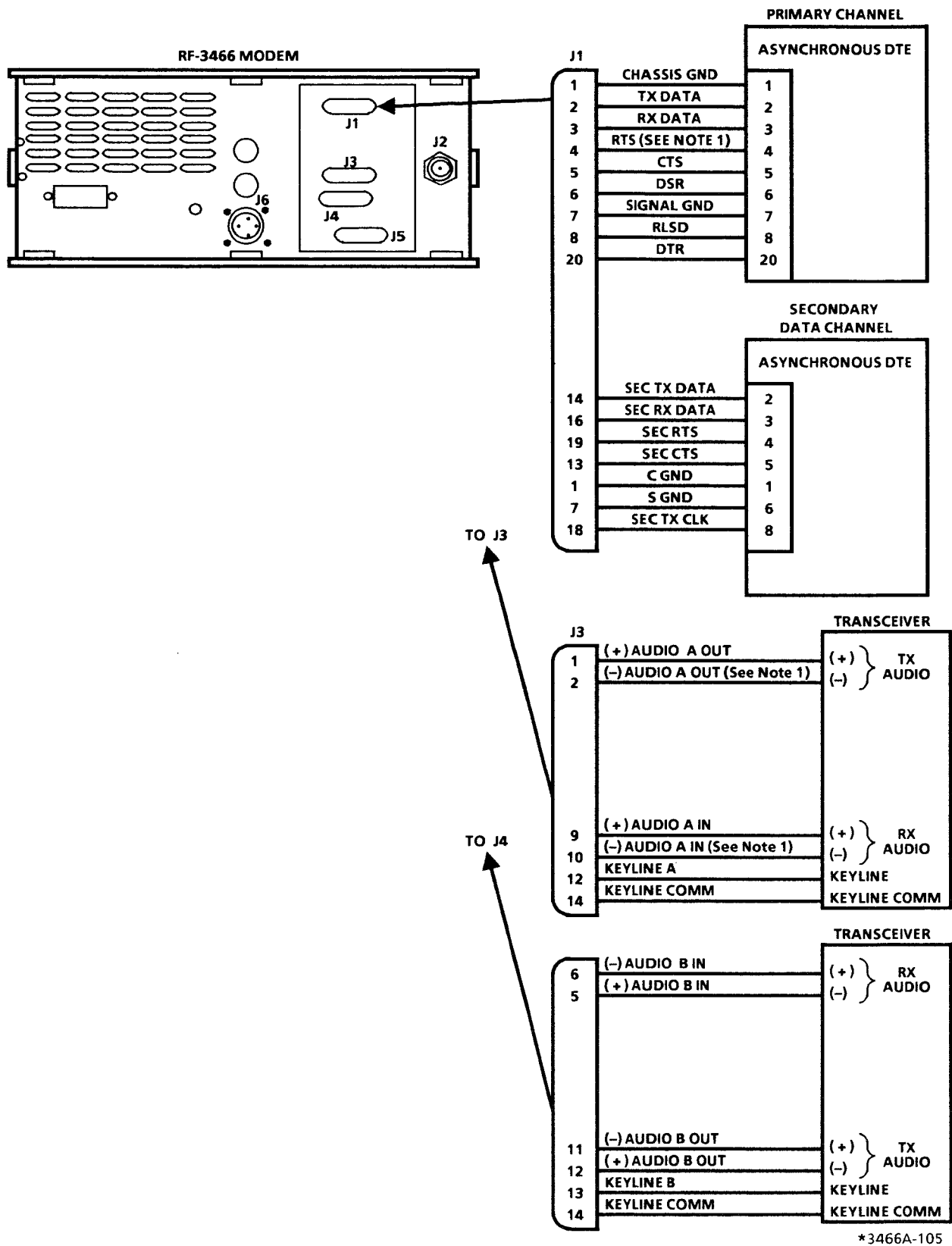


Figure 2-7. Dual Independent FSK or Simultaneous FSK and 39 Tone Mode

**Table 2-8. Selected Operating Parameters for Main Set Up Mode**

Parameter	Configuration as Shipped	Paragraph Reference
Remote Ident	255	3.9.1
Remote Rate	9600 bps	3.9.2
Power Up Bit	On	3.9.3
Halt/Fault	On	3.9.4
Loopback	Off	3.9.5
Clock	Internal	3.9.6
*Diag Rate	2400 bps	N/A
*Diag Parity	Off	N/A
*Diag Char Size	8	N/A
*Diag Stop Bits	1	N/A

\*For use by service personnel only

**Table 2-9. Selected Operating Parameters for 39-Tone Mode**

Parameter	Configuration as Shipped	Paragraph Reference
Rate	2400 bps	3.9.2
Interleave	Long	3.9.7
DTE	Synchronous	3.9.8
Chan	A only	3.9.9
Duplex	Full	3.9.10
Key Delay	45 ms	3.9.11
Clipping	On	3.9.12
Time/F Div	On	3.9.13
Dopplr Track	On	3.9.14
Acquire	Normal	3.9.15

**Table 2-10. Selected Operating Parameters for 39-Tone Mode  
 (if DTE is Asynchronous)**

Parameter	Configuration as Shipped	Paragraph Reference
DTE Rate	2400 bps	3.9.16
DTE Parity	Off	3.9.8
DTE Char Size	8	3.9.8
DTE Stop Bits	1	3.9.8
DTE Echo	Off	3.9.17
Async EOM	On	3.9.18
Flow	Xon/Xoff	3.9.19

**Table 2-11. Selected Operating Parameters for Robust Serial Option**

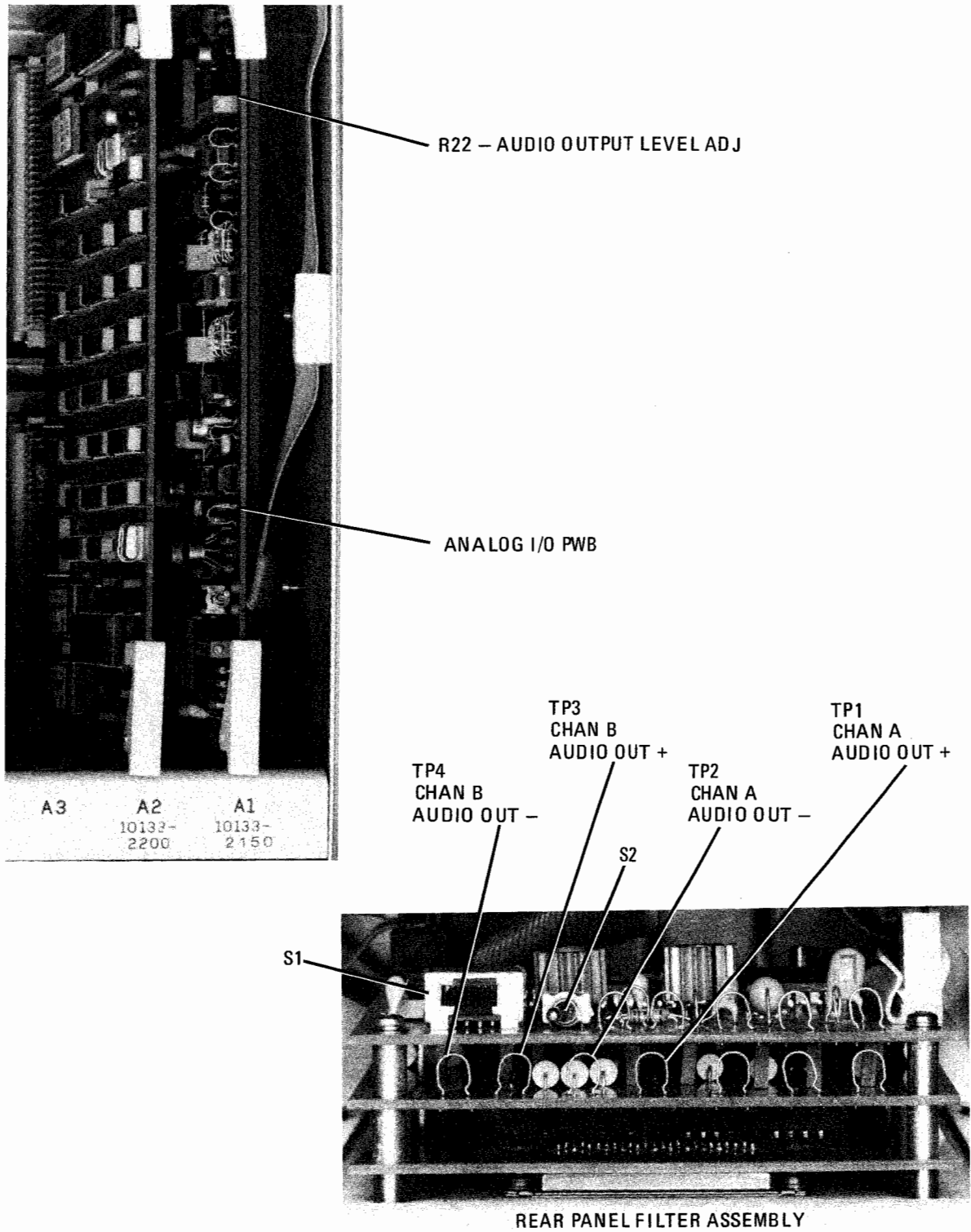
Parameter	Configuration as Shipped	Paragraph Reference
Interleave	9.6s	3.9.20
DTE	Synchronous	3.9.16
Chan	A only	3.9.9
Duplex	Full	3.9.10
Key Delay	45 ms	3.9.11

**Table 2-12. Selected Operating Parameters for Robust Serial Mode Option  
 (if DTE is Asynchronous)**

Parameter	Configuration as Shipped	Paragraph Reference
DTE Rate	2400 bps	3.9.16
DTE Parity	Off	3.9.8
DTE Char Size	8	3.9.8
DTE Stop Bits	1	3.9.8
DTE Echo	Off	3.9.17
Flow	Xon/Xoff	3.9.19

Table 2-13. Selected Operating Parameters for FSK Mode

Parameter	Configuration as Shipped	Paragraph Reference
Channel A		
Rx Rate	300 bps	3.9.21
Tx Mark	1575.0 bps	3.9.22
Tx Space	2425.0 bps	3.9.23
Rx Mark	1575.0 bps	3.9.24
Rx Space	2425.0 bps	3.9.25
Chan	Independent	3.9.26
Tx Rate	300 bps	3.9.27
Thresh Track	On	3.9.28
Mod Out	On	3.9.29
Polarity	Tx + Rx +	3.9.30
Mark Hold	Auto	3.9.31
Tune	Mark/Space	3.9.32
Track Tune	Off	3.9.33
Mod AB Mix	Off	3.9.34
DTE Rx Clock	A	3.9.35
Channel B		
Rx Rate	300 bps	3.9.21
Tx Mark	1575.0 bps	3.9.22
Tx Space	2425.0 bps	3.9.23
Rx Mark	1575.0 bps	3.9.24
Rx Space	2425.0 bps	3.9.25
Tx Rate	300 bps	3.9.27
Thresh Track	On	3.9.28
Mod Out	On	3.9.29
Polarity	Tx + Rx +	3.9.30
Mark Hold	Auto	3.9.31
B Analog In	B	3.9.36



HSM-009P(A)

Figure 2-8. Test Point and Potentiometer Locations

This completes the signal level adjustments. Remove test probes. Connect cables going to the transmitter and receiver. Set operating parameters (paragraph 2.8) before replacing the top cover.

**2.8.3 Frequency Standard**

The RF-3466A has a built-in 9600-Hz frequency standard, with a stability of 10 parts-per-million. To select this internal standard, set the CLOCK option in the Main Setup mode to "Internal", as described in paragraph 3.8.1.

Either of two external frequency standards can be used in place of the internal frequency standard. An external 1-MHz signal, with a level between 0.7 and 2.0 Vrms, may be injected at rear panel J2 when a higher degree of accuracy is required. To select this external standard, set S2-1 of the A8 assembly to OPEN, and set the CLOCK option in the Main Setup mode to "Ext 1 MHz". Note that A8 S2-1 must be set CLOSED if an external 1 MHz standard is not connected to the RF-3466A or improper operation may occur.

In synchronous mode, the RF-3466A normally supplies both the transmit and receive clocks to the connected data terminal. When DTE external clock option is selected, the data terminal supplies the transmit data clock to the RF-3466A, while the RF-3466A still supplies the receive data clock. The frequency of the external transmit clock input must be the same as the baud rate (75 to 2400 Hz) between the data terminal and the RF-3466A modem, and must be accurate to within 10 parts per million. Therefore, it must be the same as the baud rate set at the remote control or RF-3466A modem. The external transmit clock input must be present at pin 24 of rear panel J1 and provide an RS-232 logic level. DTE external clock option is only available for synchronous operation. To select this clock, set the CLOCK option in the Main Setup Mode to "Ext DTE".

**2.8.4 Switch and Jumper Configurations**

Table 2-14 shows the switch and jumper configuration as shipped for all RF-3466A PWBs. This information is supplied in the event of assembly replacement or repair.

**Table 2-14. Switch and Jumper Configurations**

Assembly	Switch Setting/ Jumper Installed	Function
A1	S1 - Normal E1 to E2, E4 to E5 E7 to E8	Multiplier Calibration + 5 dBm to -25 dBm Audio Input Range AGC Enabled
A2	E3 to E4 E7 to E8	HIL Done - Polarity Invert FFT Done - Polarity Invert
A4	E50 to E51 E53 to E54	DMA Request 0 Invert DMA Request 1 Invert
A5	E2 to E3	DMA Request Invert
A6	E50 to E51 E53 to E54	DMA Request 0 Invert DMA Request 1 Invert
A7	E55 to E56 E58 to E59	FEC/IO Interrupt Mod/Demod Interrupt

Table 2-14. Switch and Jumper Configurations (Cont.)

Assembly	Switch Setting/ Jumper Installed	Function
A8	E1 to E2 S2-1 Closed S2-2 Closed	Watchdog Timer Enable EXT 1 MHz Disable Reserved
A12A1A1	E2 to E3 S1-EIA S2-POS	Clock Polarity Select DTE Level Select MIL-188 DTE Data Polarity Select

SECTION 3

OPERATION

3.1 INTRODUCTION

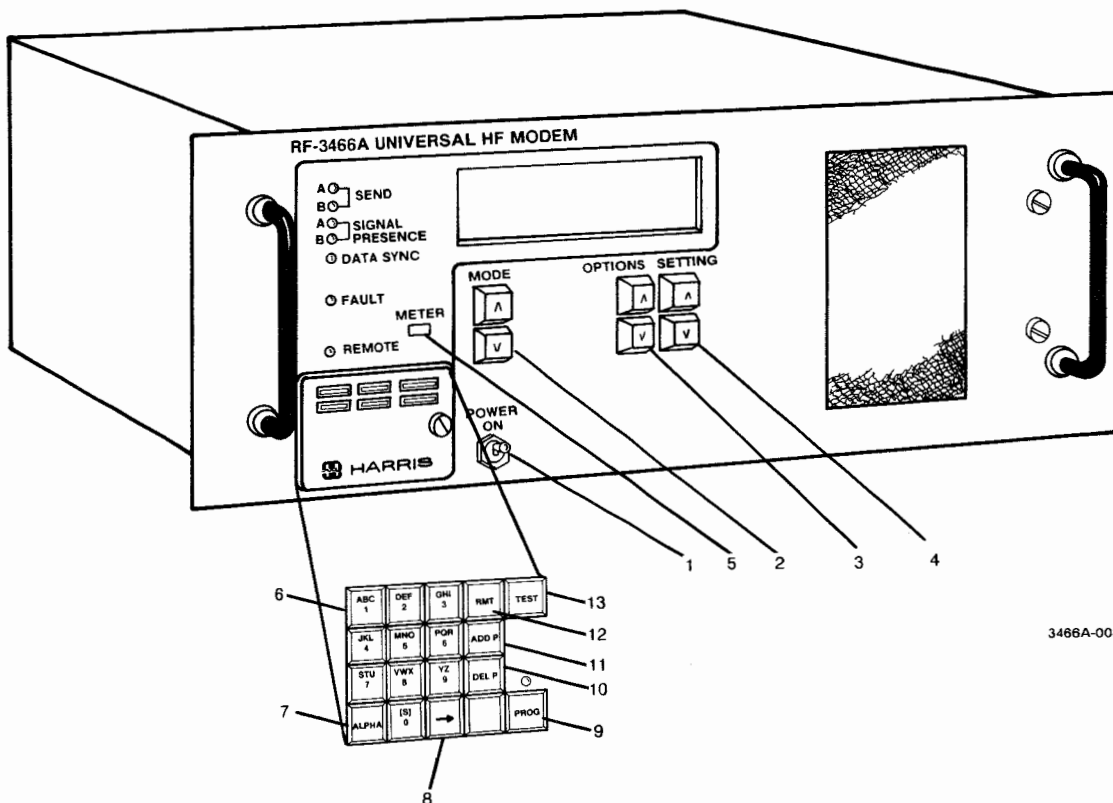
The RF-3466A is a versatile modem which has been designed to meet two basic operational needs:

- Manual operation giving complete control over all modem functions
- Preset operation allowing fast recall of complex equipment setups

This section describes all front panel controls and indicators, followed by descriptions of manual and preset modes of operation. Self test and remote control operation are described in detail. The section concludes with a detailed functional description of all modes, options, and settings.

3.2 CONTROLS AND INDICATORS

All operational controls and indicators are located on the front panel. Figure 3-1 and table 3-1 illustrate and describe the RF- 3466A controls. Note that some controls are located behind a closed door. In general, these controls are used for programming preset information and are not needed for routine operations.



3466A-008

Figure 3-1. RF-3466A Front Panel Controls

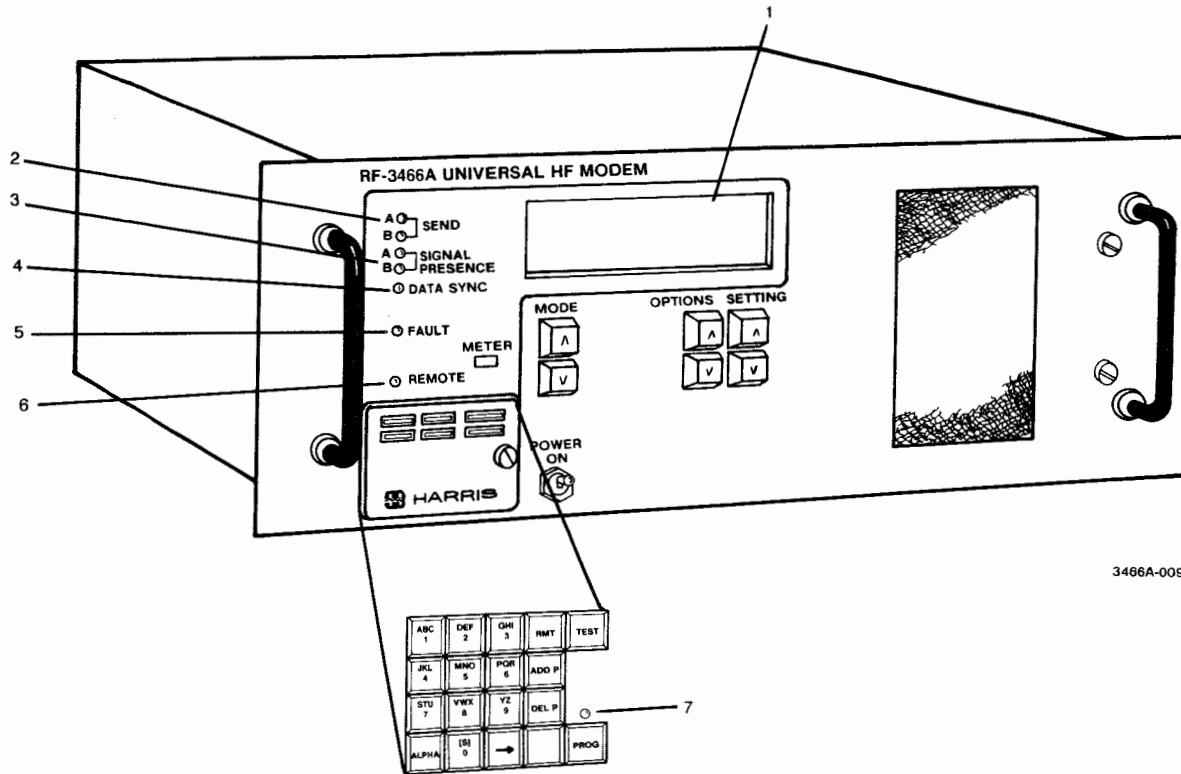
Table 3-1. RF-3466A Front Panel Controls

Item No.	Control	Function
1	POWER ON	Main power switch.
2	MODE	Two arrow buttons that scroll through the available modes of operation.
3	OPTIONS	Two arrow buttons that scroll through the options that are available for the mode selected.
4	SETTING	Two arrow buttons used to select a setting for the option shown on the alphanumeric display.
5	METER	A toggle button used in FSK mode to display the mark and space signals. When the METER pushbutton is initially pressed, the display shows the mark and space signal levels for the FSK A channel using a bargraph. When pressed a second time the display shows the mark and space signal levels for the FSK B channel. When pressed a third time, the display reverts to the normal control display.
6	ALPHANUMERIC KEYPAD	Used for alphanumeric entry of settings or preset names.
7	ALPHA	During entry of preset names, this button allows the number at the right-most position in the field to be turned into a letter. Successive depressing of the ALPHA button causes the character to be rolled through all of the letters marked on the number button, and back to the original number.
8	----->	Active during entry of preset names. This pushbutton causes the characters in the display to be right-shifted. The right most letter is shifted out of the display and deleted by this edit feature.
9	PROG	A toggle button used to access the PROGRAM mode. This mode allows access to the Main Set Up Mode and all options for all modes.
10	DEL P	Functions only in PROG mode. Used to delete preset names from memory.
11	ADD P	Functions only in PROG mode. Used to add preset names to the memory.
12	RMT	Allows selection of remote or local control. Only the OPTIONS button is operational in the remote mode. This allows the user to view the settings of the modem in the displayed mode of operation.
13	TEST	Allows selection of self-test mode. When the TEST pushbutton is pressed, the operator is prompted to press ALPHA to run a self test.

Figure 3-2 and table 3-2 illustrate and describe the RF-3466A indicators. Note that a diagnostics connector located just above the PROG LED is used by service personnel to perform testing on the modem.

### 3.2.1 Send

The SEND Lamp is turned on when the modem modulator begins to transmit data.



3466A-009

Figure 3-2. RF-3466A Front Panel Indicators

Table 3-2. RF-3466A Front Panel Indicators

Item No.	Control	Function
1	ALPHANUMERIC DISPLAY	The top line of the display shows the modem's current mode of operation. The second display line shows the options available and the selected setting for the option.
2	SEND A and B LED	Green LED lights to indicate that data is being sent.
3	SIGNAL PRESENCE A AND B LED	Green LED lights to indicate that acceptable signals are being received.
4	DATA SYNC LED	Green LED lights to indicate that modem is synchronized with a sending station, (39 tone and Robust Serial modes).
5	FAULT LED	Red LED lights to indicate the presence of a fault condition. See section 5 to evaluate fault messages.
6	REMOTE LED	Green LED lights to indicate modem is being remotely controlled.
7	PROG LED	Green LED flashed to indicate modem is being operated in PROGRAM mode.

### 3.2.2 Signal Presence A and B

These lamps indicate that the modem demodulator is receiving a signal in channel A or B, respectively, which meets an established signal-to-noise ratio threshold. A valid SIGNAL PRESENCE indication does not necessarily imply that the modem is synchronized with the received signal, nor does it imply that the bit error rate is meeting an established threshold criteria.

### 3.2.3 Data Sync

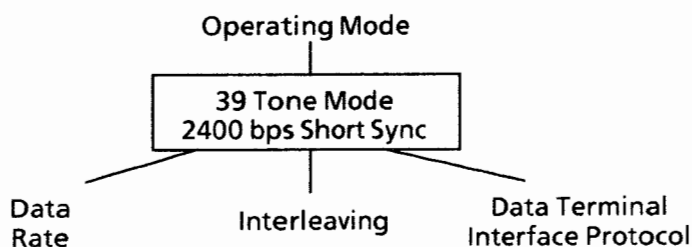
The DATA SYNC lamp indicates that the forward error correction decoder has synchronized on the incoming message, and is maintaining synchronization over the duration of the message. At the conclusion of a received message, or during a signal fade, the DATA SYNC condition is held for a time to ensure that it is really the end of the message. If another incoming message is received during this DATA SYNC hold time, the DATA SYNC is reset and synchronization is then established on the new message. The DATA SYNC hold time is a function of the modem baud rate and the interleaving delay. DATA SYNC is not used in FSK modes.

## 3.3 MANUAL OPERATION

Basic control of the RF-3466A is through the three pairs of arrow buttons directly below the alphanumeric display. These buttons control the following parameters:

- Operating mode
- Options available for each operating mode
- Settings for the available options

In both the manual and preset modes, the current mode of operation is displayed on the first line of the alphanumeric display. The second line contains status information for that mode of operation; i.e., the most important information for the mode. The following shows a typical alphanumeric display for 39 tone mode.



Dual modes of operation use two status lines: one for the primary mode of operation and the other for B channel FSK. The status lines are exactly the same as in the above example, except that the secondary status (B channel FSK) is accessed by pressing the OPTION up pushbutton.

A detailed list of options and settings available for each operating mode is found in paragraphs 3.8 and 3.9.

### 3.3.1 Selecting an Operating Mode

The list of operating modes, as they appear on the alphanumeric display, include:

- Main Set Up Mode (only shown in PROG mode)
- Fixed Preset Mode (see paragraph 3.4)

- Preset Mode (see paragraph 3.4)
- 39 Tone Mode
- Robust Serial Mode (only shown if the option is installed)
- FSK Mode
- 39 Tone/FSK Mode
- Rob Serial/FSK Mode (only shown if the option is installed)

The MODE pushbuttons are used to scroll through the list of modes of operation.

### 3.3.2 Selecting Operating Parameters.

Each operating mode has a set of operating parameters associated with it. By pressing the OPTIONS pushbutton, the modem scrolls through a frequently used list of operating parameters and their current settings. To access a complete list of operating parameters, the modem must be in PROGRAM mode.

### 3.3.3 Changing Operating Parameters

To change an operating parameter, press either SETTING pushbutton with the option showing and the modem will scroll through the list of available settings for that option. The setting that appears on the alphanumeric display is the current setting for the modem.

### 3.3.4 Saving Selections as a Preset

After selecting the operating parameters for an operating mode, the operator may wish to store the selection in the modem's memory as a preset.

To do this, the operator can be in any mode (except Preset Mode). After selecting the options for the mode, press the PROG pushbutton and then the ADD P pushbutton. (Add Preset only functions in the program mode.) The display prompts for the name of the preset to be added. For example:

39 Tone Mode
Name ? _____

The user enters the name (up to 12 characters) by using the numerical keypad for number entries or by using the ALPHA button to change the number entries to letters. The ALPHA pushbutton allows the number at the right-most position in the field to be turned into a letter. Successive depressing of the ALPHA button causes the character to be rolled through all of the letters marked on the number button, and back to the original number.

The -----> pushbutton is an edit feature that causes the characters in the display to be right-shifted. The right most letter is shifted out of the display and deleted.

After entering the new preset press the PROG pushbutton to return to normal operation. If the user now scrolls over to Preset Mode, the new entry will be listed as the next available preset number.

## 3.4 PRESET OPERATION

The RF-3466A contains two operating modes that use preset information: the Fixed Preset Mode and the Preset Mode.

The Fixed Preset Mode contains presets that have been programmed before the modem is shipped and cannot be changed. When the Fixed Preset Mode is selected by the MODE pushbutton, the OPTIONS buttons are disabled; however, the SETTING buttons allow the operator to view the presets. Fixed Preset Mode can be used as an operating mode or as a baseline for creating custom presets.

The Preset Mode contains presets that have been programmed by the user. When the Preset Mode is selected by the MODE pushbutton, the OPTIONS buttons are disabled; however the SETTING buttons allow the operator to view the presets.

Presets are listed in numerical order (01, 02, 03, etc).

A detailed list of options and settings available for each operating mode is found in paragraph 3.7.

### 3.4.1 Entering the Preset Mode

The Preset Mode is entered by pressing the MODE buttons until the display shows Preset Mode. When in Preset Mode, each of the presets can be accessed by pressing the SETTING buttons. (The OPTIONS buttons are inactive.) The first entry in the preset list is the manual setting. The alphanumeric display shows:

Preset Mode Manual Setting
-------------------------------

### 3.4.2 Selecting a Preset

Pressing the SETTING buttons cause the modem to scroll through the selected presets until the selection comes back to the Manual Setting position. An example of a preset display would be:

Preset Mode		
01 Name		Terminal 1

### 3.4.3 Reviewing the Operating Parameters of a Preset

When a preset is selected, the operator can view the settings for that preset by pressing either of the MODE pushbuttons. The display will switch to the mode of the selected preset and display a P in the top left corner:

P	39 Tone Mode	
A02 Chan		B Only

The user can then examine the parameters by using the OPTIONS buttons. Pressing the MODE buttons a second time will return the display to the preset mode.

### 3.4.4 Temporary Alteration of a Preset's Parameters

When the operator is reviewing the parameters for a preset described above, all of the buttons are functional and the options can be changed; however, this is a temporary change and the preset will revert to the original settings when a MODE pushbutton is pressed. This feature can be used to change data rates or other parameters of a temporary nature.

The changes can be saved by using the ADD P pushbutton to create a new preset, as described in paragraph 3.3.4.

### 3.4.5 Deleting a Preset

To delete a preset, the user must be in the Preset menu and the PROG mode. Use the SETTING button to select the preset to be deleted. Then, press the DEL P (Delete Preset) pushbutton. The display will show:

Press ALPHA - delete  
Press other - bypass

If the ALPHA pushbutton is pressed, the preset is deleted and the display shows the next preset on the list. If any other button is pressed, the display shows the currently selected preset. In either case, PROG mode is terminated and must be reselected in order to delete another preset.

When a preset is deleted, the number it was given when it was added is left blank. For example, if a modem has five presets stored in memory, they would occupy the numbers 01, 02, 03, 04, and 05. If the operator deletes the 03 preset, the list of presets would read: 01, 02, 04, and 05. The next added preset would become 03.

### 3.4.6 Exiting Preset Mode

Use the SETTING buttons to scroll through the list of presets until the manual setting appears on the display:

Preset Mode  
Manual Setting

Now the MODE pushbuttons can be used to exit to another operating mode.

## 3.5 METERING

The METER button on the front panel is a toggle button that functions only when using one of the FSK modes. It allows the received signal to be fine-tuned for optimum performance. When using an FSK mode, pressing the METER button the first time causes the display to change to a bar graph. This bar graph shows the received mark and space tone signal levels for FSK channel A. Pressing the METER button a second time shows the received mark and space tone signal levels for FSK channel B. Pressing it a third time returns the display to its original form. In dual waveform modes pressing the METER button causes the display to show signal levels for FSK channel B. Pressing it again returns the display to its original form.

To fine-tune a received signal, the option to be tuned should be selected using the OPTIONS buttons. Next, the METER button is pressed to display the signal levels for the desired channel. By pressing the SETTINGS buttons the frequency of the option can be incremented or decremented in 1/2-hertz steps. If the SETTINGS buttons are held down the frequency will increment or decrement until the button is released. By watching the bar graph display the signal can be fine-tuned to achieve maximum signal strength. Note that the mark and space frequencies can be tuned independently, or the center frequency can be tuned which effectively tunes mark and space tones simultaneously.

## 3.6 SELF-TEST

The RF-3466A contains a built-in test (BIT) feature that is designed to test as much of the modem as possible without operator intervention. This modem self-test can be entered in two ways. There is also a short self-test of the front panel that can be used if the front panel controls are unresponsive.

If the FAULT LED lights or an error message is displayed during any of the above test procedures, consult the maintenance section of this manual.

### 3.6.1 Self-Test on Power Up

When the Power Up BIT option is turned on in the Main Set Up Mode, the self-test occurs automatically on power up. The alphanumeric display will say TEST IN PROGRESS while the following occurs at the front panel:

- The front panel LEDs will alternately turn on and off. This occurs for approximately 32 seconds during the modem's self test routine.
- When the self-test routine is complete, all the LEDs will turn on for one second and then turn off. The alphanumeric display will then show the last mode of operation for which the modem was set.
- If a fault was detected, the fault lamp will stay on and the display will identify failed modules.

### 3.6.2 Using the TEST Button for Self-Test

The self test can also be executed by pressing the TEST pushbutton after the modem is turned on. After pressing TEST the user is prompted to begin the test. The display will show:

Press ALPHA - test  
Press 9 - bypass

When the self-test is done this way, TEST IN PROGRESS does not appear on the alphanumeric display. Instead, individual tests are listed on the alphanumeric display with the words PASS, FAIL, OR TIMEOUT after each test.

### 3.6.3 Testing the Front Panel Controls

To test only the front panel controls, press and hold the TEST pushbutton, then turn the power on. The TEST button must be held approximately one second after turning on the power. A brief test of the front panel controls will occur. To end the test, turn power off. (See paragraph 5.4.3 for a detailed explanation of the front panel controls test.)

## 3.7 REMOTE CONTROL OPERATION

The RF-3466A can be controlled from a remote location. The RMT pushbutton toggles between remote and local control. In remote control, the REMOTE LED lights on the front panel and all controls are non-functional except for the OPTIONS pushbuttons. If an operating parameter can be remotely controlled, it is noted in a special column in tables 3-3 through 3-16.

## 3.8 FUNCTIONAL DESCRIPTIONS

This paragraph describes in detail all MODE, OPTIONS, and SETTING selections that can be made for each selectable operating mode. It also notes which parameters can be remotely controlled. Manual Mode selections are separated from Program Mode selections. Program selections are also given for 39-tone and robust serial modes, when the data terminal interface is asynchronous.

It is important to note that any setting changes made to a given waveform will affect all modes which use that waveform. For example, changes made in 39 Tone mode will affect the 39 Tone/FSK mode. Similarly, changes made to the FSK portion of Robust Serial/FSK would affect both FSK mode and 39 Tone/FSK mode.

Options and settings are described in paragraphs 3.9.1 through 3.9.37.

### 3.8.1 Main Set Up Mode

The Main Set Up Mode contains unit specific parameters which pertain to operation of the modem. It can only be entered when the modem is in Program mode. None of the operating parameters in the Main Set Up Mode can be remotely controlled. The parameters, as they appear on the alphanumeric display, are listed in table 3-3.

**Table 3-3. Main Set Up Mode  
(Available Only in Program Mode)**

Option	Setting	Paragraph
01 Remote Ident	1 to 255	3.9.1
02 Remote Rate	75 150 300 600 1200 2400 4800 9600	3.9.2
03 Power Up Bit	Off On	3.9.3
04 Halt/Fault	Off On	3.9.4
05 Loopback	Off On	3.9.5
06 Clock	Internal Ext DTE Ext 1Mhz (if enabled)	3.9.6
07 Diag Rate*	75 150 300 600 1200 2400 4800 9600	N/A
08 Diag Parity*	Off Odd Even	N/A
09 Diag Char Size*	7 8	N/A
10 Diag Stop Bits*	1 2	N/A

\*These options used by service personnel only.

### 3.8.2 39-Tone Mode

The selectable options are listed in tables 3-4 (manual mode), 3-5 (program mode), and 3-6 (if the data terminal equipment is asynchronous). It is also noted in the tables whether the option is remotely controllable.

**Table 3-4. 39-Tone Mode (Manual Mode Selections)**

Option	Setting	Remotely Controllable	Paragraph
01	Rate 75 bps 150 bps 300 bps 600 bps 1200 bps 2400 bps 2400 voice	X	3.9.37
02	Interleave Short Long Alt S Alt L	X	3.9.7
03	DTE Asynchronous Synchronous	X	3.9.8

**Table 3-5. 39 Tone Mode (Program Mode Selections)**

Option	Setting	Remotely Controllable	Paragraph
04	Chan A only B only Diversity	X	3.9.9
05	Duplex Half Full	X	3.9.10
06	Key Delay 45 ms 340 ms 630 ms 900 ms		3.9.11
07	Clipping Off On		3.9.12
08	Time/F Div Off On		3.9.13
09	Dopplr Track Off On	X	3.9.14
10	Acquire Normal Norm/Enh Enh/Norm Enhanced		3.9.15

**Table 3-6. 39 Tone Mode  
(Program Selections if DTE is Asynchronous)**

Option	Setting	Paragraph
11 DTE Rate	75 150 300 600 1200 2400 Slaved	3.9.16
12 DTE Parity	Off Odd Even	N/A
13 DTE Char Size	5 6 7 8	N/A
14 DTE Stop Bits	1 2	N/A
15 DTE Echo	Off On	3.9.17
16 Async EOM	Off On	3.9.18
17 Flow	CTS Xon/Xoff	3.9.19

### 3.8.3 Robust Serial Mode (Option)

The selectable options are listed in tables 3-7 (manual mode), 3-8 (program mode), and 3-9 (if the data terminal equipment is asynchronous). It is also noted in the tables if an option is remotely controllable.

**Table 3-7. Robust Serial Mode (Manual Mode Selections)**

Option	Setting	Remotely Controllable	Paragraph
01 Interleave	0.0s 1.2s 4.8s 9.6s	X	3.9.20
02 DTE	Asynchronous Synchronous	X	3.9.8

**Table 3-8. Robust Serial Mode (Program Mode Selections)**

Option	Setting	Remotely Controllable	Paragraph
03 Chan	A only B only	X	3.9.9
04 Duplex	Half Full	X	3.9.10
05 Key Delay	45 ms 340 ms 630 ms 900 ms		3.9.11

**Table 3-9. Robust Serial Mode  
(Program Selections if DTE is Asynchronous)**

Option	Setting	Paragraph
06 DTE Rate	75 150 300 600 1200 2400 Slaved	3.9.16
07 DTE Parity	Off Odd Even	N/A
08 DTE Char Size	5 6 7 8	N/A
09 DTE Stop Bits	1 2	N/A
10 DTE Echo	Off On	3.9.17
11 Flow	CTS Xon/Xoff	3.9.19

### 3.8.4 FSK Mode

There are two status lines in the FSK mode: one for Channel A and one for Channel B. The display initially shows the channel A status line; the other can be viewed by pressing the option up arrow. An example of the status lines would be:

FSK Mode Fc 1700 Fs $\pm$ 85	FSK Mode B Fc 2400 Fs $\pm$ 425
---------------------------------	------------------------------------

The numeric keypad may be used to enter data rate and mark and space frequencies. The setting buttons allow half-hertz selection of mark and space frequencies.

The selectable options are listed in tables 3-10 (manual mode) and 3-11 (program mode). It is also noted in the tables if an option is remotely controllable.

### 3.8.5 39 Tone/FSK Mode

The 39 Tone/FSK Mode is a dual mode of operation that provides both 39 Tone and FSK. The settings for 39 Tone appear on Channel A; FSK is always on Channel B.

A typical status display setting when the MODE pushbutton is used to enter this dual mode is:

39 Tone/FSK Mode 2400 V      Short      Sync
---

By pressing the OPTIONS up arrow pushbutton, the second status display might be:

39 Tone/FSK Mode B Fc 2400 Fs $\pm$ 425
--

All operating parameters are selected in the same way as in the single mode of operation.

The selectable options are listed in tables 3-12 (manual mode), 3-13 (program mode), and 3-14 if the data terminal equipment is asynchronous. It is also noted in the tables if the option is remotely controllable.

Table 3-10. FSK Mode (Manual Mode Selections)

Option	Setting	Remotely Controllable	Paragraph
Channel A:			
A01 Rx Rate	45 to 1200 bps (steps of 1 bps)	X	3.9.21
A02 Tx Mark Tx Cent	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.22
A03 Tx Space Tx Shift	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.23
A04 Rx Mark Rx Cent	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.24
A05 Rx Space Rx Shift	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.25
Channel B:			
B01 Rx Rate	45 to 1200 bps (steps of 1 bps)	X	3.9.21
B02 Tx Mark Tx Cent	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.22
B03 Tx Space Tx Shift	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.23
B04 Rx Mark Rx Cent	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.24
B05 Rx Space Rx Shift	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.25

Table 3-11. FSK Mode (Program Mode Selections)

Option	Setting	Remotely Controllable	Paragraph
Channel A:			
A06 Chan	Independent Diversity	X	3.9.26
A07 Tx Rate	45 to 1200 bps (steps of 1 bps)	X	3.9.27
A08 Thresh Track	Off On	X	3.9.28

Table 3-11. FSK Mode (Program Mode Selections) (Cont.)

Option	Setting	Remotely Controllable	Paragraph
Channel A (Cont.):			
A09	Mod Out	Off On Switched	X  3.9.29
A10	Polarity	Tx- Rx- Tx- Rx + Tx + Rx- Tx + Rx +	X  3.9.30
A11	Mark Hold	Off On Auto	X  3.9.31
A12	Tune	Cent/Shift Mark/Space	3.9.32
A13	Track Tune	Off On	3.9.33
A14	Mod AB Sum	Off On	3.9.34
A15	DTE Rx Clock	A B	3.9.35
Channel B:			
B06	Tx Rate	45 to 1200 bps (steps of 1 Hz)	X 3.9.27
B07	Thresh Track	Off On	X 3.9.28
B08	Mod Out	Off On Switched	3.9.29
B09	Polarity	Tx- Rx- Tx- Rx + Tx + Rx- Tx + Rx +	X 3.9.30
B10	Mark Hold	Off On Auto	X 3.9.31
B11	Analog In	A B	3.9.36

Table 3-12. 39 Tone/FSK Mode (Manual Mode Selections)

Option	Setting	Remotely Controllable	Paragraph
A01 Rate	75 bps 150 bps 300 bps 600 bps 1200 bps 2400 bps 2400 voice	X	3.9.37
A02 Interleave	Short Long Alt S Alt L	X	3.9.7
A03 DTE	Asynchronous Synchronous	X	3.9.8
FSK Channel B selections:			
B01 Rx Rate	45 to 1200 bps (steps of 1 bps)	X	3.9.21
B02 Tx Mark Tx Cent	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.22
B03 Tx Space Tx Shift	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.23
B04 Rx Mark Rx Cent	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.24
B05 Rx Space Rx Shift	0 to 3400.0 (steps of 0.5 Hz)	X	3.9.25

Table 3-13. 39 Tone/FSK Mode (Program Mode Selections)

Option	Setting	Remotely Controllable	Paragraph
A04 Duplex	Half Full	X	3.9.10
A05 Key Delay	45 ms 340 ms 630 ms 900 ms		3.9.11

**Table 3-13. 39 Tone/FSK Mode (Program Mode Selections) (Cont.)**

Option	Setting	Remotely Controllable	Paragraph
A06 Clipping	Off On		3.9.12
A07 Time/F Div	Off On		3.9.13
A08 Dopplr Track	Off On	X	3.9.14
A09 Acquire	Normal Norm/Enh Enh/Norm Enhanced		3.9.15
FSK Channel B Selections:			
B06 Tx Rate	45 to 1200 bps (steps of 1 bps)	X	3.9.27
B07 Thresh Track	Off On	X	3.9.28
B08 Mod Out	Off On Switched	X	3.9.29
B09 Polarity	Tx- Rx- Tx- Rx+ Tx+ Rx- Tx+ Rx+	X	3.9.30
B10 Mark Hold	Off On Auto	X	3.9.31

**Table 3-14. 39 Tone/FSK Mode (Program Selections if DTE is Asynchronous)**

Option	Setting	Paragraph
A10 DTE Rate	75 150 300 600 1200 2400 Slaved	3.9.16
A11 DTE Parity	Off Odd Even	N/A

**Table 3-14. 39 Tone/FSK Mode (Program Selections if DTE is Asynchronous) (Cont.)**

Option	Setting	Paragraph
A12	DTE Char Size 5 6 7 8	N/A
A13	DTE Stop Bits 1 2	N/A
A14	DTE Echo Off On	3.9.17
A15	Async EOM Off On	3.9.18
A16	Flow CTS Xon/Xoff	3.9.19

**3.8.6 Robust Serial/FSK Mode**

The Robust Serial/FSK Mode is a dual mode of operation that provides both Robust Serial and FSK. The settings for Robust Serial appear on Channel A; FSK is always on Channel B.

A typical status display setting when the MODE pushbutton is used to enter this dual mode is:

Rob Ser/FSK Mode 75 bps Inter 1.2s
---------------------------------------

By pressing the OPTIONS pushbutton, the second status display might be:

Rob Ser/FSK Mode B Fc 2400 Fs ± 425
--

All operating parameters are selected in the same way as in the single mode of operation.

The selectable options are listed in tables 3-15 (manual mode), 3- 16 (program mode), and 3-17 if the data terminal equipment is asynchronous. It is also noted in the tables if the option is remotely controllable.

**Table 3-15. Robust Serial/FSK Mode (Manual Mode Selections)**

Option	Setting	Remotely Controllable	Remotely Controllable
A01	Interleave 0.0s 1.2s 4.8s 9.6s	X	3.9.20
A02	DTE Asynchronous Synchronous	X	3.9.8

**Table 3-15. Robust Serial/FSK Mode (Manual Mode Selections) (Cont.)**

Option	Setting	Remotely Controllable	Paragraph
FSK Channel B Selections:			
B01 Rx Rate	45 to 1200 bps (steps of 1 bps)	X	3.9.21
B02 Tx Mark Tx Cent	0 to 3400.0 (steps 0.5 Hz)	X	3.9.22
B03 Tx Space Tx Shift	0 to 3400.0 (steps 0.5 Hz)	X	3.9.23
B04 Rx Mark Rx Cent	0 to 3400.0 (steps 0.5 Hz)	X	3.9.24
B05 Rx Space Rx Shift	0 to 3400.0 (steps 0.5 Hz)	X	3.9.25

**Table 3-16. Robust Serial/FSK Mode (Program Mode Selections)**

Option	Setting	Remotely Controllable	Paragraph
A03 Duplex	Half Full	X	3.9.10
A04 Key Delay	45 ms 340 ms 630 ms 900 ms		3.9.11
FSK Channel B Selections:			
B06 Tx Rate	45 to 1200 bps (steps of 1 bps)	X	3.9.27
B07 Thresh Track	Off On	X	3.9.28
B08 Mod Out	Off On Switched	X	3.9.29

**Table 3-16. Robust Serial/FSK Mode (Program Mode Selections) (Cont.)**

Option	Setting	Remotely Controllable	Paragraph
FSK Channel B Selections (Cont.):			
B09	Polarity Tx- Rx- Tx- Rx + Tx + Rx- Tx + Rx +	X	3.9.30
B10	Mark Hold Off On Auto	X	3.9.31

**Table 3-17. Robust Serial/FSK Mode (Program Selections if DTE is Asynchronous)**

Option	Setting	Paragraph
A05	DTE Rate 75 150 300 600 1200 2400 Slaved	3.9.16
A06	DTE Parity Off Odd Even	N/A
A07	DTE Char Size 5 6 7 8	N/A
A08	DTE Stop Bits 1 2	N/A
A09	DTE Echo Off On	3.9.17
A10	Flow CTS Xon/Xoff	3.9.19

### 3.9 PARAMETER DESCRIPTIONS

This section describes in detail all OPTION and SETTINGS parameters available in the various operating modes.

#### 3.9.1 Remote Identification

The modem's remote control identification code is set from the Main Set Up Mode. The identification code is selected between 1 and 255.

#### 3.9.2 Remote Rate

The modem will interface with a Harris remote control unit at baud rates from 75 to 9600 bits per second.

#### 3.9.3 Power Up Bit

The Main Set Up Mode allows the user the option of disabling the power-up BIT that normally runs when power is applied or when the master reset is pressed. This should be left in the ON position to activate the built-in test feature of the RF-3466A.

#### 3.9.4 Halt On Fault

When this feature is set to ON, and a fault occurs, a fault message will be displayed on both lines of the display. The first line will be overwritten after one second with the message "Hit any key to go on". During this time the modem is inactive and will not respond to DTE or remote control signals. This ensures that the operator will see the error message. When any front panel button is pressed the modem will be reinitialized with all LEDs off, and return to the standard display.

In some tactical situations this feature may be undesirable. In that case the MAIN SETUP MODE can be used to disable it. When it is set to OFF, and a fault occurs, the fault message will be displayed for three seconds. After that the modem will be reinitialized and return to the standard display. The FAULT LED will be illuminated to alert the operator that a fault has been detected.

#### 3.9.5 Loopback

When set to ON, a continuous analog loopback test is run after the power up BIT is finished. This can be used as a troubleshooting aid. For normal operation Loopback should be set to OFF. To run the test, both Power Up BIT and Loopback must be set to ON. Turning the modem power off and back on will then cause both tests to run. To stop the loopback test set Loopback to OFF, then turn the modem power off and back on.

#### 3.9.6 Clock

There are three choices available to set up the master oscillator for the modem. When set to Internal, the modem generates the 10.1376 MHz master clock via an internal free-running phase-locked loop circuit. When set to Ext DTE, the master clock is slaved to a transmit clock which must be provided by the data terminal equipment (DTE). The third option is Ext 1 MHz. In order to use this option S2-1 on the A8 Digital I/O assembly must be set to open, and an external 1 MHz frequency reference must be connected to J2 on the rear panel. An error condition will occur if Ext 1 MHz is selected when there is no external standard provided. S2-1 acts as a form of interlock to help prevent this fault condition from occurring.

### 3.9.7 39 Tone Mode Interleaving Factor

Time interleaving of the outgoing data is used to reduce bit errors caused by burst conditions on the radio channel. While not affecting the data rate, interleaving does introduce a time delay.

The interleaving factor is used to define the degree of interleaving. As the factor increases, the degree of interleaving becomes greater, time delay becomes longer, and the protection against burst errors increases. Some systems impose timing constraints because of end-to-end delay requirements such as digital voice transmissions. These constraints limit the interleaving delay to a specific maximum.

Multiple interleaving delays are provided for each data rate. This provides the best possible burst protection and, at the same time, satisfies the different timing constraints for the various systems.

There are four interleaving factors available: Short, Long, Alternate Short, and Alternate Long.

Tables 3-18 and 3-19 show the modem startup delay and modem throughput delay as a function of the data mode setting, interleaving factor (short/long), and whether Time/Frequency Diversity is enabled (paragraph 3.7.23). Note that SHORT implies no interleaving at all, for all rates except 2400 bps. (A no interleaving mode for 2400 is also available in the voice position, SHORT.)

The modem startup delay is defined as the elapsed time between the application of the RTS and CTS signals. The throughput delay is defined as the length of time expended between data entrance at the transmitting modem and the same data exiting from the receiving modem.

**Table 3-18. Modem Startup and Throughput Delays (Short or Long Mode) in Seconds  
(Delays Assume a Keyline Delay Setting of 45 ms)**

Data Mode	Short Interleaving			Long Interleaving		
	Startup**		Throughput	Startup**		Throughput
	Norm	Enh		Norm	Enh	
Voice	.450	N/A	.367	.315	N/A	.637
2400 Sync	.0225	.0225	5.07	.0225	.0225	9.88
2400 Async	.450	2.12	.341	.0225	.0225	10.13
1200	.450	2.12	.416	.0225	.0225	12.60
600	.450	2.12	.558	.0225	.0225	12.94
600*	.450	2.12	.738	.0225	.0225	13.12
300	.428	2.09	.821	.0225	.0225	13.39
300*	.428	2.09	1.09	.0225	.0225	13.66
150	.383	2.05	1.37	.0225	.0225	14.15
150*	.383	2.05	1.69	.0225	.0225	14.47
75	.293	1.96	2.42	.0225	.0225	13.49
75*	.293	1.96	2.76	.0225	.0225	13.83

\*Time/Frequency Diversity Enabled

\*\*Norm and Enh refer to acquisition mode (See paragraph 3.9.15)

**Table 3-19. Modem Startup and Throughput Delays (ALTERNATE Short or Long Mode) in Seconds  
(Delays Assume a Keyline Delay Setting of 45 ms)**

Data Mode	Short Interleaving			Long Interleaving		
	Startup**		Throughput	Startup**		Throughput
	Norm	Enh		Norm	Enh	
Voice	.160	N/A	0.974	.0225	N/A	1.29
2400	.0225	1.58	1.58	.0225	.945	2.75
1200	.0225	1.49	1.71	.0225	.225	4.24
600	.0225	1.46	2.0	.0225	.135	4.6
600*	.0225	1.46	2.13	.0225	.135	4.77
300	.0225	1.51	2.32	.0225	.315	4.65
300*	.0225	1.51	2.58	.0225	.315	4.92
150	.0225	1.40	3.1	.0225	.113	5.6
150*	.0225	1.40	3.35	.0225	.113	5.90
75	.0225	1.46	4.3	.0225	.360	6.7
75*	.0225	1.46	4.58	.0225	.360	7.01

\*Time/Frequency Diversity Enabled

\*\*Norm and Enh refer to acquisition mode (See paragraph 3.9.15)

### 3.9.8 Synchronous or Asynchronous DTE

When selecting asynchronous operation, set baud rate, parity, character length, number of stop bits, echo/no echo, XON/XOFF (CTS), and EOM. These must be set to match the data terminal's interface parameters.

### 3.9.9 Channel Diversity

The modem can be set for dual channel diversity reception, or it can receive audio independently on channel A or B.

### 3.9.10 Duplex

In the full-duplex mode, the RF-3466A can simultaneously transmit and receive a message. In the half-duplex mode, if the RTS input at the DTE interface is active, the modem will transmit a message but the receive path of the modem will be disabled. When the RTS is removed and the message transmission is completed, then the receive section of the modem will again be enabled and incoming messages will be recognized.

Half-duplex mode is often required if the modem is being used with an HF Transceiver which supplies a "side tone" back to the modem during a transmission (this happens when the modem is interfaced to the transceiver via the audio handset connector of the radio). In this case, the half-duplex mode prevents the modem from "echoing" back this "received" message to the DTE.

### 3.9.11 Key Delay

The modem can control the transmitter keyline function. The modem delays audio output to the transmitter after application of the keyline to allow for the transmitter startup delay. This delay can be set between 45 milliseconds and 900 milliseconds.

### 3.9.12 Clipping

Clipping limits the peak amplitude of the audio signal so the HF radio signal can be maintained at its maximum average power level. Clipping is part of the digital signal process and when on is normally set to achieve a baseband peak-to-average ratio of 10 dB which results in a transmitted PEP/ $P_{rms}$  ratio of 7 dB or less.

### 3.9.13 Time/Frequency Diversity

With data rates of 600, 300, 150, and 75 baud, a choice of signalling formats is available. Time/Frequency diversity will provide a performance advantage over in band frequency diversity for many types of HF channel conditions, although it will add some delay to the overall system throughput (360 ms or less).

### 3.9.14 Doppler Track

Normally the modem automatically corrects for frequency errors introduced by vehicle motion, shifts of ionosphere, or by frequency standard inaccuracies in the radio transmitter and receiver. Doppler track provides continuous correction as part of the demodulation routine. Doppler track can be disabled if frequency errors greater than  $\pm 2$  Hz are not expected.

### 3.9.15 Acquisition

The RF-3466A has an enhanced acquisition feature that, under low signal-to-noise ratio (SNR) conditions, provides improved probability of signal detection and acquisition. This mode can be selected independently for two data rate ranges: 75-300 bps and 600-2400 bps. When enhanced operation is selected, a longer preamble is used which adds delay to the system throughput. The frequency correction range is also reduced from  $\pm 75$  Hz to  $\pm 20$  Hz. The enhanced acquisition mode is particularly desirable in the low data rate range. This mode will permit reliable synchronization at SNRs as low as -3 dB. A performance advantage will be realized for high rate modes as well, although the high rate modes are generally used at SNRs where the normal synchronization is adequate. Voice mode defaults to normal acquisition.

The choices for this option are in the format "low range/high range". The Normal and Enhanced settings mean that both ranges are either normal or enhanced, while Norm/Enh means that the low range is set to normal and the high range is set to enhanced. Similarly, Enh/Norm means that the low range is set to enhanced and the high range is set to normal.

### 3.9.16 DTE Baud Rate

The asynchronous DTE baud rate can be set at 75, 150, 300, 600, 1200, or 2400.

For asynchronous DTEs supporting XON/XOFF handshake, or CTS signalling, the DTE baud rate setting can be equal to or greater than the modem baud rate. For example, if the DTE baud rate is set to 2400 bps, the modem baud rate can be varied from 2400 bps to 75 bps, depending upon HF channel conditions. As long as the DTE responds to XON/XOFF or CTS, the differences in modem and DTE baud rates can be regulated to maintain data integrity. If the DTE cannot respond to XON/XOFF or CTS, then the DTE baud rate must be set to match the modem baud rate. This must occur each time the modem baud rate is changed. A SLAVE mode is available that will eliminate the need for DTE rate manipulation. In the SLAVE mode, the DTE baud rate setting of the modem follows the data rate setting of the modem as the baud rate is changed.

### 3.9.17 DTE Echo/No Echo

The RF-3466A can supply an echo back to the DTE when DTE Echo operation is selected. The data received by the modem on the TX data line is sent back to the DTE via the RX data line when the option is enabled. This

type of echo back is usually referred to as a Host Echo. When echo is selected, the receive side of the modem is disabled.

### 3.9.18 Asynchronous EOM

When the modem is used with an asynchronous DTE and EOM is enabled, the sending modem will insert a string of 10 EOM characters in the outgoing data stream at the end of a message. This happens when RTS is removed by the sending DTE. The receiving modem uses the incoming EOM characters to detect the end-of-message. When this occurs, the modem mutes the RX data stream to the receiving DTE. This may be an undesirable feature to some DTEs. For instance, DTEs utilizing an ARQ-type half-duplex protocol will normally send their own turn-around character. In this case, the modem's EOM characters are not needed and only serve to delay the link turn-around time.

### 3.9.19 Flow

In asynchronous mode, with a DTE character length of 7 or 8 bits selected, a choice is available to regulate data transfer between the RF-3466A and DTE. When set to CTS, the Clear-To-Send signal at the DTE interface is removed and reissued to regulate data transfer from the sending DTE. When set to XON/XOFF, control characters are inserted into the data stream to regulate data transfer from the sending DTE. Note that some data terminals support XON/XOFF while others only support CTS. Check the data terminal before setting this option.

### 3.9.20 Interleaving Factor (Robust Serial Option)

Time interleaving of the outgoing data is used to reduce bit errors caused by burst conditions on the radio channel. While not affecting the data rate, interleaving does introduce a time delay.

The interleaving factor is used to define the degree of interleaving. As the factor increases, the degree of interleaving becomes greater, time delay becomes longer, and the protection against burst errors increases. Some systems impose timing constraints because of end-to-end delay requirements. The constraints limit the interleaving delay to a specific maximum.

### 3.9.21 FSK Rx Rate

This sets the FSK receive data rate, selectable in 1 bps increments over the range of 45 bps to 1200 bps. Because the FSK modem is asynchronous, the modem will function as long as the Rx rate is set higher than the actual channel rate; however for optimum performance it should be set equal to the channel rate.

### 3.9.22 Tx Mark, Tx Center

The FSK frequencies can be specified as either a mark/space frequency pair or as a center frequency and shift. The choice is made using the TUNE option, available in the FSK Program mode. When the Tx Mark/Cent option is selected the RF-3466A display will show either Tx Mark or Tx Cent depending on the TUNE setting. The Tx Mark or Tx Center frequency can then be altered using either the numeric keypad or the SETTING buttons.

If the frequencies are specified as a center frequency and shift, it is important to note that the sum of the center frequency plus the shift frequency must be less than 3400. Similarly, the center frequency minus the shift frequency must be greater than 0. If these limits are exceeded, even temporarily while a change is being made, the values will automatically be adjusted to fit within the limits.

### 3.9.23 Tx Space, Tx Shift

The FSK frequencies can be specified as either a mark/space frequency pair or as a center frequency and shift. The choice is made using the TUNE option, available in the FSK Program mode. When the Tx Space/Shift option is selected, the RF-3466A display will show either Tx Space or Tx Shift, depending on the TUNE setting. The Tx Space or Tx Shift frequency can then be altered using either the numeric keypad or the SETTING buttons.

If the frequencies are specified as a center frequency and shift, it is important to note that the sum of the center frequency plus the shift frequency must be less than 3400. Similarly, the center frequency minus the shift frequency must be greater than 0. If these limits are exceeded, even temporarily while a change is being made, the values will automatically be adjusted to fit within the limits.

### 3.9.24 Rx Mark, Rx Center

The FSK frequencies can be specified as either a mark/space frequency pair or as a center frequency and shift. The choice is made using the TUNE option, available in the FSK Program mode. When the Rx Mark/Cent option is selected, the RF-3466A display will show either Rx Mark or Rx Cent, depending on the TUNE setting. The Rx Mark or Rx Center frequency can then be altered using either the numeric keypad or the SETTING buttons.

If the frequencies are specified as a center frequency and shift, it is important to note that the sum of the center frequency plus the shift frequency must be less than 3400. Similarly, the center frequency minus the shift frequency must be greater than 0. If these limits are exceeded, even temporarily while a change is being made, the values will automatically be adjusted to fit within the limits.

### 3.9.25 Rx Space, Rx Shift

The FSK frequencies can be specified as either a mark/space frequency pair or as a center frequency and shift. The choice is made using the TUNE option, available in the FSK Program mode. When the Rx Space/Shift option is selected, the RF-3466A display will show either Rx Space or Rx Shift, depending on the TUNE setting. The Rx Space or Rx Shift frequency can then be altered using either the numeric keypad or the SETTING buttons.

If the frequencies are specified as a center frequency and shift, it is important to note that the sum of the center frequency plus the shift frequency must be less than 3400. Similarly, the center frequency minus the shift frequency must be greater than 0. If these limits are exceeded, even temporarily while a change is being made, the values will automatically be adjusted to fit within the limits.

### 3.9.26 FSK Channel

When set to INDEPENDENT, the channel A and channel B FSK signals operate as two separate independent modems. When set to DIVERSITY, the two receive channels are combined using an equal gain diversity technique for improved bit error rate performance.

### 3.9.27 FSK Tx Rate

This sets the Tx clock rate, and is selectable in 1 bps increments over the range of 45 bps to 1200 bps. Note that this has no effect on the speed at which normal asynchronous data can be sent.

### 3.9.28 Threshold Tracking

When set to ON, the threshold tracker attempts to track the center of the received FSK signal to optimize the data output under conditions of selective fades as encountered on HF channels. Threshold tracking works best at data rates of 600 bps and below and should be set to OFF for higher rates. It should also be set to OFF for Gaussian channels such as telephone networks.

### 3.9.29 Modulator Output

When set to OFF, the FSK modulator output is disabled and no audio will be present at the radio interface. When set to ON, the modulator will always produce an output. If no data is being sent, then a constant mark signal will be present at the radio interface. When set to SWITCHED, the transmit audio will only be present when data is being sent, one second after assertion of the RTS signal.

### 3.9.30 Polarity

This feature controls the polarity of the FSK transmit and receive data. Settings are available as follows:

Setting	Meaning
Tx- Rx-	Both transmit and receive data are inverted
Tx- Rx +	Transmit data is inverted, receive data is non-inverted
Tx + Rx-	Receive data is inverted, transmit data is non-inverted
Tx + Rx +	Both transmit and receive data are non-inverted

### 3.9.31 Mark Hold

When set to ON, the demodulator output will be a constant mark signal. When set to AUTO, the demodulator output will be set to a mark signal when the received signal level drops below a preset threshold. When set to OFF, the demodulator will operate continuously. In that case corrupted data may be presented to the data terminal under poor channel conditions.

### 3.9.32 Tune

When set to CENT/SHIFT, the FSK frequencies can be entered as a center frequency and shift. When set to MARK/SPACE, the FSK frequencies can be entered as a mark frequency and a space frequency.

### 3.9.33 Track Tune

When set to OFF, all FSK frequencies for both channels can be set and changed independent of each other. However, this means that if the operator wants to change both the transmit and receive frequencies it will require two operations.

When Track Tune is set to ON, any changes made to the channel A transmit frequencies will also occur on the channel A receive, channel B transmit, and channel B receive frequencies. In this case, if the operator wants to change both the transmit and receive frequencies it only requires one operation. Note that these frequencies will be changed to the same values as the channel A transmit settings. After setting the channel A transmit frequency, the others can be changed independently if desired.

### 3.9.34 Mod AB Sum

When set to ON, the channel A and channel B modulator outputs are mixed together and output on audio channel A. The combined signal has an output level equal to that of a single modulator output. Setting this parameter to OFF keeps the FSK channels separate.

### 3.9.35 DTE Rx Clock

The modem can provide a recovered receive clock to one of the FSK data terminal interface ports. The DTE Rx Clock option allows the user to assign the receive clock to either of the two ports. Setting it to A routes the clock recovered from FSK channel A data to the data terminal associated with FSK channel A. Setting it to B routes the clock recovered from FSK channel B data to the data terminal associated with FSK channel B.

### 3.9.36 B Analog In

When using channel B of the FSK mode, the source of the receive audio can be selected. When this option is set to B, the receive audio associated with FSK channel B will be demodulated. When it is set to A, the channel B demodulator will be demodulating the receive audio associated with FSK channel A.

### 3.9.37 39 Tone Modem Rate

The modem supports baud rates of 75, 150, 300, 600, 1200, and 2400 bps. When the modem is used with synchronous DTE equipment, the modem baud rate must match the baud rate of the DTE.

#### NOTE

When the modem is used with asynchronous DTE equipment, it is possible to operate the modem at a lower baud rate than the DTE (although this places certain requirements on the DTE for handshake characteristics, as discussed in section 1.5).

Voice mode is used when the modem's data terminal equipment is a voice digitizer. In voice operation, a baud rate of 2400 bps is established. In voice mode, the interleaving delay inserted by the Error Correction process of the modem is much shorter than that used for the 2400 bps data mode, resulting in less end-to-end delay for voice transmission. Voice mode supports both half and full-duplex operation. Note that selection of voice mode forces the modem to be in the synchronous state, regardless of front panel setting.

## SECTION 4

### THEORY OF OPERATION

#### 4.1 INTRODUCTION

This sections describes the RF-3466A Universal HF Modem theory of operation for its two primary modes of operation: 39-tone and FSK. This is followed by descriptions of the major assemblies.

The RF-3466A Universal HF Modem has been designed to overcome the problems which limit the rates at which data may be passed over an HF radio link. Typically, HF radio data links have been confined to low data rates and are subject to high error rates. The RF-3466A overcomes the problems presented by fading, multipath propagation, and interference on HF channels.

Figure 4-1 is a simplified block diagram of the RF-3466A.

#### 4.2 39-TONE THEORY OF OPERATION

The microprocessor-based architecture of the RF-3466A combines phase shift keying with digital signal processing, FEC data interleaving, channel diversity, and inband diversity, to achieve high data rates and minimize errors.

Figure 4-2 illustrates the modulation and demodulation functions. Modulation begins with the reception of a serial data stream from the DTE. The DTE can be a teletypewriter, voice digitizer, facsimile unit, or any other device compatible with an EIA RS-232 or MIL-188 interface format.

FEC codes are calculated and added to the incoming data stream. The data and FEC bits are organized in a matrix. The matrix configuration allows adjacent groups of data bits to be redistributed in time to reduce burst errors. This process, called interleaving, is described in more detail in paragraph 4.2.5.

The actual modulation is performed by high speed microprocessors. The digital signal processing produces a string of 12-bit words that are converted to an audible signal. The audio signal is transmitted to the receive site and demodulated.

Demodulation recovers the transmitted data from the received audio signal. Like modulation, the actual demodulation is a digital process. The received audio signal is sampled at a rate of 7200 cycles-per-second to generate a string of 12-bit words that digitally represent the audio signal. The digital signal processing includes frequency correction calculations and the actual demodulation. A major portion of the demodulation is a lengthy, continuous calculation called a fast Fourier transform. This calculation recovers phase shift information that yields the received data. The interleaving matrix created during the modulation process is reconstructed to put the data bits in their original order. The FEC code is evaluated and data errors are corrected before the data is sent to the receiving DTE in a serial stream.

##### 4.2.1 Modulation

The modulation method employed in the RF-3466A is a type of Phase-Shift-Keying (PSK). Basically, PSK shifts a sinusoidal wave in time to represent a binary data bit. The shift is measured in degrees. The form of PSK used in the RF-3466A is called Time Differential Quaternary Phase Shift Keying (TDQPSK). With this form of PSK, an individual wave can be shifted by 45°, 135°, 225°, or 315°. With four possibilities, each phase shift can be used to represent one of four unique two-bit combinations, as listed below:

Phase Shift	Data
45°	10
135°	00
225°	01
315°	11

The phase shift of a tone must be measured against some reference. In the modem, the phases of individual tones are changed at regular intervals. The time segments between phase changes are called frames. The phase shift of a signal in a frame is measured against the position of the signal in the previous frame. Thus the shift becomes time differential. The fundamentals of TDQPSK are illustrated in figure 4-3.

The modulated signals in the RF-3466A are audible tones. The modem generates, modulates, and broadcasts 39 tones simultaneously. The 39 tones are all whole-integer harmonics of the 56.25 Hz fundamental. This separates the tones enough to minimize interference while limiting the total bandwidth to 3 kHz. The 39 tones are listed in table 4-1. An unmodulated tone at 393.75 Hz is generated and broadcast by the modem to be used for frequency correction (see paragraph 4.2.3).

QPSK allows each tone to carry two data bits. 78 data bits can be included in each frame. With a frame length of 22.5 milliseconds, the modem achieves a baud rate of 3466 bits-per-second. FEC reduces the effective data rate to 2400 bits-per-second.

Tone generation, phase modulation, and signal mixing are done digitally. The digital signal processes are based on an algorithm called the inverse fast Fourier transform. A digital-to-analog conversion is used to generate the composite audio signal.

#### 4.2.2 Demodulation

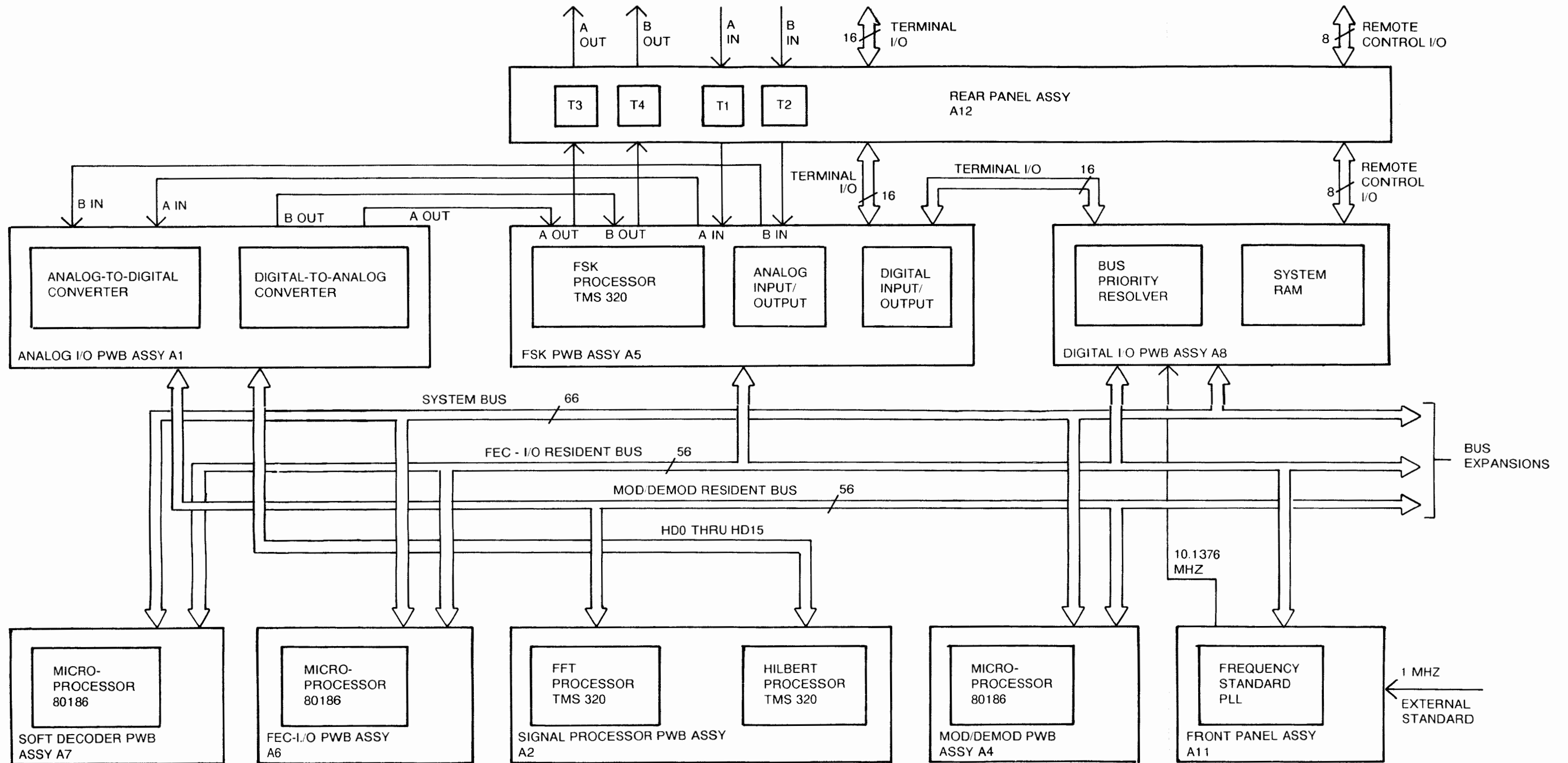
Demodulation is the process of recovering data from the received audio signal. This is done digitally in the RF-3466A. The actual demodulation is preceded by a frequency correction routine to eliminate any error introduced during transmission. An algorithm based on the fast Fourier transform is used to separate the 39 tones and determine their phase shifts.

The fast Fourier transform is a mathematical tool used in digital signal processing to convert a variable of time into a variable of frequency spectrum including the 39 tones listed in table 4-1. The relative phase of each tone is expressed as the position of a vector on a coordinate system, where the axes are I and Q. The modulation process uses four-phase shifts, each separated by 90°. The demodulation process only needs to determine which quadrant the phase shift vector is in to retrieve the data, as illustrated in figure 4-4. Confidence values are computed for each bit and are a function of amplitude and angle. For fixed amplitude, the "I" data bit confidence value reaches its maximum for vector positions of 90° and 270° (see figure 4-3), while the "Q" data bit confidence value reaches its minimum. At 0° and 180° the roles of the "I" bit and "Q" bit are reversed. The confidence values are used in the FEC soft-decision decoding process.

The retrieved data is interleaved to reposition the bits in their original order and run through an FEC routine before being sent to the receiving DTE.

#### 4.2.3 Frequency and Frame Synchronization

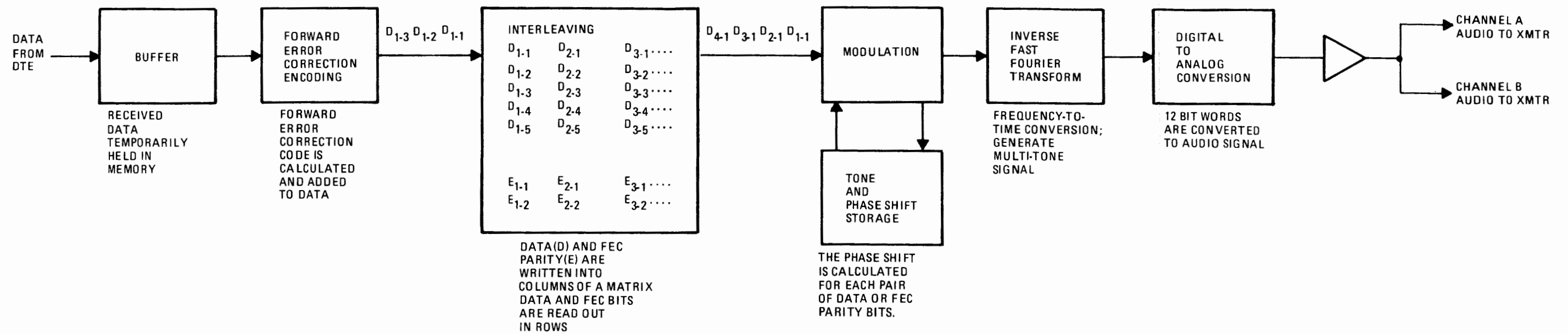
A two-part preamble is used to synchronize the sending and receiving units at the beginning of each transmission. The first part of the preamble is used by the receiving unit to correct for frequency errors. Frequency errors can be introduced by vehicle motion, shifts of the ionosphere, or by the radio equipment. Because the modulated tones are only 56.25 Hz apart, frequency shifts can cause data errors. Part two of the preamble establishes frame synchronization.



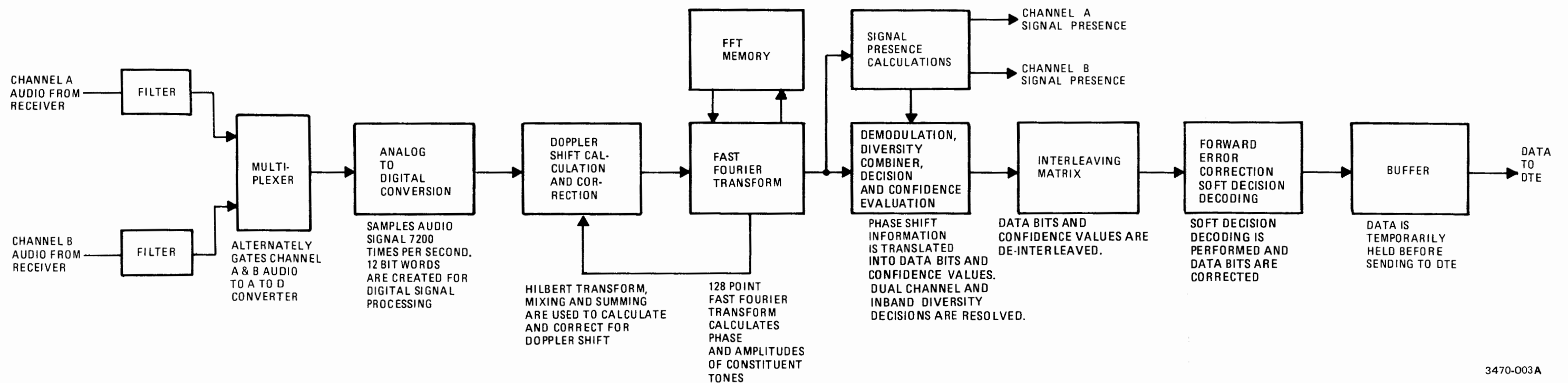
3466A-004

Figure 4-1. RF-3466A Simplified Block Diagram

**MODULATION**

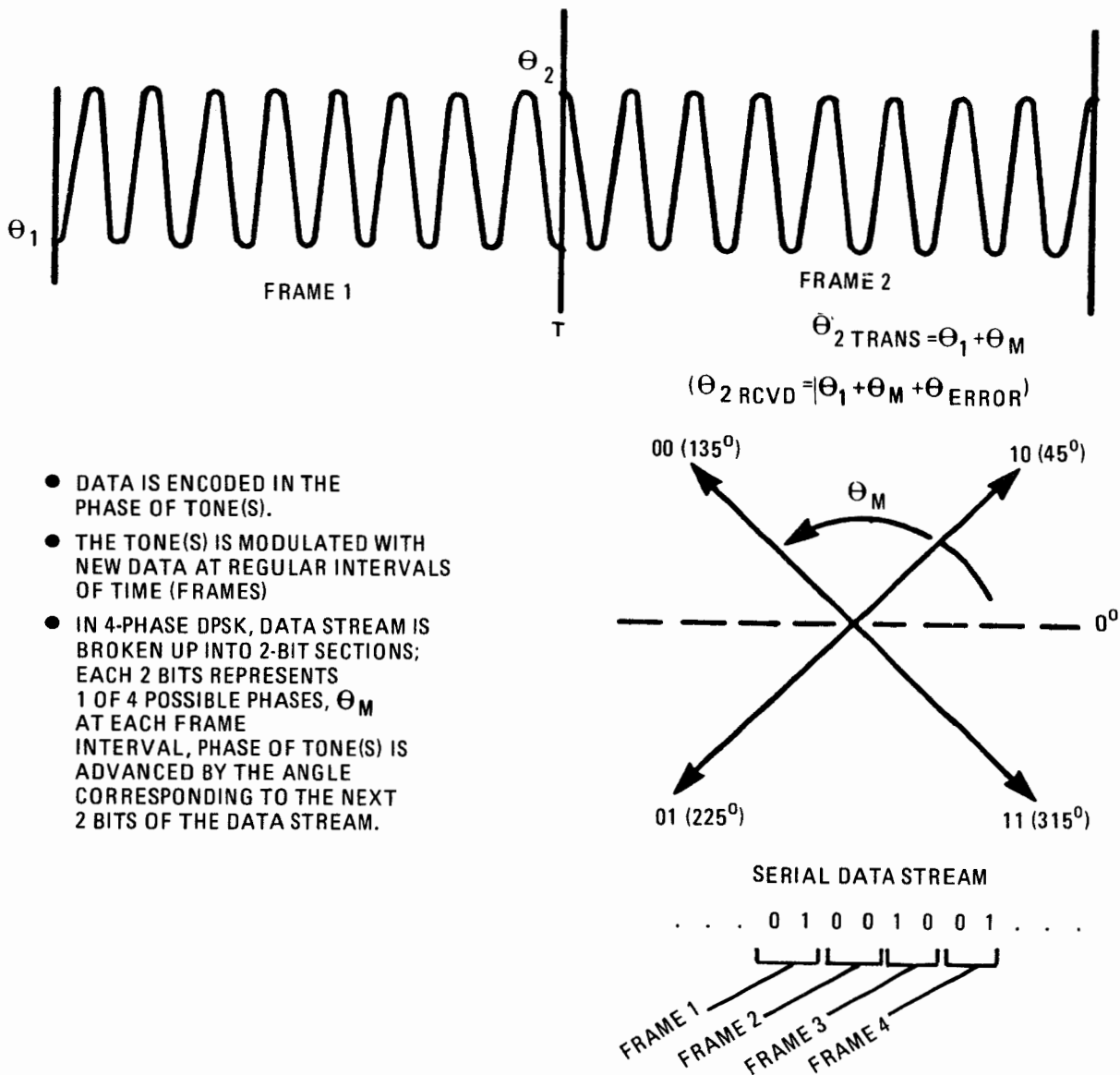


**DEMODULATION**



3470-003A

Figure 4-2. 39-Tone Modulation and Demodulation Functions



HSM-013

Figure 4-3. TDQPSK Fundamentals

Table 4-1. 39-Tone Library

Tone	Harmonics	Frequency (Hz)
0	7	393.75
1	12	675.00
2	13	731.25
3	14	787.50
4	15	843.75
5	16	900.00
6	17	956.25
7	18	1012.50
8	19	1068.75
9	20	1125.00
10	21	1181.25
11	22	1237.50
12	23	1293.75
13	24	1350.00
14	25	1406.25
15	26	1462.50
16	27	1518.75
17	28	1575.00
18	29	1631.25
19	30	1687.50
20	31	1743.75
21	32	1800.00
22	33	1856.25
23	34	1912.50
24	35	1968.75
25	36	2025.00
26	37	2081.25
27	38	2137.50

Table 4-1. 39-Tone Library (Cont.)

Tone	Harmonics	Frequency (Hz)
28	39	2193.75
29	40	2250.00
30	41	2306.25
31	42	2362.50
32	43	2418.75
33	44	2475.00
34	45	2531.25
35	46	2587.50
36	47	2643.75
37	48	2700.00
38	49	2756.25
39	50	2812.50

The part one preamble is characterized by the presence of four unmodulated tones at 787.5, 1462.5, 2137.5, and 2812.5 Hz. This part of the preamble lasts for the equivalent of 14 frames or 315 milliseconds. Upon recognizing this pattern, the receiving unit initiates an algorithm that can correct for frequency errors up to 75 Hz. The frequency correction is done digitally and is illustrated in figure 4-5.

The principle behind the correction can be demonstrated mathematically for a single received tone  $S(t)$ . The received signal can be expressed as:

$$S(t) = \text{COS}(\omega_S + \omega_E)t$$

where  $\omega_S$  is the signal frequency and  $\omega_E$  is the error frequency.

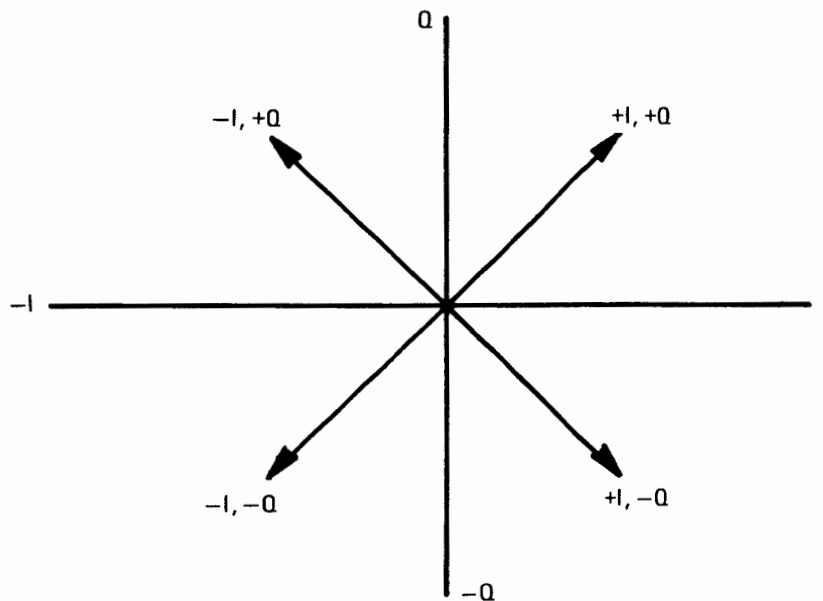
The Hilbert transform is a digital signal processing algorithm that produces a  $-90^\circ$  phase shift of the received signal. The shifted signal  $S(t)$  can be expressed as:

$$S(t) = \text{SIN}(\omega_S + \omega_E)t$$

By mixing  $S(t)$  with  $\text{COS}(-\omega_E t)$  and  $S(t)$  with  $\text{SIN}(-\omega_E t)$ , and combining the results, the error is eliminated to yield the corrected signal  $y(t)$ ; where:

$$y(t) = [S(t) \text{COS}(-\omega_E t)] - [S(t) \text{SIN}(\omega_E t)] = \text{COS}(\omega_E t)$$

The same process is performed continuously during the data transmission using the 393.75-Hz doppler tracking tone as a reference. The modem can correct for shifts up to 3 Hz per second.



<u>I</u>	<u>Q</u>	<u>ANGLE</u>	<u>DATA</u>
+	+	45 <sup>0</sup>	1 0
-	+	135 <sup>0</sup>	0 0
-	-	225 <sup>0</sup>	0 1
+	-	315 <sup>0</sup>	1 1

HSM-014

**Figure 4-4. Vector Representation of Phase Shift**

The second part of the preamble establishes the frame boundaries. Part two of the preamble is characterized by the presence of three biphase modulated tones at 1125.0 Hz, 1800 Hz, and 2475.0 Hz. The phase of each tone alternates between two angles. The receiving unit looks for the phase shift and uses this to locate the frame boundary.

The signal at the frame boundaries is unstable due to multipath distortion. The receiving modem splits the received signal into periods based on the frame boundaries. A guard time of 4.7 milliseconds separates the integration time periods of two adjacent frames, as illustrated in figure 4-6. Frequency and phase shift calculations are performed on the signal received during the integration time.

The preamble is followed by a single frame containing all 39 tones. This frame is used by the receiving modem to establish an initial phase reference for each tone.

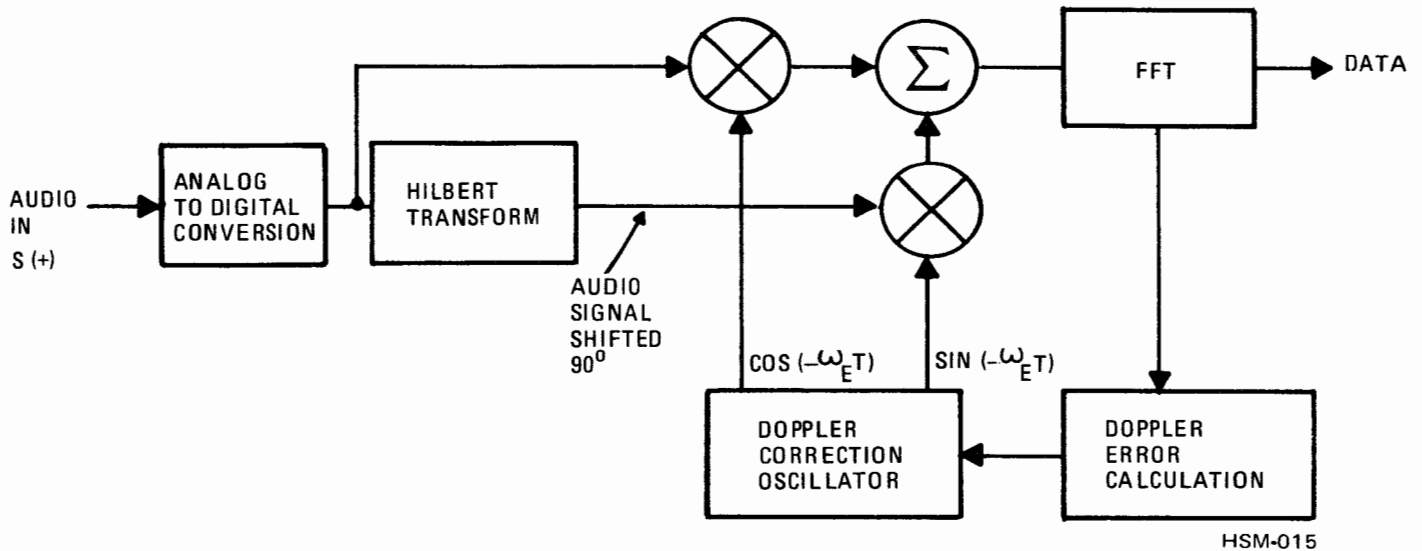


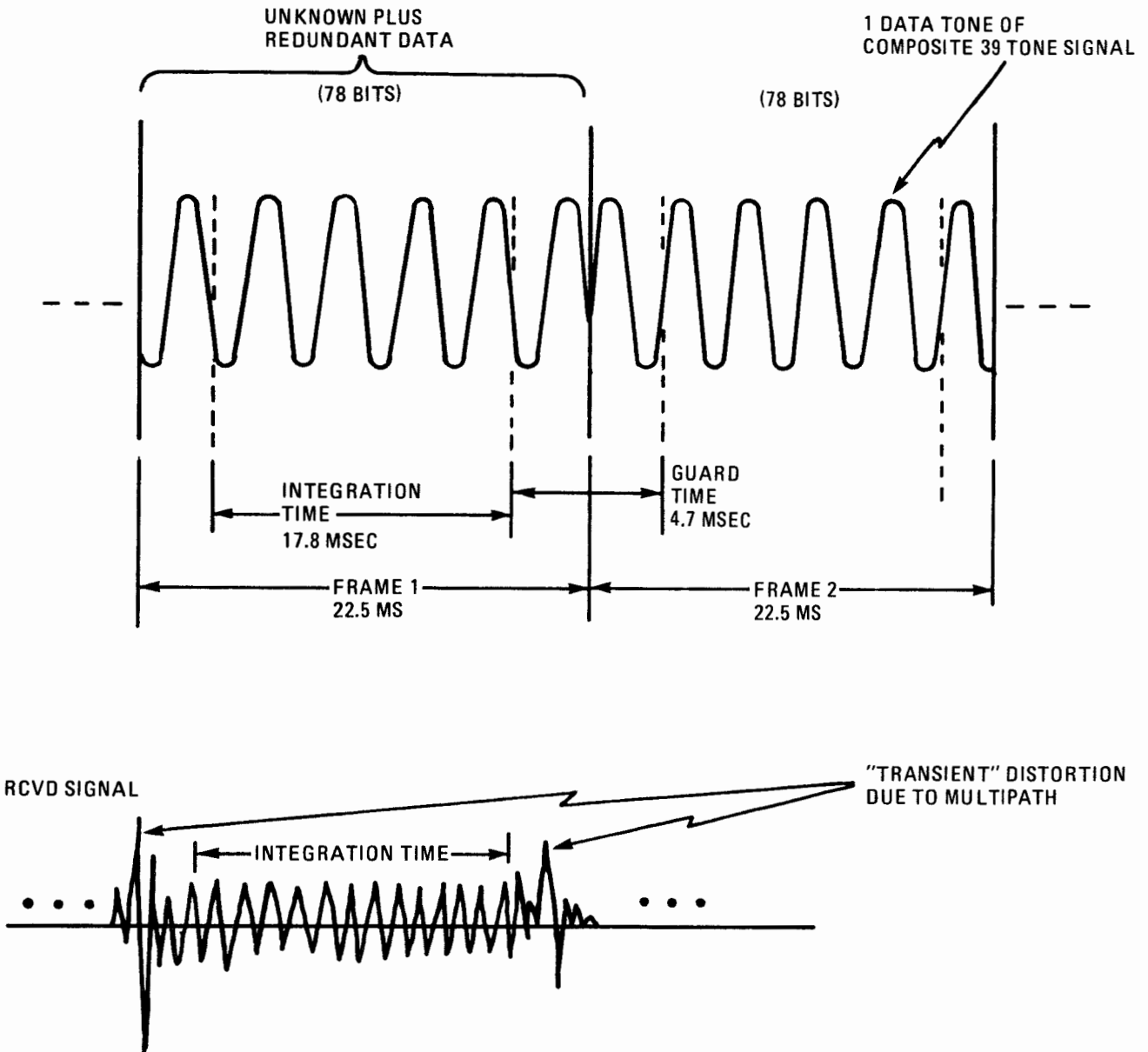
Figure 4-5. Frequency Correction

#### 4.2.3.1 Enhanced Acquisition

To successfully demodulate data, the modem must first recognize a valid signal, and then establish frequency and frame synchronization. The RF-3466A has an enhanced acquisition feature that provides improved probability of signal detection and acquisition when the signal-to-noise ratio is poor. This feature can be selected independently for two data rate ranges: 75-300 bps and 600-2400 bps. Enhanced acquisition extends the modem's synchronization capability by an additional 6 dB. However, this additional performance is realized at the expense of increased startup delay at certain interleaving settings, and reduced frequency reacquisition range.

Enhanced acquisition mode is better understood if it is compared to the normal acquisition mode. The major difference between the two modes is the extended preamble that is required for enhanced acquisition. Table 4-2 shows the differences between the preambles of the two modes.

The startup delay of the modem is extended for certain interleaving settings when in enhanced acquisition mode, as shown in tables 3-18 and 3-19. This is a factor that should be considered in view of various system delay requirements.



HSM-017

Figure 4-6. Frame Boundaries

Table 4-2. Normal/Enhanced Acquisition Preambles

Mode	Preamble Time Duration			
	Phase 1 (doppler)	Phase 2 (sync)	Phase 3 (reference)	Total
Normal	0.315 seconds	0.1800 seconds	0.0225 seconds	0.5175 seconds
Enhanced	1.305 seconds	0.6075 seconds	0.2700 seconds	2.1825 seconds

There are two reasons for the enhanced mode extended preamble. The first is the signal presence detector which, when in enhanced mode, requires more time to process each phase of the preamble prior to declaring it valid. Secondly, the doppler correction and frame boundary detection processes are made more powerful under noisy channel conditions. This, in turn, requires a longer preamble.

In normal synchronization mode, the frequency correction range is  $\pm 75$  Hz. If a preamble is detected, this correction will take place during phase 1 and will require 0.315 seconds. If a preamble is missed entirely, or if synchronization is lost in a long deep fade, the frequency tracker can also correct over the full  $\pm 75$  Hz offset range, although this could require from 10 seconds to two minutes, depending on the actual offset and the particular HF channel conditions.

In enhanced synchronization mode, the modem can correct for frequency offsets in the  $\pm 75$  Hz range, although a longer duration phase 1 preamble (1.305 seconds) is required. If a preamble is missed, or if synchronization is lost in a long deep fade while in enhanced mode, the frequency tracker can only correct for  $\pm 20$  Hz. The reduced tracking/reacquisition range provides for reliable frequency correction at SNRs as low as -3 dB. Therefore, although an offset as large as  $\pm 75$  Hz can be accommodated if a valid preamble is received, the enhanced synchronization frequency correction range has been specified as  $\pm 20$  Hz to reflect the tracking/reacquisition performance. This will place stricter requirements on the frequency accuracy of radio equipment, as specified in table 1-1.

The enhanced mode extends the synchronization range an additional 6 dB over the normal mode, and is recommended to obtain optimum performance at rates of 300 bps and lower.

Although higher data rates are not normally used in poor channel conditions that require enhanced synchronization, the more powerful synchronization would provide fewer missed preambles and false signal declarations, even under marginal link conditions. Thus, enhanced synchronization should be considered for high rate modes as well.

The enhanced mode trades reduced frequency-tracking range and increased startup delay for improved synchronization under poor HF channel conditions. In applications where the enhanced-mode frequency range or throughput delay is not tolerable, the modem should be set for normal acquisition, as described in paragraph 3.9.15.

#### 4.2.4 Forward Error Correction (FEC) Code

FEC involves encoding data at the sending station so the receiving station can correct errors introduced during transmission. The FEC code is derived from, and therefore reflects, the bit pattern in the data stream. Once computed, this code is inserted into the data stream by the sending unit. The receiving unit computes code bits for the received data and compares them to those computed by the sending unit. Differences in the codes calculated at the sending and receiving end of the link are used to locate and correct data errors.

The RF-3466A employs a Reed-Solomon code. To implement this, the data stream is divided into four-bit segments called symbols. At the 2400 bit-per-second rate, the Reed-Solomon (14, 10, 2) code is used. This means that at this data rate the data is organized into code words 14 symbols long. Each code word has ten data symbols and four code symbols. Two symbol errors in each received code word can be corrected.

At data rates of 1200 bits-per-second and below, the Reed-Solomon (7, 3, 2) code is employed. In this version, the code words are seven symbols long, with three data symbols and four code symbols. Two symbol errors in each word can be corrected.

The Reed-Solomon code is a systematic block code. The code words are always the same length and the code symbols follow the data symbols in each word. The code is non-binary with symbols of fixed length to help guard against burst errors.

Using the symbol confidence values computed by the demodulator, the soft-decision decoding is able to correct a greater number of corrupted symbols in a codeword than can be corrected by a hard-decision decoding algorithm. The soft-decision decoder performs three different decodings of each received codeword:

- Hard decoding
- A decoding in which the two symbols with the lowest confidence values are treated as being in error (i.e., "erased").
- A decoding in which the four symbols with the lowest confidence values are treated as being in error (i.e., "erased").

It then selects the decoding most likely to recover the data symbols.

A synchronizing sequence is inserted into the data stream so the receiving unit can detect word boundaries. The DATA SYNC indicator on the front panel is lit when the receiving unit achieves code word synchronization.

#### 4.2.5 Interleaving

Between the encoding and modulation operations, the binary signal undergoes an interleaving process in which adjacent symbols are intermixed and distributed in time in a systematic way. This produces no net change in transmission rate, although it may introduce a substantial delay depending on the interleaving factor. Interleaving enhances the ability of the decoder to correct errors arising from localized channel disturbances such as short fades or lightning activity. Between the demodulation and decoder, a deinterleaving process restores the received data signal to its original order, thereby breaking up error clusters and distributing the damaged symbols over several code words. The power of the decoding process will then be sufficient to correct many of the errors, because the number of errors in each code word is small.

The purpose of interleaving is to break up error clusters in the received data. The principle of operation is as follows:

Imagine that the message "We hold these truths to be self-evident" is to be transmitted. At the modulator, the interleaver begins by loading the message into the columns of matrix, with the result shown in figure 4-7. Subsequently, it reads out the message by rows, with the following result:

W-TTETRO-HU-HETBOSHELES-D--S.

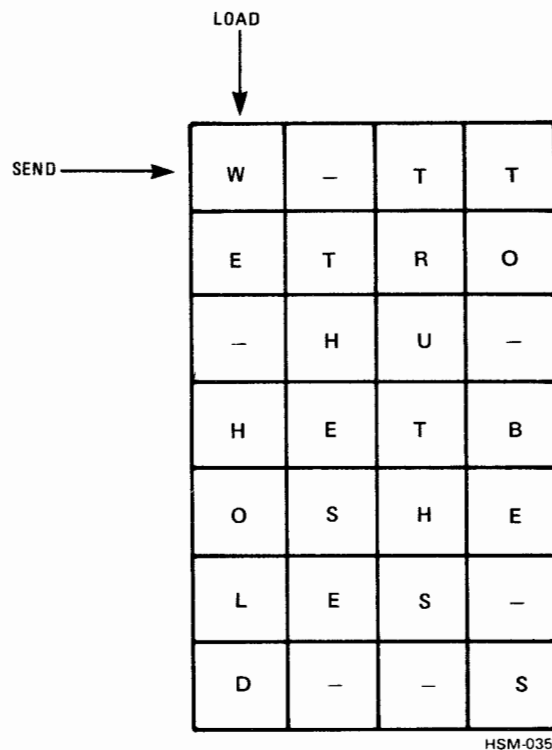


Figure 4-7. Interleaving Matrix

At the demodulator, the process is reversed - the deinterleaver loads by rows, and reads out by columns. The original message will be received correctly if there are no transmission errors. However, there will be a delay in recovering the message, because each matrix has to be filled before the message can be passed on.

Suppose now that a disturbance on the channel wipes out the entire first row of the matrix, producing the following four-character error cluster:

XE-HOLD X TH/ESE-XRUTHS/-XO-BE-S  
(where the errors are indicated by X)

Breaking up the message into groups of ten characters, as in the case of a (14, 10, 2) code, no code word contains more than two errors; all of the above errors can be corrected. Without interleaving, four errors would occur in the first code character, and could not be corrected.

The interleaving factor F is equal to the number of columns in the interleaving matrix (F = 4 in the matrix of figure 4-7). The delay incurred in the interleaving process increases with F, and in the RF-3466A can approach 10 seconds at the maximum value of F. Since delays of this magnitude are seldom acceptable on links operated in a conversational mode, the RF-3466A provides a means for eliminating the interleaving delay by setting F = 1.

#### 4.2.6 Diversity

Diversity in the modem refers to sending and/or receiving data by more than just one path. Channel and inband diversity are used in the RF-3466A. Two audio paths are built into the modem so that the modulated signal can be broadcast on two different carriers to achieve channel diversity. Inband diversity is the process of modulating more than one tone with the same data.

Dual channel diversity at the sending station is provided by two audio outputs, so that identical signals can be routed to two separate transmitters. Separate sidebands of an ISB transmitter can also be used.

Demodulation, when channel diversity is used, involves some special processing. The two received audio signals are multiplexed before the analog-to-digital conversion. The digital signal processing processes the two signals simultaneously. Signal quality calculations are used to accept and reject data from the two channels before performing the diversity combining operation.

For inband diversity, each bit of data is modulated onto two to 16 different tones, depending upon the baud rate. The diversity factors are listed in table 4-3. Two forms of inband diversity are available, frequency and time/frequency diversity. In frequency diversity, the tones which carry the same data are all transmitted within the same symbol interval. In time/frequency diversity, the redundant tones are transmitted over successive symbol intervals, thereby achieving a time spread for added protection in fades. For most types of HF channel conditions, the Time/Frequency diversity will yield improved performance over the standard frequency diversity mode, although it will add some additional delay as shown in table 4-3.

Table 4-3. Diversity Factors

Baud Rate	Diversity Factor	Additional Delay (Time/Frequency Mode only)
2400	1	0
1200	1	0
600	2	180 ms
300	4	293 ms
150	8	338 ms
75	16	360 ms

#### 4.2.7 Signal Clipping

The audio output of the RF-3466A may be clipped to improve the system performance by limiting the peak-to-RMS ratio of the signal. The output signal is made up of 39 tones with equal amplitudes and resembles band-limited white noise. Periodic high peaks of this signal can be clipped without affecting the performance of the modem.

Limiting the peak-to-RMS ratio of the audio signal allows the power output of the HF transmitter to be increased. The added RF signal strength improves system performance.

Clipping is part of the digital signal processing and is enabled or disabled at the front panel. When clipping is enabled, the baseband peak-to-average ratio is maintained at 10 dB.

#### 4.2.8 Keyline Control

Keyline and mute signals are available on the radio interface connectors for controlling the HF transmitter and receiver.

Since the transmitter may require some time (from keyline assertion) before it can properly transmit, the modem waits for a selectable interval (the keyline delay) following the assertion of the keyline before enabling the modulator output. If necessary, the modem will hold off assertion of CTS to assure that no data will be lost during this keyline/audio delay.

The mute signal may be used to disable the receiver during transmission. It may be used to prevent receiver overload due to interference from the system transmitter in simplex operation.

#### 4.3 BINARY FSK THEORY OF OPERATION

In the FSK mode, the RF-3466A can interoperate with virtually any binary FSK modulator/demodulator. Mark/space frequency selections from 0 to 3400 Hz (1/2 Hz resolution) are accommodated. The modem uses two independent FSK modulators and demodulators with independent mark/space/rate selections for each channel. The two modulator/demodulator channels can also be configured for dual-channel diversity operation. See paragraph 4.4.4 for a detailed theory of operation.

#### 4.4 MAJOR ASSEMBLIES

Signal processing and data manipulation for 39-tone operation are performed on PWB assemblies A1, A2, A4, A6, A7, and A8. A5 provides FSK operation. The major assemblies of the RF-3466A are listed in table 4-4.

The functions of the individual assemblies are discussed in paragraphs 4.11.1 through 4.11.9.

##### 4.4.1 Analog I/O PWB Assembly A1

Figure 4-8 is a block diagram of the Analog I/O PWB Assembly Circuit. Analog-to-digital and digital-to-analog conversions are performed on this assembly. In addition, this assembly incorporates an audio AGC at the input of each diversity channel. Two audio ranges are available for this assembly. Jumper placement determines the audio range selected.

##### 4.4.1.1 Digital-to-Analog Conversion

The fully-modulated transmit data signal is received in digital form from Signal Processor assembly A2. The digital signal is received on lines MD4 through MD15 of the MOD/DEMODO resident bus. The data is clocked into FIFOs U8, U9, and U10. The data is clocked out of the FIFOs and into D-to-A converter U18 at 7200 Hz. The analog signal is a composite of the 39 orthogonal, phase-shifted tones. The signal is filtered by U3 and amplified by U7 before being sent to the transmitter from the rear panel. R22 provides gain adjustment for audio output level.

##### 4.4.1.2 Analog-to-Digital Conversion

The received audio signals from both diversity channels are passed through a 10 dB pad to multiplexer U1. During power-up BIT operation, the analog loopback signal is selected in place of the received audio, through multiplexer U1. Channel A and channel B audio signals are filtered by U2 and U3, respectively. The received audio signal from each channel is normalized to its rms value, such that the output signal from U28 is maintained at a constant rms level over a 30-dB dynamic range. Amplifier U4, RMS-to-DC converters U5 and U6, and analog divider U28 form a feed-forward AGC circuit configuration. The AGC exhibits an attack time

Table 4-4. Major Assemblies

Ref. Desig.	Assembly	Functions
A1	Analog I/O PWB	Performs analog-to-digital and digital-to-analog conversions. Provides input audio AGC.
A2	Signal Processor PWB	Performs all digital signal processing including; Fast Fourier Transform, Inverse Fast Fourier Transform, and Hilbert Transform.
A4	Mod/Demod PWB	Performs modulation and demodulation of tone set, signal presence detection, frequency correction, and frame (time) synchronization.
A5	Binary FSK PWB	Provides dual modulator/dual demodulator FSK capability.
A6	FEC I/O PWB	Performs FEC encoding; data I/O; supervision of all transmit and receive functions; front panel control and status; remote control and status; and supervises all BIT and diagnostics.
A7	Decoder PWB	Receives data from Mod/Demod as dot/cross pairs; performs all FEC decoding, hard and soft decision. Sends decoded data to FEC I/O for output to DTE.
A8	Digital I/O PWB	Provides parallel-to-serial interface between the FEC I/O processor and the front panel DTE and Remote Control. Provides non-volatile system RAM for communication between the FEC I/O, Mod/Demod, and Soft Decoder processors and storage of operating parameters.
A10	Interconnect PWB (Motherboard)	Provides bus and power connections for all assemblies.
A11	Front Panel Assembly	Provides operator/programmer controls for selecting operator parameters; provides the internal frequency standard and master oscillator.
A12	Rear Panel	Provides the mounting area for the I/O connectors. Filters input and output signals. Provides DTE and remote control line-drivers and receivers. Contains audio-transformers, keyline and mute switches.

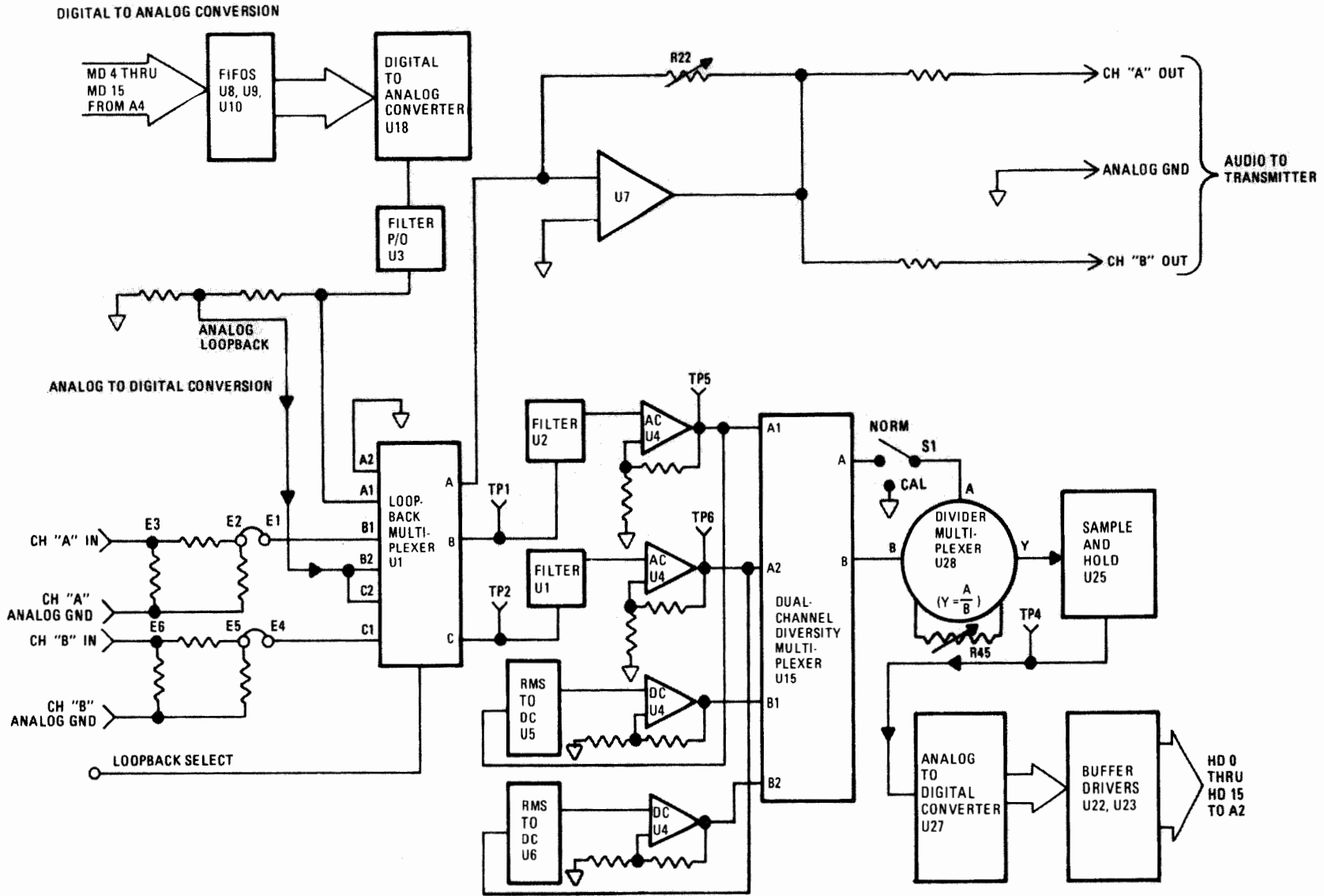
of approximately 30 ms, and a decay time of 450 ms. This is determined by averaging and filter capacitors associated with U4, U5, and U6. Multiplexer U15 permits the two diversity channels to timeshare divider U28. Analog divider U28 alternately passes channel A and channel B signals to sample and hold IC U25.

The standard audio input range over which AGC maintains a constant level is + 5 dBm to -25 dBm (jumper E1 to E2 and E4 to E5). The optional range of -5 dBm to -35 dBm is also available (jumper E1 to E3 and E4 to E6) for low signal level applications.

The sampling rate for each audio signal is 7200 Hz. The audio signal samples are converted to digital signals by A-to-D converter U27. The 12-bit output of U27 is buffered by U22 and U23, and placed on lines HD4 through HD15 of the Hilbert processor bus.

The AGC can be disabled by jumpering E8 to E9. The normal configuration is AGC enabled, E7 jumpered to E8.

Switch S1 and potentiometer R45, used for dc offset level adjustment, are factory set and should not be changed in the field. S1 must be left in the normal position (NORM) for proper operation of the AGC.



HSM-041

Figure 4-8. Analog I/O PWB Assembly Block Diagram

#### 4.4.2 Signal Processor PWB Assembly A2

The Signal Processor PWB assembly (A2) works with the MOD/DEMOD assembly to perform all digital signal processing. Figure 4-9 is a block diagram of the A2 assembly.

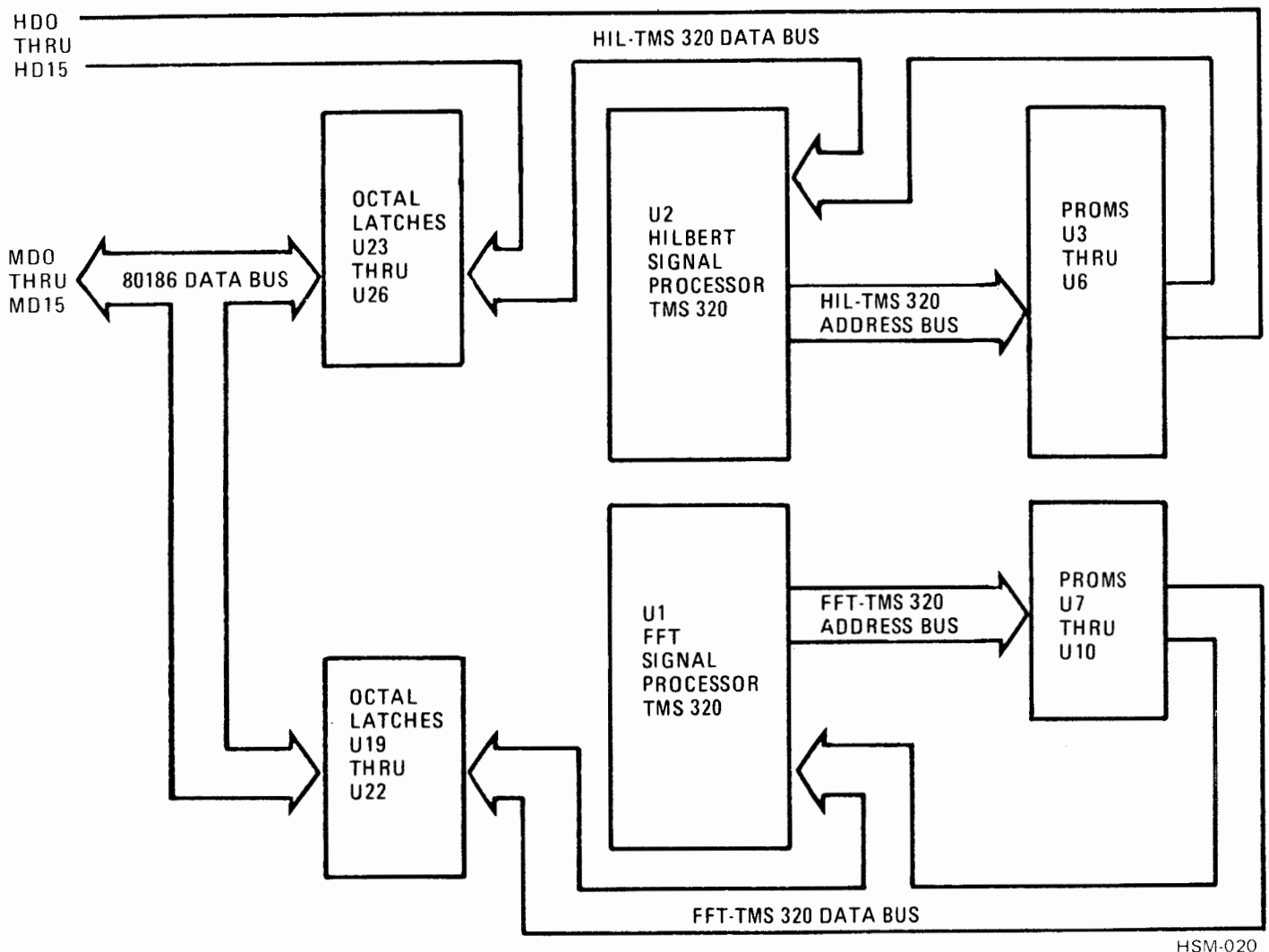


Figure 4-9. Signal Processor PWB Assembly Block Diagram A2

The major components of the A2 assembly are two TMS320 signal processors, U1, and U2. These are microprocessors designed to handle the lengthy, rapid calculations associated with digital signal processing. The two signal processors operate as slaves to the 80186 microprocessor on the MOD/DEMOD assembly. Each signal processor is dedicated to performing a certain set of calculations. U1 has been labeled the FFT signal processor. It performs the calculation of the fast Fourier transform during demodulation and the inverse fast Fourier transform during modulation. These functions are performed sequentially during full-duplex operation. The algorithms for these procedures are stored in PROMs U7 through U10. U2 is dedicated to performing the calculations of the Hilbert transform and is therefore called the Hilbert signal processor. The Hilbert transform algorithm is stored in PROMs U3 through U6.

The 12-bit digitized words representing the receive audio signal (i.e., time samples) are sent to the signal processing PWB assembly on lines HD4 through HD15 of the HIL-TMS320 data bus. Signal Processor U2 performs a Hilbert Transform (90° phase shift) on the incoming samples and subsequently applies the appropriate frequency correction as required. The corrected 12-bit words are then transferred to the Mod/Demod PWB Assembly via MD0 through MD15. The Mod/Demod PWB returns 128-word blocks of the digitized audio samples to the FFT Processor U1, for fast Fourier Computations.

The transmit audio signal is manufactured digitally primarily by the MOD/DEMOMD PWB assembly. The digital representation of the modulated tones is sent to the FFT processor on A2. The FFT processor performs an inverse fast Fourier transform that sums the individual tones to create the complete transmit audio signal. The signal is transferred to the Analog I/O assembly on MD4 through MD15 of the MOD/DEMOMD resident bus for D-to-A conversion.

#### **4.4.3 MOD/DEMOMD PWB Assembly A4**

Figure 4-10 is a block diagram of the MOD/DEMOMD PWB assembly. The major component of the assembly is an 80186 microprocessor, U1. Other components of the assembly make up the microprocessor support circuit and include latches, buffers, bus transceivers, interrupt controllers, a programmable timer, and an expandable memory. U1 functions as a slave to the microprocessor on the FEC I/O PWB assembly and a master to the TMS320 signal processors on the Signal Processor PWB assembly. The MOD/DEMOMD PWB assembly oversees all digital signal processing tasks, including data transfers between the A4 and A2 assemblies and to the A1 assembly.

Two bus systems are used to transfer data to and from the A4 assembly. The system buses connect the A4 assembly via the A8 Digital I/O PWB assembly to the A6 FEC I/O assembly, and the A7 Soft Decoder assembly. The resident buses connect A4 with the Signal Processor assembly A2 and the Analog I/O assembly A1.

#### **4.4.4 FSK PWB Assembly A5**

Figure 4-11 is a block diagram of the FSK PWB Assembly A6. The major component of the assembly is the TMS 320C25 digital signal processor which uses digital signal processing techniques to improve reliability, precision, and performance.

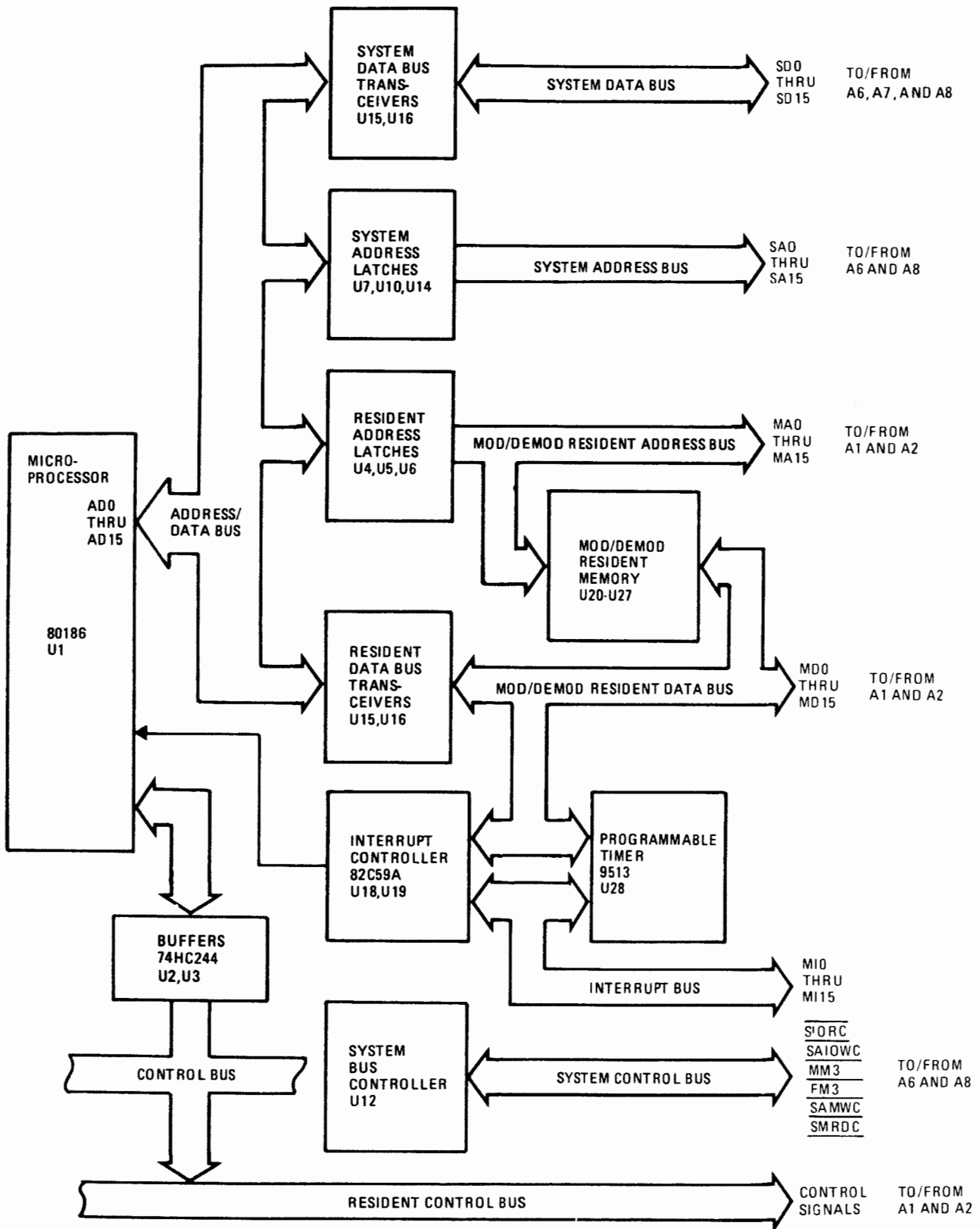
##### **4.4.4.1 FSK PWB Transmit Data Signal Flow**

The FSK mode is implemented in hardware and firmware contained on the A5 assembly. As shown in figure 4-12, the TX Data Signal enters the board from the data terminal equipment via the A12 rear panel assembly and is routed directly to the digital signal processor (U29). The incoming clock and control signals, and the Secondary TX Data, are read into the digital signal processor (DSP) using buffer U7.

The FSK modulator block includes:

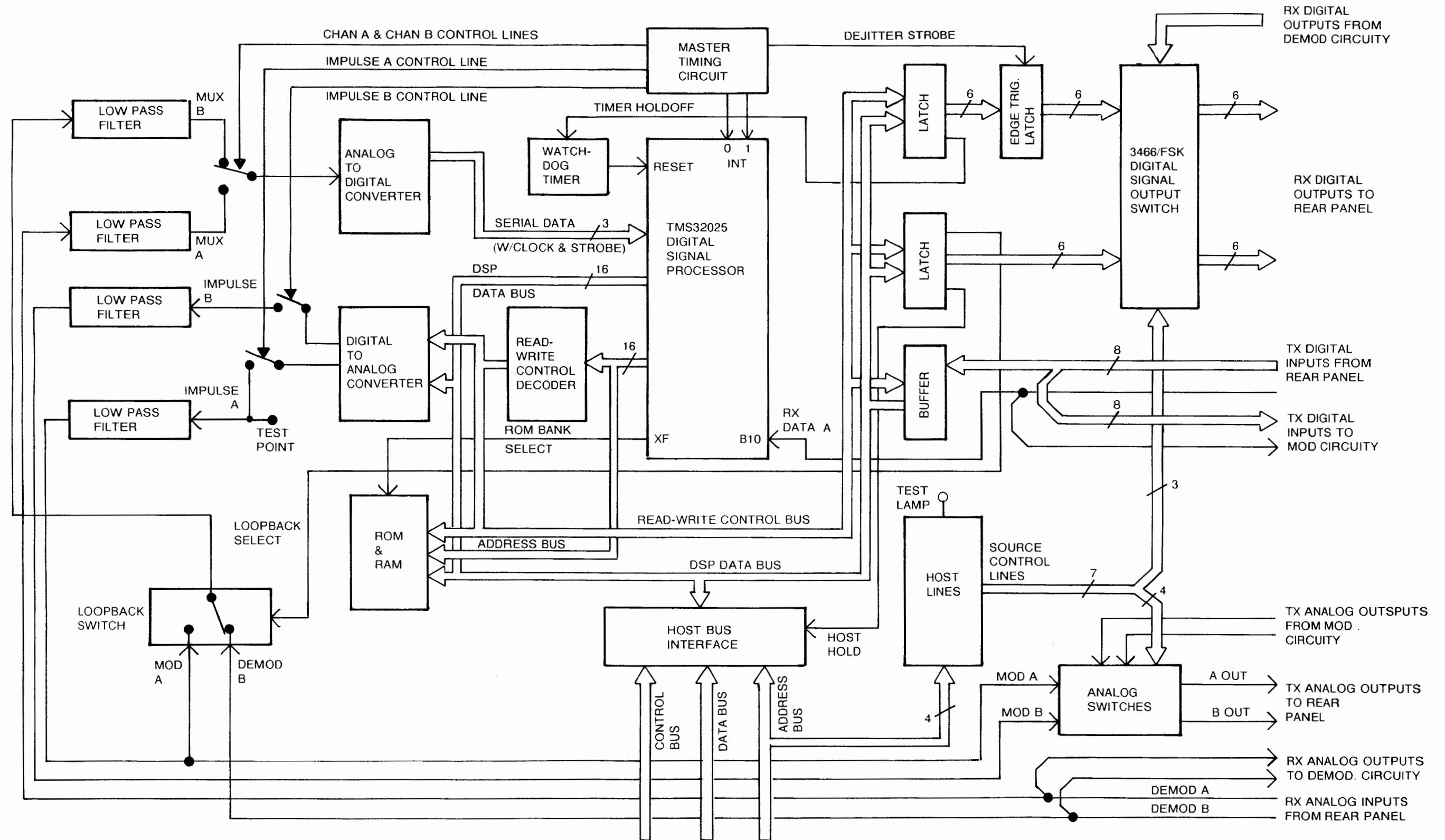
- A digital signal processor (DSP) U29, which is a 16-bit microprocessor with a specialized instruction set for this type of application.
- A read only memory (ROM), and a read-write memory (RAM) associated with and controlled by the DSP.
- A read-write control circuit controlled by the DSP.

The DSP is interrupted at regular intervals by the INT 0 and INT 1 signals. These 14.4 kHz pulse trains are effectively 180 degrees out of phase. Together, they force the DSP to alternate between processing the transmit data circuits A and B. At the end of each processing sequence the processed data is written to the digital-to-analog (D-A) latches (U35 and U36) via the DSP data bus.



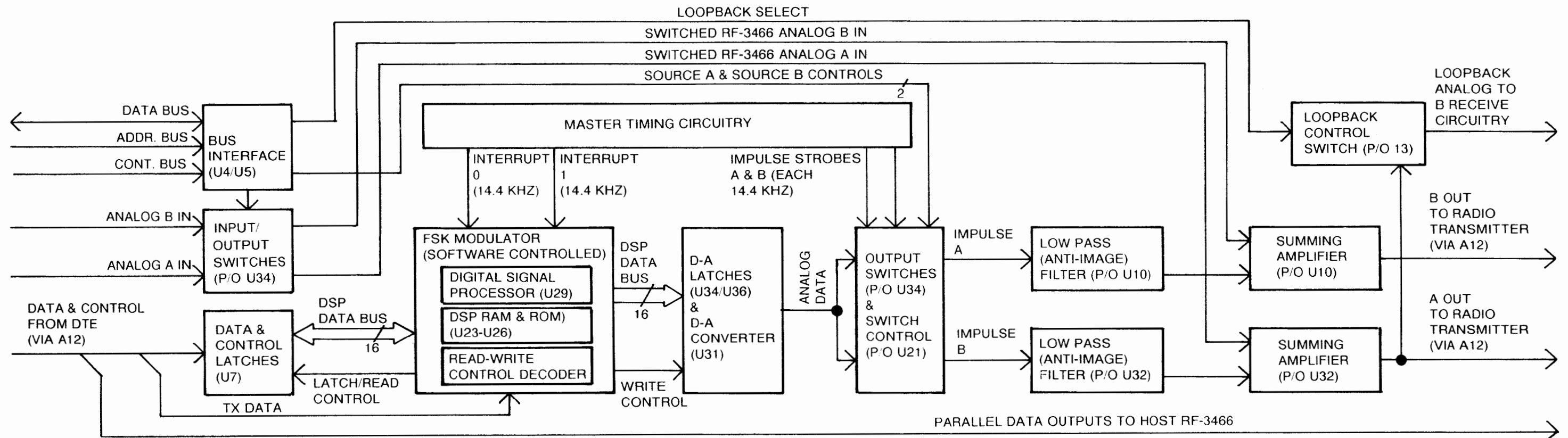
HSM-021 (B)

Figure 4-10. MOD/DEMOM PWB Assembly Block Diagram



3466A-007

Figure 4-11. FSK PWB (P/N 10133-2500) Block Diagram



3466A-005

Figure 4-12. FSK PWB Transmit Signal Flow

The D-A converter reads parallel data from the D-A latches and outputs it as an analog signal consisting of alternating channel A and channel B signals. These are routed to two output switch sections of U34.

The U34 switch sections are enabled by the Host Bus Interface circuitry, and their output is clocked by Impulse Strobe A and Impulse Strobe B signals from the master timing circuitry. The resulting outputs are two amplitude modulated pulse trains, designated Impulse A and Impulse B, each having a 14% (1:7) duty cycle.

The Impulse A and Impulse B signals are routed through 3400 Hz low pass filters, and form one input to A and B signal combiners. Additional input to these combiners are normal transmit tone data signals routed through additional switch sections of U34. The resulting signals, A Out and B Out, are routed to radio transmitter(s) via the A12 Rear Panel Assembly.

#### 4.4.4.2 FSK PWB Receive Data Signal Flow

As shown in figure 4-13, channel A and channel B tone data is received from the radio receivers via the A12 Rear Panel Assembly. When commanded by the DSP microprocessor, the transmitted A Out signal can be looped back to the B channel input via a portion of U13.

The signals are then routed through 3400 Hz low pass filters to additional input switching. Two 14.4 kHz squarewave control signals, Chan A and Chan B, are 180 degrees out of phase and multiplex the two input signals into a single analog data signal to the A-D Converter.

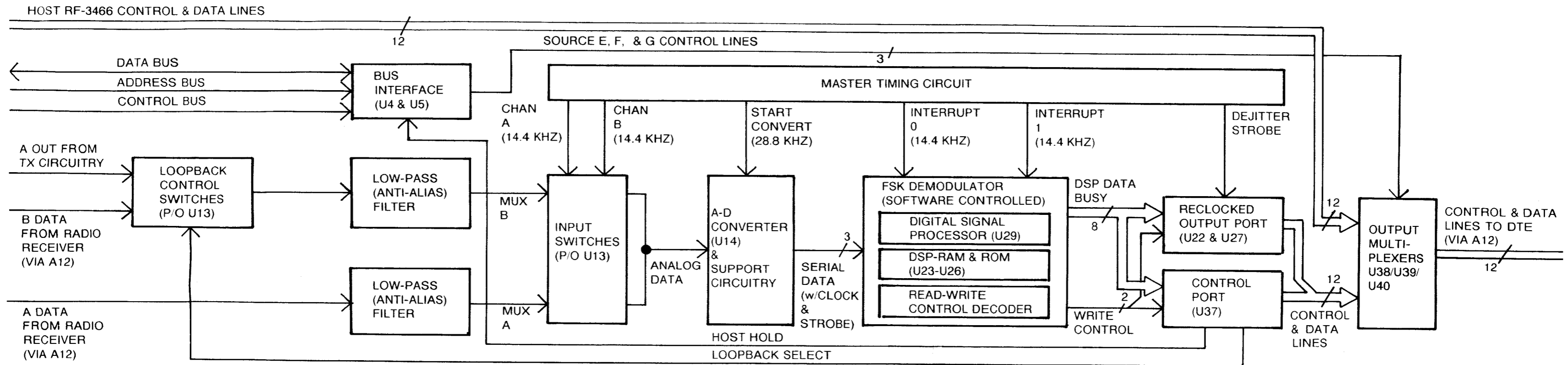
The A-D converter alternately samples the A and B channel tone data which it then converts to a serial data stream that is sent to the DSP for processing. The serial interface is synchronous and consists of A-D Data, A-D Clock, and A-D Strobe. The FSK Demodulator is the same digital signal processor, RAM, ROM, and read-write control circuitry described previously. The difference between transmit and receive operation is in the software. As with transmit signal processing, the Interrupt 0 and Interrupt 1 signals from the master timing circuitry are used to synchronize the DSP between channel A data and channel B data.

The FSK Demodulator performs the required signal processing, and the resulting data is written to the Control Port (U37) and the Reclocked Output Ports (U22 and U27). Because different signal processing routines may require varying amounts of time, the timing of data written into these circuits may not be synchronized with the board's master timing signals. The Dejitter Strobe, derived from board's master timing, synchronizes the timing of selected output signals (i.e.: Rx Data, Rx Clock, etc.), and prevents jitter in their logic level transitions.

Terminal data and control signals are routed from the Control and Reclocked Output Ports to the U38, U39, and U40 Output Multiplexers. Equivalent signals from the RF-3466A are also routed to these multiplexers. The multiplexers switch between these two sets of input under the control of the Source E, Source F and Source G lines, and the multiplexer output signals are routed to the data terminal via the A12 Rear Panel Assembly.

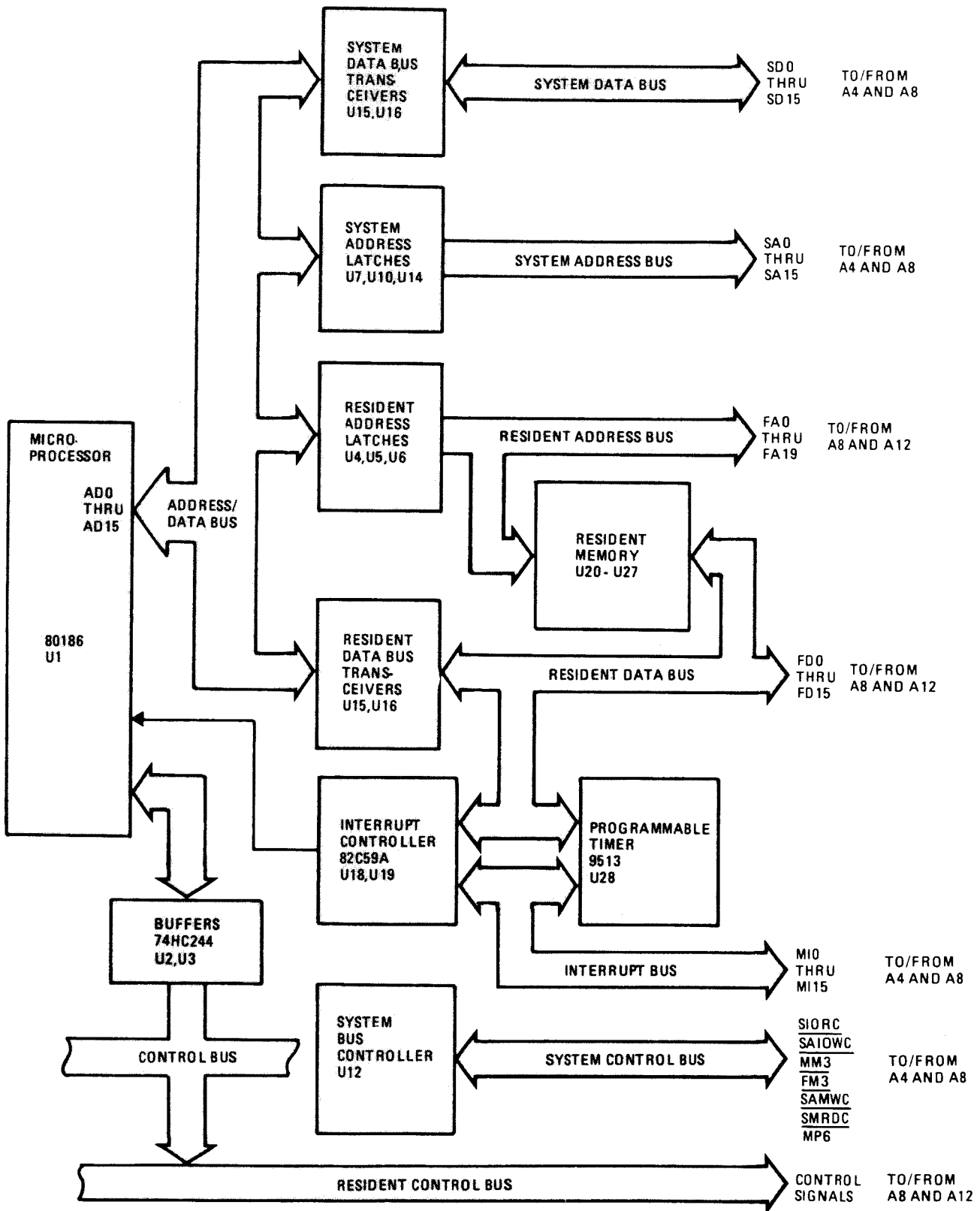
#### 4.4.5 FEC I/O PWB Assembly A6

Figure 4-14 is a block diagram of the FEC I/O PWB assembly A6. The major component of the FEC I/O assembly is an 80186 microprocessor U1, which acts as the master processor for the modem. The other components of the FEC I/O assembly make up a support circuit for the microprocessor. U1 generates FEC codes, controls the BIT/BITE operation, and oversees the signal processing. Two separate bus systems are used to connect the FEC I/O PWB assembly with the modem's other assemblies. The system buses transfer data and control signals between A6, A4, and A7 via A8. The resident buses pass data and control signals from A6 to the Front Panel PWB A11 and the Digital I/O assembly A8.



3466A-006

Figure 4-13. FSK PWB Receive Signal Flow



HSM-022(A)

Figure 4-14. FEC I/O PWB Assembly Block Diagram

#### 4.4.6 Decoder Assembly A7

The A7 Decoder Assembly receives data from the A4 Mod/Demod PWB as dot/cross pairs and performs all FEC decoding (hard and soft decision). It also sends decoded data to the A6 FEC I/O PWB for output to the DTE. Figure 4-15 is a block diagram of the Decoder PWB.

The Decoder's most significant component is an 80186 microprocessor (U1). Other components on the assembly contribute to the microprocessor support circuit. This circuit consists of latches, buffers, bus transfers, an interrupt controller, a programmable timer, and an expandable memory.

The system buses interface the A7 assembly with the A8 Digital I/O PWB Assembly and the A6 FEC I/O PWB Assembly. The resident bus is used for communicating with the memory and peripheral devices on the Soft Decoder board.

#### 4.4.7 Digital I/O PWB Assembly A8

Figure 4-16 is a block diagram of the Digital I/O PWB assembly A8. The major function of the assembly is to interface the modem with the Data Terminal Equipment (DTE) and the remote control unit. It also provides the serial interface between the front panel assembly and the FEC I/O assembly A6. Universal Synchronous Asynchronous Receiver Transmitters (USARTs) perform the interface functions including parallel-to-serial and serial-to-parallel conversions.

The non-volatile system RAM can be accessed by the FEC I/O, Soft Decoder, and MOD/DEMOM PWB assemblies through the system buses.

The six octal DIP switches, mounted on A8, are reserved for future options and enhancements.

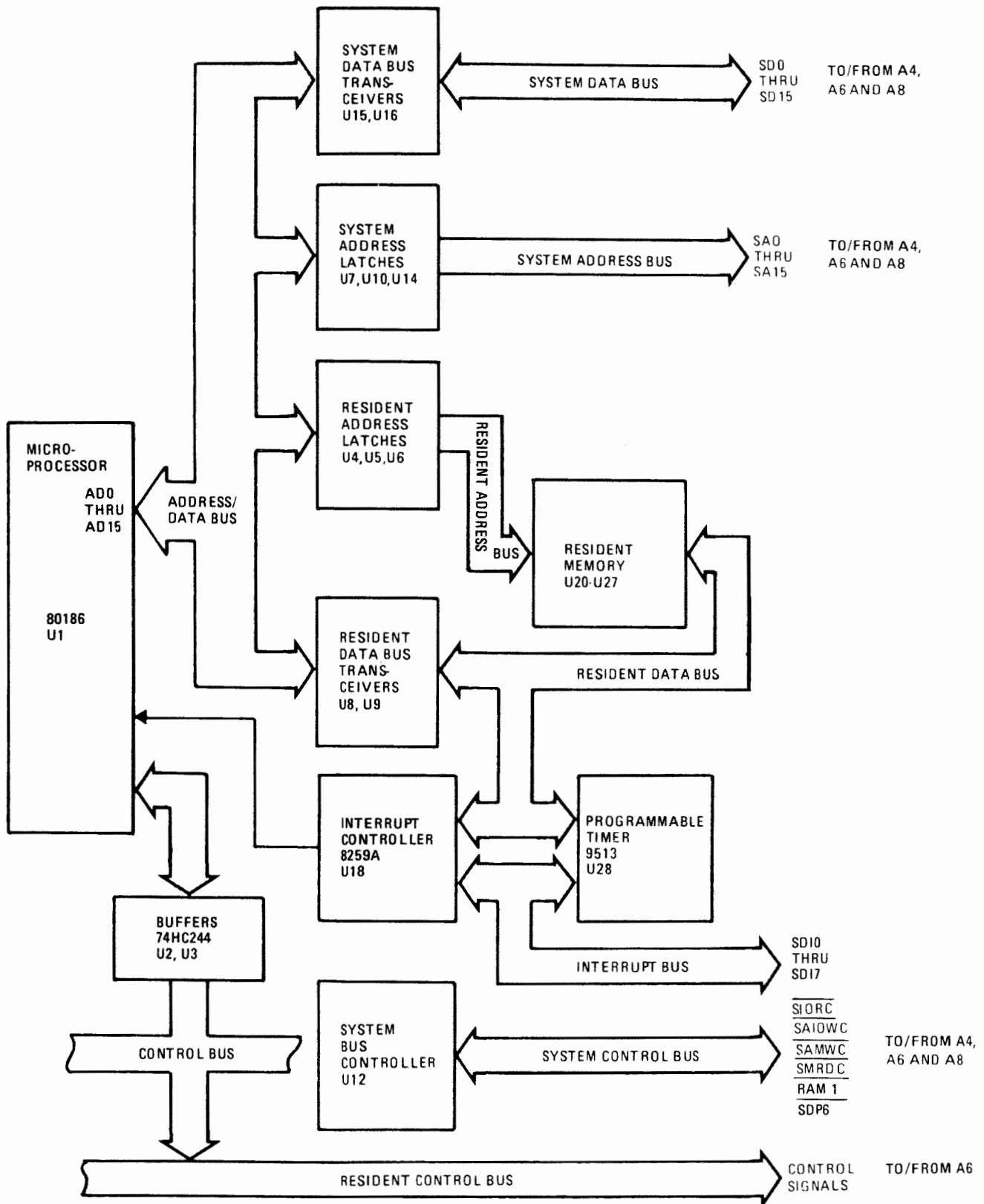
The modem's watchdog timer is located on A8. The function of this timer is to reset the modem in the event of an on-line hardware failure. The timer is a monostable multivibrator (one-shot) that is reset periodically by the microprocessor on the FEC I/O PWB assembly. When the modem is operating correctly, the timer will always be reset before it times out.

A reset switch is mounted on the A8 assembly. This can be used by the operator or installation technician to reset the modem.

#### 4.4.8 Ac Power Supply Assembly A9

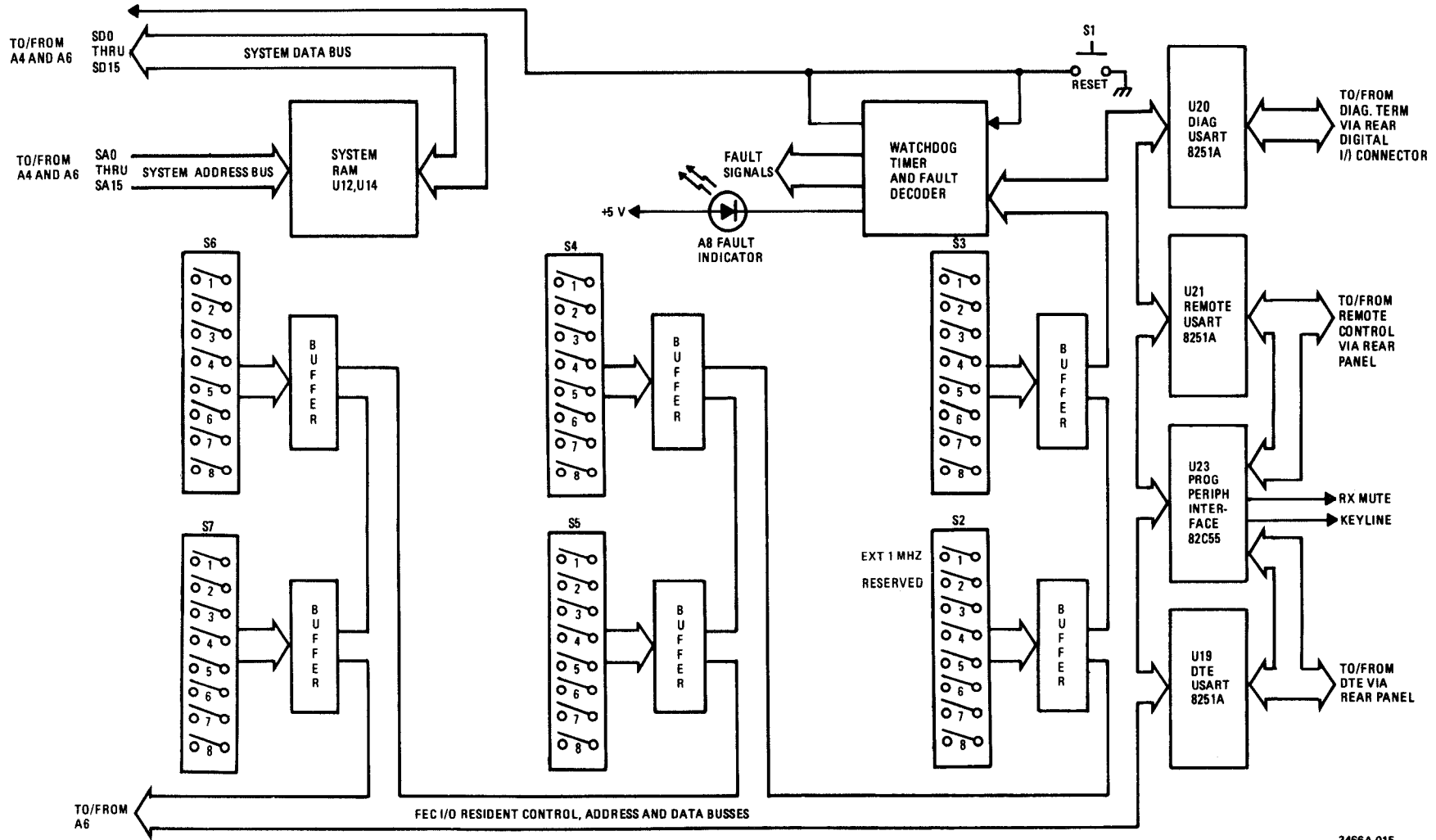
The modem is normally equipped with an ac-to-dc switching power supply assembly, A9. The supply can operate on a 115V or 230V ac line source. The supply generates dc outputs of 17 Amps at +5 V, 1 Amp at +15 V, and 1 Amp at -15 V. All inputs and outputs of the supply are EMI-filtered by the A9A2 assembly. Figure 4-17 is a block diagram of the power supply assembly. The supply is equipped with overvoltage protection and two current limiter circuits for the high current +5 V supply. The primary current limiter automatically restores the 5 V supply when an existing overcurrent condition is removed. A backup current limiter shuts down the supply if the primary protection fails. Ac undervoltage protection and soft-start power-up protection are built-in.

Potentiometer R27 provides adjustment of the +5 V output level. Potentiometer R52 provides adjustment of the short circuit current limit of the supply (current limit occurs when the load current exceeds 17 Amps from the +5 V output). Both adjustments are set at the factory and require no further field adjustment.



3470-004

Figure 4-15. Decoder Block Diagram



3466A-015

Figure 4-16. Digital I/O PWB Assembly Block Diagram

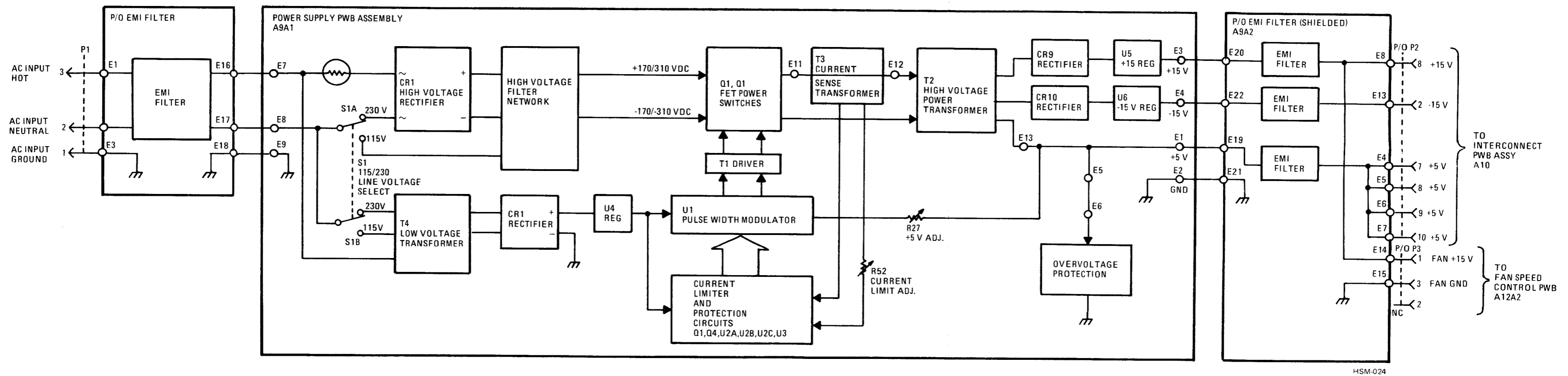


Figure 4-17. Power Supply Assembly Block Diagram

#### 4.4.9 Interconnect PWB Assembly A10

Interconnect PWB assembly A10 provides interconnection for all other subassemblies of the modem. Most control signals, address signals, data, and power are distributed by the Interconnect PWB Assembly. All assemblies except the front and rear panels, and the power supply, mount on the Interconnect PWB assembly via board edge connectors.

#### 4.4.10 Front Panel Assembly A11

The Front Panel assembly A11 consists of 3 subassemblies:

- Logic/Clock assembly A11A1
- Switch assembly A11A2
- Display assembly A11A3

The Display assembly is a self-contained module with no serviceable components. The A11A1 and A11A2 assemblies are described in detail in the following paragraphs. Figure 4-18 is a block diagram of the Front Panel assembly.

##### 4.4.10.1 Logic/Clock Assembly A11A1

The Logic/Clock assembly contains two independent circuits that can be considered as two separate assemblies, although they are contained on the same circuit board. The Logic circuit performs all functions related to the front panel. The interface to this circuit is a serial RS-232 link which connects the Logic circuit to the Digital I/O assembly A8. The Clock circuit generates the 10.1376 MHz master oscillator signal. The interface to this circuit is a parallel TTL level link which connects the clock circuit directly to the resident bus of the FEC I/O assembly A6.

The core of the Logic circuit is microcontroller U1. Support circuitry includes the watchdog timer circuit U2 and Q1, address latch U4, Read Only Memory (ROM) U6, chip select generator U16, and LED drivers U7 and U8. Multiplexer U10 allows the serial link to be switched between the Logic circuit and a diagnostic port used by service personnel. U9 performs level translations between RS-232 and TTL signals for the serial links. There are provisions for future enhancements via the Random Access Memory (RAM) site U3. Note that this is a socket designed to accept a RAM device when needed. The data bus and control signals from U1 are routed to the Display Module A11A3 via connector J3.

The Clock circuit generates the 10.1376 MHz master oscillator, and consists of a phase locked loop (PLL) made up of PLL U13, loop filter U14, and voltage controlled oscillator (VCO) U23. The frequency reference for U13 can be either 9600 Hz or 1 MHz, depending on the source of the reference. If the modem clock (Main Set Up Mode) is set for Internal or Ext DTE reference, then the source is an internally generated 9600 Hz clock. If it is set for Ext 1 MHz, then the reference is 1 MHz.

The source of the 9600 Hz is a PLL circuit consisting of U21, U22, and voltage controlled crystal oscillator (VCXO) Y2. Multiplexer U19 controls whether the 9600 Hz oscillator will be locked to the DTE TX clock or free running. U20 latches data from the FEC I/O assembly A6 to control the 9600 Hz PLL circuit. Multiplexer U12 performs switching between the external 1 MHz and internal 9600 Hz references for the 10.1376 MHz PLL. Differential amplifier U11 is used for waveshaping and amplification of the external 1 MHz reference.

#### 4.4.10.2 Switch Assembly A11A2

Switch assembly A11A2 contains all front panel controls and indicators, with the exception of the Vacuum Florescent Display module A11A3. The assembly connects to the Logic/Clock assembly via a parallel interface at J1. All front panel switches are configured in a matrix which is scanned by microcontroller U1 of the Logic/Clock Assembly A11A1. When any button is depressed the key closure is detected by the scanning process and appropriate action is initiated. The front panel LEDs are current-limited by resistors R1 and R2. Note that provisions have been made for future enhancements of the RF-3466A. The assembly has been designed to allow additional switches and LEDs to be added if needed.

#### 4.4.11 Rear Panel Assembly A12

The Rear Panel assembly includes four PWBs: three filter PWB assemblies (A12A1A1 through A12A1A3), and the Fan Speed Control PWB (A12A2). The filter PWB assemblies provide filtering, buffering, and signal isolation as required and physical connection between the rear panel and other modem assemblies. The Fan Speed Control PWB is an adjustable voltage regulator that supplies the modem's cooling fan. A block diagram of the filter assembly is shown in figure 4-19.

##### 4.4.11.1 Rear Panel Filter Assembly

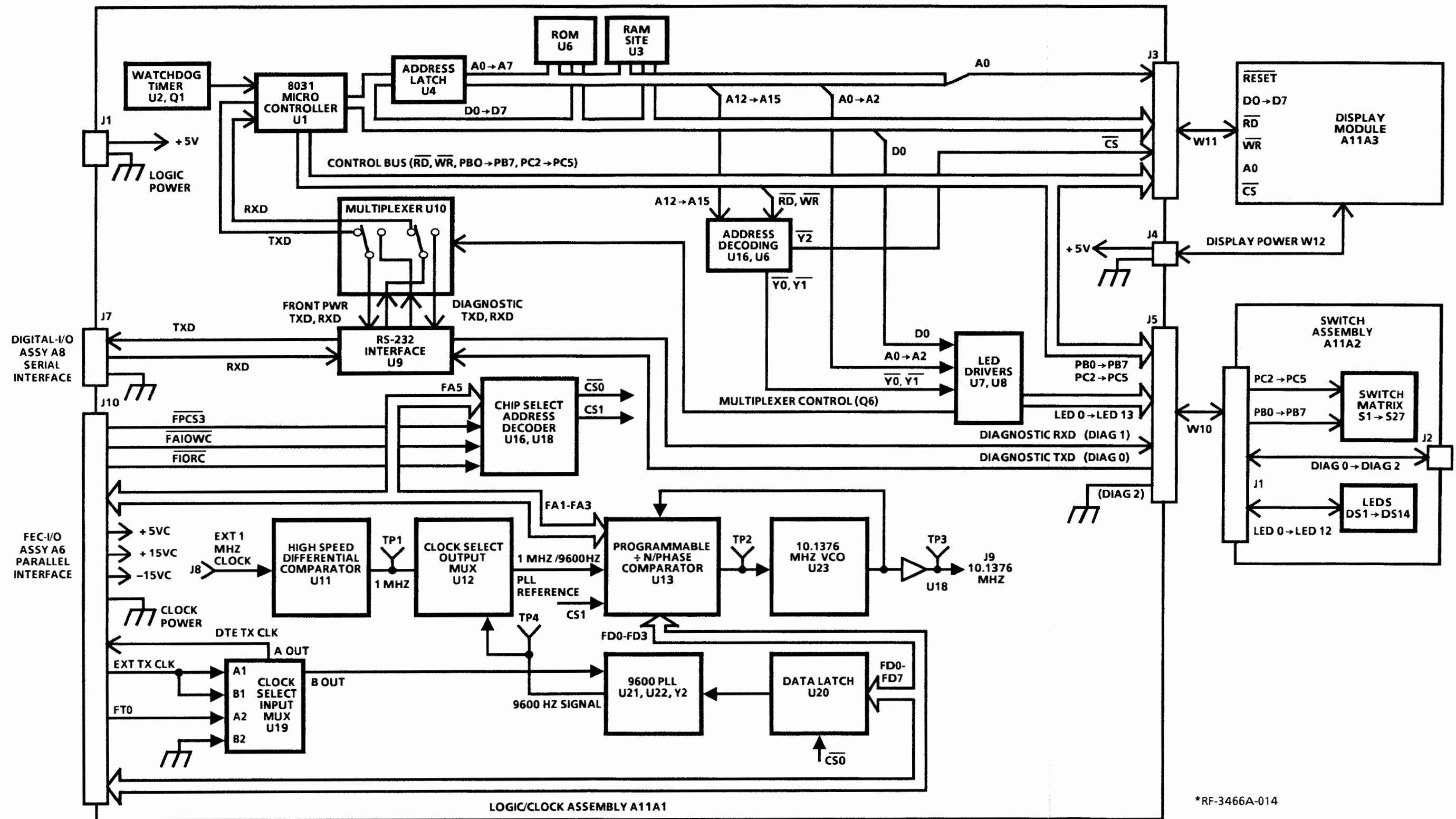
Filter PWB Assembly No. 1, A12A1A1 performs several interface functions. Manually operated switches, S1 and S2, are used to select EIA RS-232C, MIL-188C, or MIL-188-100 for the data terminal interface. Line drivers and receivers are provided for the remote control lines and the DTE lines. Solid-state switch networks (Q1, Q3 and Q2, Q4) are used to control the KEYLINE/MUTE signals. Transformers T1 through T4 provide isolation and impedance matching for the Audio In and Audio Out signals. Test points for monitoring the Audio In signals and power supply voltages are located on the A1 assembly. TP1, TP2, and TP3 are used to monitor the Audio In signals. TP4 monitors the positive line driver supply, TP5 monitors the negative line driver supply, and TP6 monitors the + 5 V supply.

Filter PWB Assembly No. 2, A12A1A2 provides RC filtering for most signals entering or leaving the modem. The assembly also connects Filter PWB Assembly No. 1 with Filter PWB Assembly No. 3. Test points for monitoring some of the DTE interface signals and the Audio Out signals are also located on the A2 assembly. TP1 through TP4 monitor Audio Out (channels A and B). TP5 monitors RX Data, TP6 monitors TX Clock, and TP7 monitors TX Data.

Filter PWB Assembly No. 3, A12A1A3 contains rear panel connectors J1, J3, J4, and J5. The A3 assembly provides a physical connection between the rear panel and Filter PWB Assembly No. 2. Test points for monitoring the remote control RS-422 interface and some of the DTE interface signals are located on the A3 assembly. TP1 and TP2 monitor 422 OUT, TP3 and TP4 monitor 422 IN. TP5 monitors CTS, TP6 monitors RX Clock, and TP7 monitors RTS.

##### 4.4.11.2 Fan Speed Control

Fan Speed Control PWB assembly A12A2 switches the cooling fan speed between fast and slow depending upon the modem's temperature. The assembly is essentially a temperature-controlled voltage regulator. The assembly delivers approximately 9 volts to the fan for slow speed operation and approximately 12 volts for the faster fan speed. Figure 4-20 is a block diagram of the assembly. U1 is a temperature-sensitive diode. The voltage drop across the diode varies directly with the internal temperature of the modem. The voltage drop across the diode is compared to a preset fixed value by U2A. U2A controls the regulator circuit (U2B, Q1) to deliver + 9 V or + 12 V to the fan as required. Resistor R3 establishes the temperature at which the fan switches to high speed (approximately 32° C external ambient).



\*RF-3466A-014

Figure 4-18. Front Panel Assembly Block Diagram

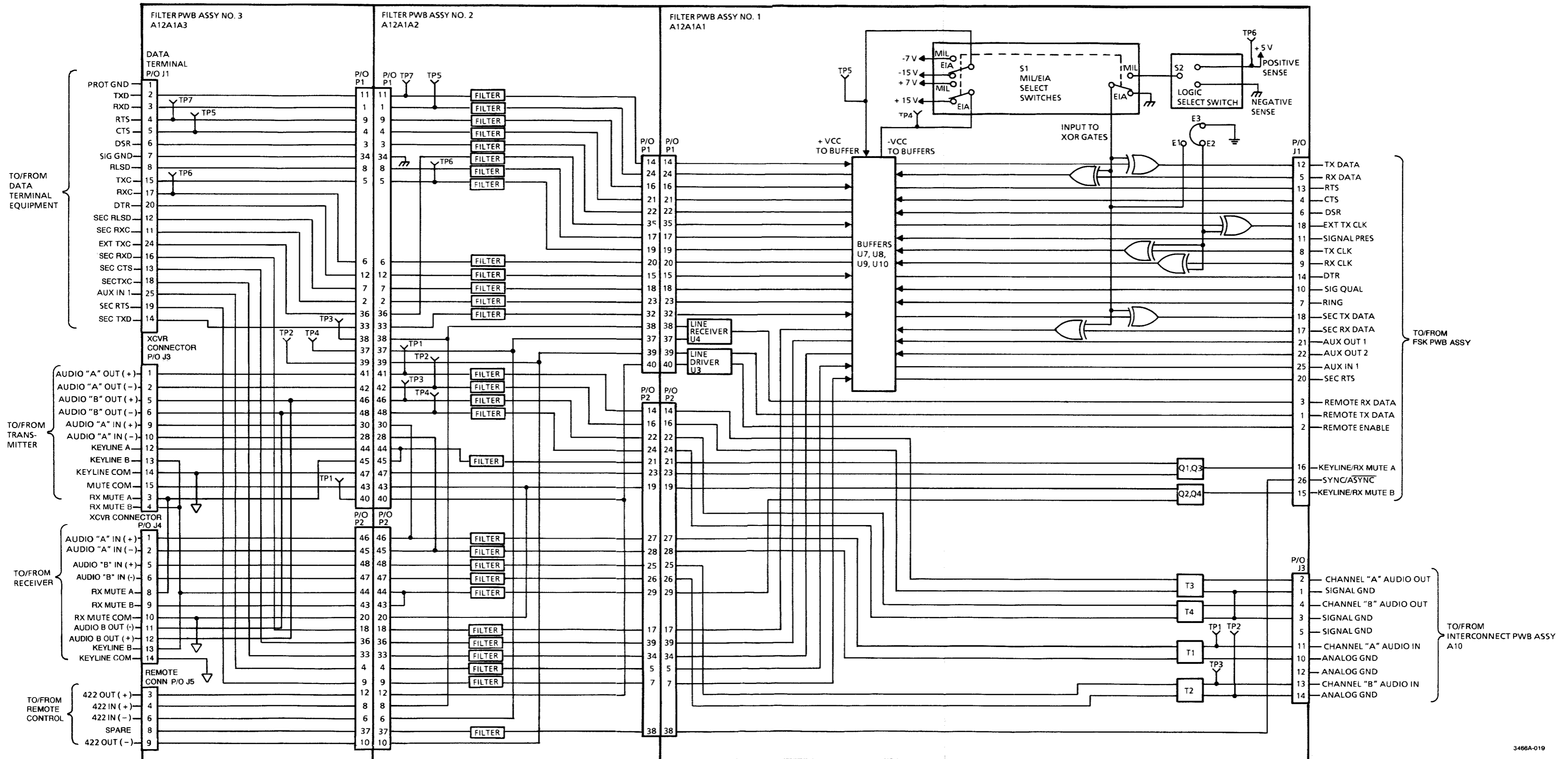


Figure 4-19. Rear Panel Filter Assembly A12A1 Block Diagram

3466A-019

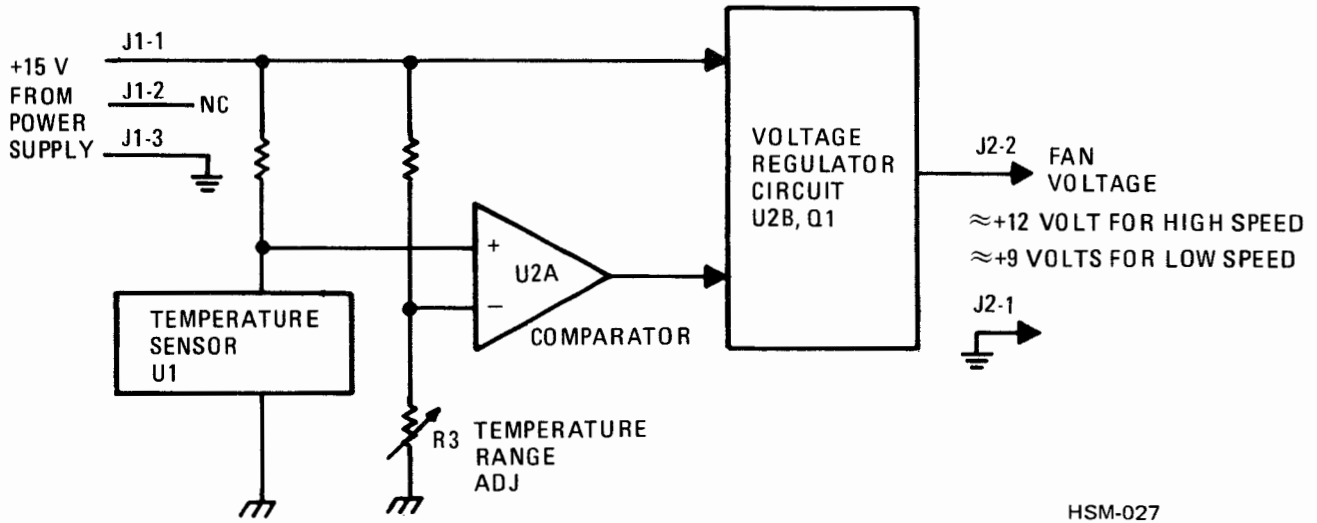


Figure 4-20. Fan Speed Control Block Diagram

## SECTION 5 MAINTENANCE

### 5.1 INTRODUCTION

Advanced hardware and software design techniques have been used in the RF-3466A to minimize regular maintenance and simplify troubleshooting procedures. The Built-In-Test (Bit) feature can be used to quickly identify and replace faulty modules in the field.

The use of high speed microprocessors and complex programming makes troubleshooting to the component level difficult even when the proper test equipment is available. Therefore, it is recommended that a spares program be developed through Harris Corporation, RF Communications Group, Long Range Radio Division, Field Service.

#### NOTE

Tables 2-8, 2-9, 2-10, and 2-13 list the operating parameters that were selected when the unit was shipped from the factory. Refer to these tables for system alignment.

#### 5.1.1 Protection of Static Sensitive Devices

Diode input protection is provided on all CMOS devices. This protection is designed to guard against adverse electrical conditions such as electrostatic discharge. Although most static sensitive devices contain some protective circuitry, several precautionary steps should be taken to avoid the application of potentially damaging voltages to the inputs of the device.

To protect static sensitive devices from damage, the following procedures should be followed:

- a. Keep all static sensitive devices in their protective packaging until needed. This packaging is conductive and should provide adequate protection for the device. Storing or transporting static sensitive devices in conventional plastic containers could be destructive to the device.
- b. Disconnect power prior to insertion or extraction of sensitive devices. This also applies to PWBs containing such devices.
- c. Double check test equipment voltages and polarities prior to conducting any tests. Verify that no transients exist.
- d. Use only soldering irons and tools that are properly grounded. Ungrounded soldering tips or tools can destroy these devices. **SOLDERING GUNS MUST NEVER BE USED.**
- e. Avoid contact with the leads of the device. The component should always be handled very carefully by the ends or the side opposite the leads.
- f. Avoid contact between PWB circuits or component leads and synthetic clothing.

## 5.2 REQUIRED PERIODIC MAINTENANCE

### 5.2.1 Air Filter Removal and Cleaning

The air filter on the front panel should be removed and cleaned at regular intervals. Frequency is determined by the amount of dirt and dust in the surrounding environment.

#### 5.2.1.1 Procedure

- a. Remove air filter by flexing it between two fingers and pulling gently.
- b. Wash filter in a mild soap solution and rinse thoroughly.
- c. Dry filter completely.
- d. Replace filter by flexing between two fingers and inserting in opening.

### 5.2.2 Alignment Procedure 9600-Hz PLL

The only adjustment on the A11A1 Logic/Clock PWB (P/N 10133-1850) is the free-running frequency of the 9600-Hz Phase Lock Loop Circuit. Perform the following steps to make this adjustment:

#### CAUTION

The 9600-Hz PLL adjustment should be attempted only if a frequency counter with 7 digits of accuracy and .001 Hz resolution is available. This adjustment will be required only if the 9600-Hz VCXO frequency should drift due to aging, or if components in this circuitry are replaced.

- a. Switch off ac power to the RF-3466A. Remove the top cover.
- b. Connect a frequency counter probe to TP4 of the A11A1 Logic/Clock PWB.
- c. Switch on ac power to the RF-3466A.
- d. Ensure that frequency standard select on the Main Set Up Mode is set to the INTERNAL position.
- e. Adjust A11A1-R18 so that the frequency measured at TP4 is 9600 with an accuracy of  $\pm 0.02$  Hz or better.
- f. Remove the frequency counter probe from A11A1-TP4, and set frequency standard on Main Set Up Mode to the desired operating position.

## 5.3 BIT/BITE DESCRIPTION AND USE

The BIT (Built-In-Test) feature of the RF-3466A can be used to quickly identify and replace faulty modules. The BIT is a resident program that automatically runs when the modem is powered up or reset, when the power-up BIT select is in the ON position. Loopback paths have been included in the hardware design to facilitate the automatic testing. The front panel alphanumeric display is used to display fault messages, and each module is equipped with its own LED fault indicator.

The BIT routine can be initiated manually by pressing the TEST pushbutton. If power up BIT is enabled the BIT routine will be run automatically in the event of a catastrophic failure (a micro-processor malfunction that causes the watchdog timer to timeout and trigger a reset). The BIT is performed in two segments. First, the memories are checked and then the signal processing functions are checked. The two segments of the BIT are illustrated in figures 5-1 and 5-2. In some cases, the BIT will not be able to isolate a fault to an individual module. In these cases, the fault message will indicate that one of two possible failed modules, will be indicated. If no faults are detected, the self-test sequence will require approximately 32 seconds to complete.

Normally, the modem will halt if the BIT discovers a failure. However, this feature is undesirable in some tactical situations. Therefore, the halt on fault feature can be overridden by disabling it in the Main Set Up Mode.

Assembly locations are called out in figure 5-3.

## 5.4 TROUBLESHOOTING GUIDELINES

### 5.4.1 General

Most major failures are detected and reported by BIT. The unit will automatically be tested upon power up if the Power Up bit is enabled, but the operator can run BIT at any time by pressing the TEST pushbutton.

To replace a failed module:

- Turn the POWER switch to the off position.
- Remove the modem's top cover.
- Remove the failed module. Note its position and orientation.
- Insert the replacement module in the same slot and with the same orientation.
- Turn POWER switch to the ON position. The unit will automatically initiate a BIT procedure.
- Replace top cover if the unit passed the BIT.

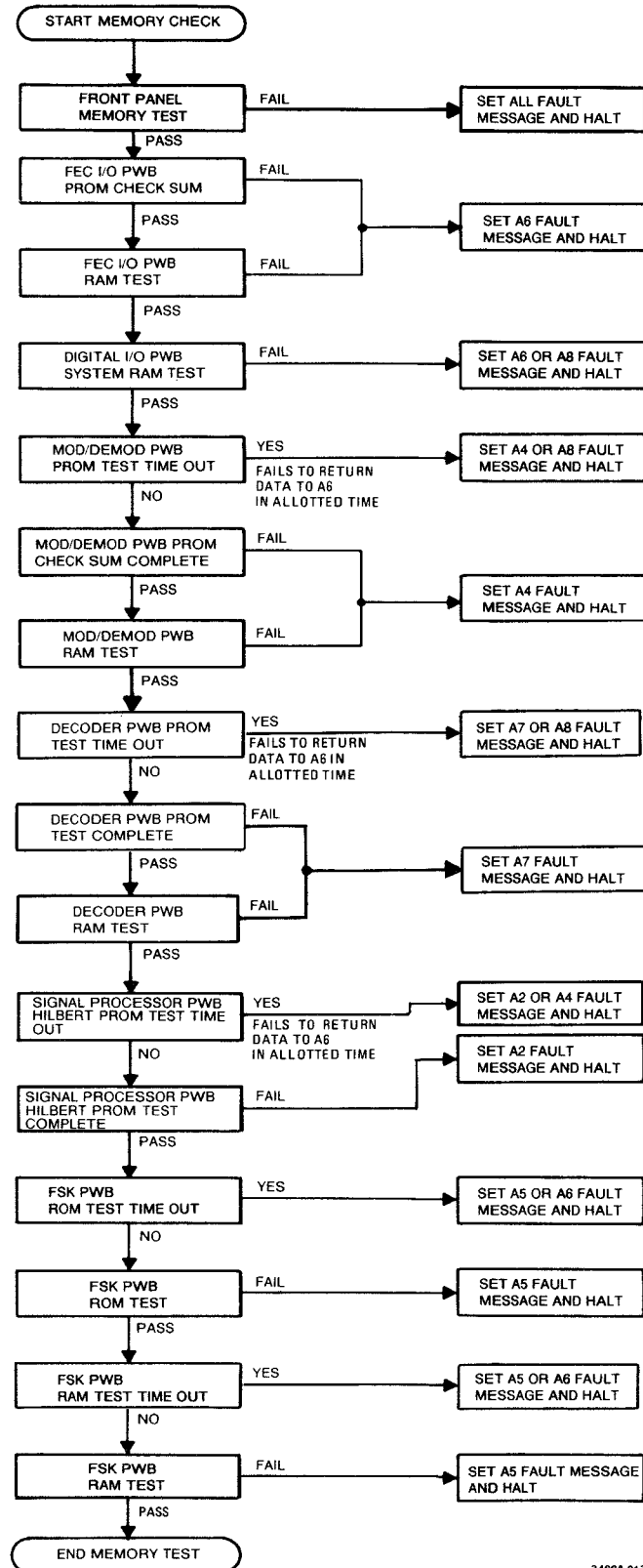
When BIT indicates that one of two modules has failed, replace the indicated modules, one at a time. To isolate the faulty module, run BIT after each suspected module is replaced.

### 5.4.2 Power Supply/Rear Panel/Fan

BIT does not test the Rear Panel assembly or the power supply; however, faults on these assemblies are relatively easy to isolate.

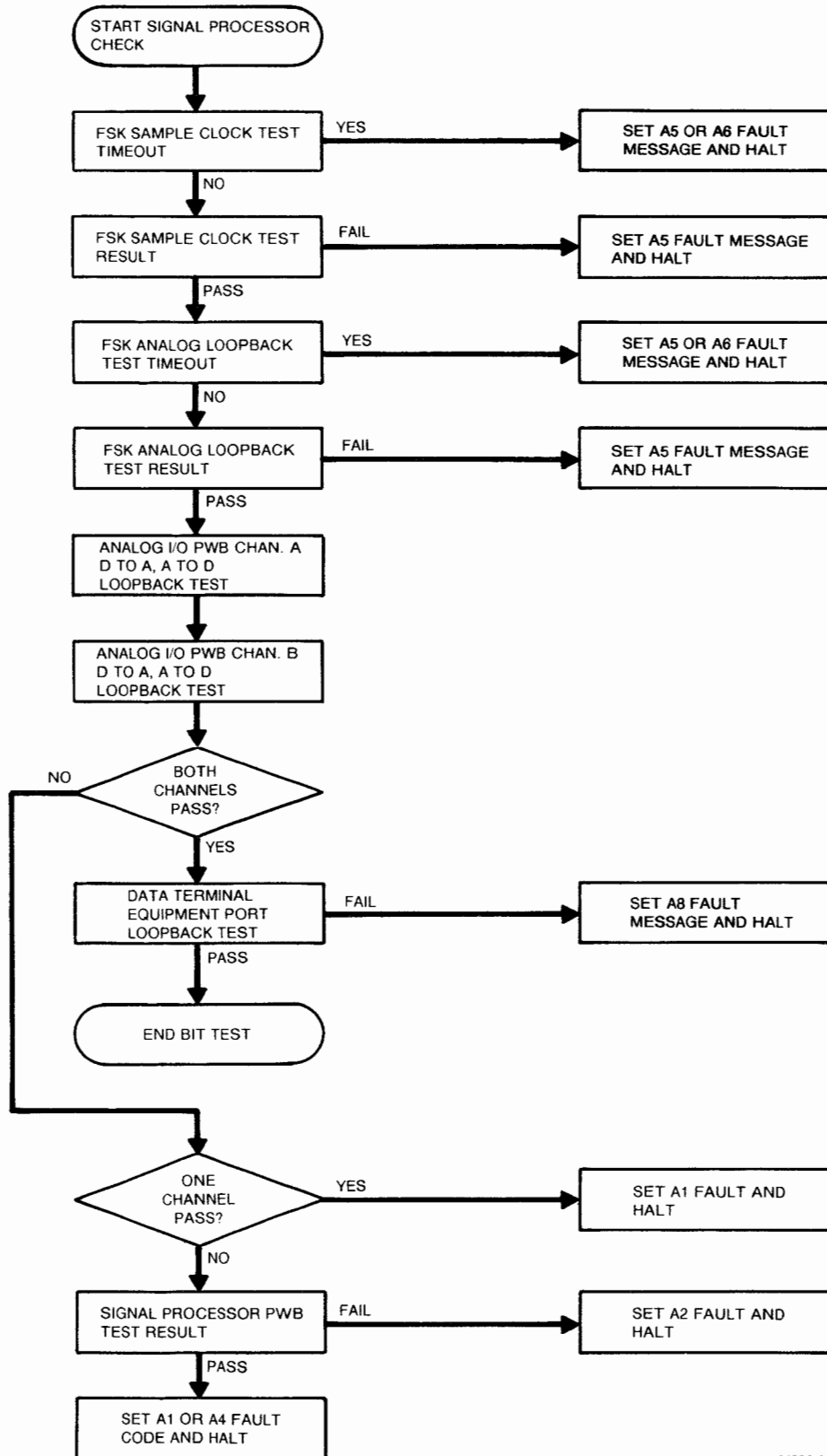
A power supply failure can be suspected if the front panel does not light when the POWER switch is in the ON position.

The Rear Panel assembly A12 forms the interface between the modem and the transmitter, receiver, data terminal equipment, and remote control unit. Problems with signal transmission between the modem and any of the other units may be in the Rear Panel assembly. Use standard signal tracing techniques to isolate signal transmission problems. Replace the Rear Panel assembly as required.



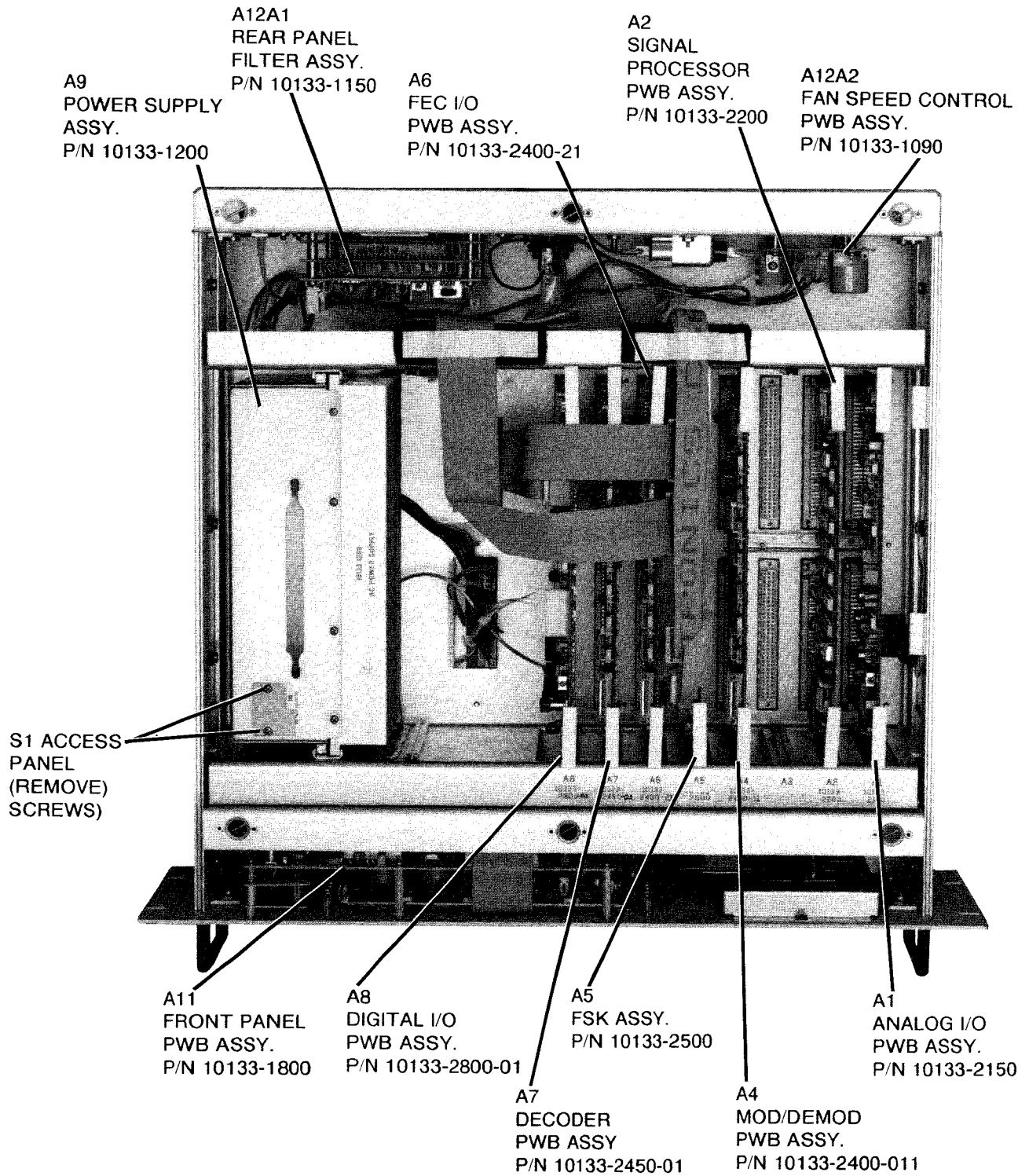
3466A-017

Figure 5-1. BIT Memory Check



3466A-018

Figure 5-2. BIT Signal Processing Tests



3466A-010(P)

Figure 5-3. RF-3466A Assembly Locations

Cooling fan failures can be attributed to the fan itself or the Fan Speed Control PWB assembly A12A2. If the fan fails to operate, first check for the presence of a proper voltage across the fan's power inputs. If the voltage is present, replace the fan. If the supply voltage is absent, replace the Fan Speed Control PWB assembly A12A2.

### 5.4.3 Front Panel

If the power supply is operational and the unit will not function, the fault may be on the front panel. The Front Panel assembly A11 can be tested by pressing and holding the TEST pushbutton and then turning the unit on. During the test, the operator will be prompted to press any key. Pressing a key will cause the display to be filled with two lines of 20 letters. All of the letters should be the same. Each key on the RF-3466A will produce a different letter when pressed. To end this test, turn power off.

If test does not appear to be running at all and the power supply has been checked, the most likely source of the problem is the Logic/Clock assembly A11A1.

If the display does not show intelligible messages, but at one point during the test all of the LEDs turn on and then go off, the most likely source of the problem is the Display Module A11A3.

If when pressing the keys, one key does not cause a change in the letters displayed, then the most likely source of the problem is the Switch assembly A11A2.

## 5.5 REPLACEMENT PROCEDURES

### 5.5.1 General

All modules tested by the BIT can be accessed by removing the top cover. To replace A1, A2, A4, A5, A6, A7, or A8:

- Turn the POWER switch to the OFF position.
- Disconnect power cable from power source.
- Remove top cover.
- Lift defective module from card cage, noting position and orientation. (For A8, disconnect ribbon cable and coaxial connector prior to removal.)

#### NOTE

All modules are keyed for proper orientation and position. If insertion of the replacement module is difficult, check for proper slot location and orientation.

- Insert replacement module in the same slot.

## 5.5.2 Front Panel PWB (A11) Removal and Replacement Procedure

Refer to figure 5-4 for the following replacement procedures.

### 5.5.2.1 Front Panel Assembly Removal

- a. Place power switch in the OFF position.
- b. Disconnect power cable from power source.
- c. Remove top cover from unit.
- d. Remove the four screws that secure the front panel to the chassis.
- e. Pull the front panel forward.

### 5.5.2.2 A11A1 PWB Removal and Replacement Procedure

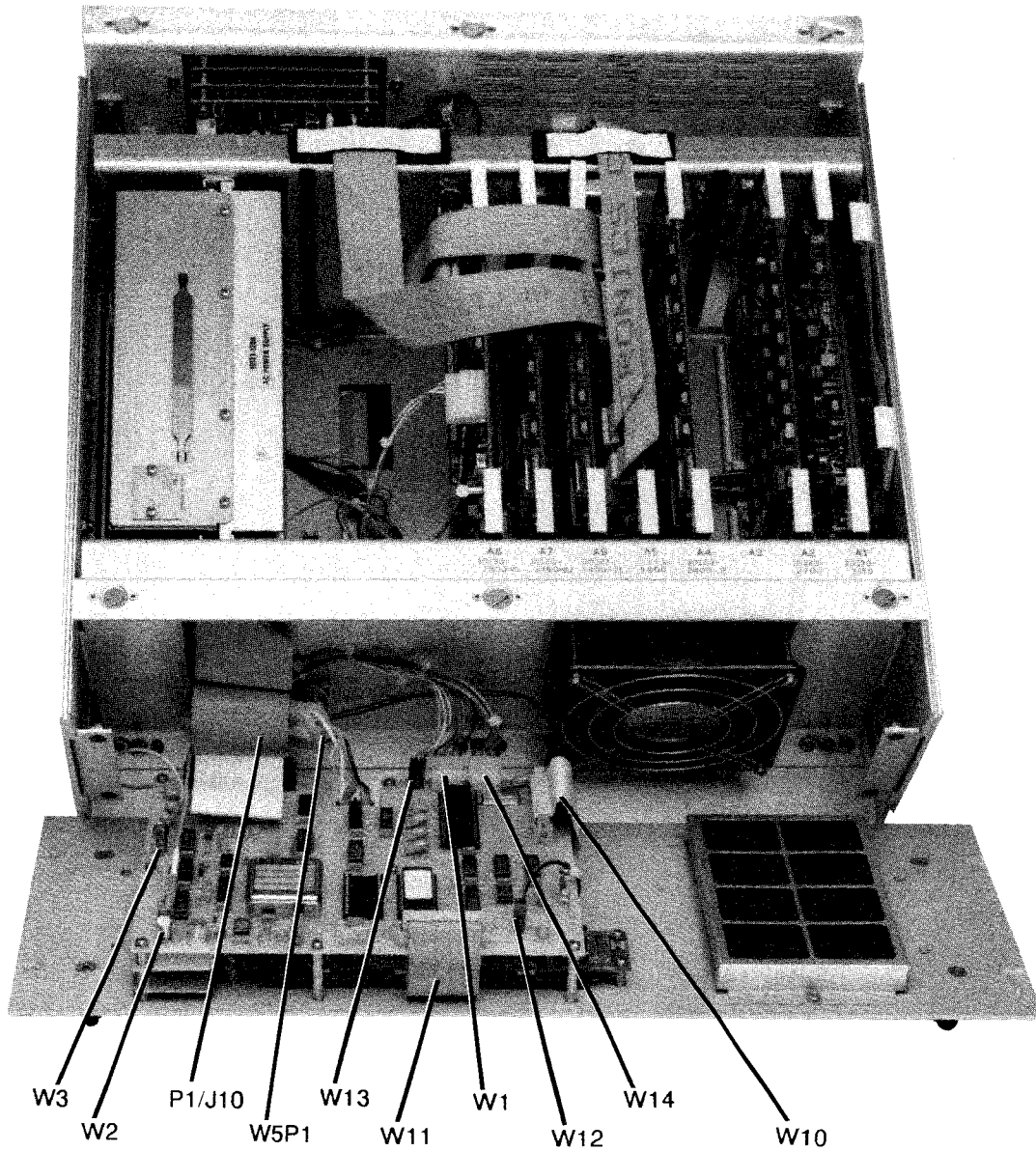
- a. Disconnect cables W1, W2, W3, W5, W10, W11, W12, W13, W14, and connector P1 from J10.
- b. Remove screws that secure Logic/Clock assembly A11A1 to the front panel.
- c. Remove PWB assembly, noting position and orientation.
- d. If A11A1 was the faulty module, go to paragraph 5.5.2.5; otherwise proceed to paragraph 5.5.2.3 for replacement of A11A2 assembly or paragraph 5.5.2.4 for replacement of A11A3 assembly.

### 5.5.2.3 A11A2 PWB Removal and Replacement Procedure

- a. Perform the steps in paragraph 5.5.2.2 for the removal of A11A1 PWB.
- b. Remove the screws that secure Switch assembly A11A2 to the front panel.
- c. Remove PWB assembly, noting position and orientation.
- d. Position replacement module on the front panel.
- e. Secure PWB assembly to front panel with screws removed in step b.

### 5.5.2.4 A11A3 PWB Removal and Replacement Procedure

- a. Perform the steps in paragraph 5.5.2.2 for the removal of A11A1 PWB.
- b. Remove the screws that secure Display assembly A11A3 to the front panel.
- c. Remove PWB assembly, noting position and orientation.
- d. Position replacement module on the front panel.
- e. Secure PWB assembly to front panel with screws removed in step b.



3466A-011(P)

Figure 5-4. Front Panel PWB Cable Connections

### 5.5.2.5 Front Panel Assembly Installation

- a. Position A11A1 module on the front panel
- b. Secure A11A1 assembly to front panel with screws removed in step b. of paragraph 5.5.2.2.
- c. Connect cables W1, W2, W3, W5, W10, W11, W12, W13, W14, and plug connector P2 to J10.
- d. Secure the front panel to the chassis with screws removed in step d. of paragraph 5.5.2.1.
- e. Restore power to the modem.

### 5.5.3 Rear Panel Filter Assembly Removal and Replacement

- a. Turn POWER off and disconnect cables from J1, J3, J4, and J5 at rear of modem.
- b. Remove the four screws that secure the filter assembly to the rear panel (see figure 5-5).

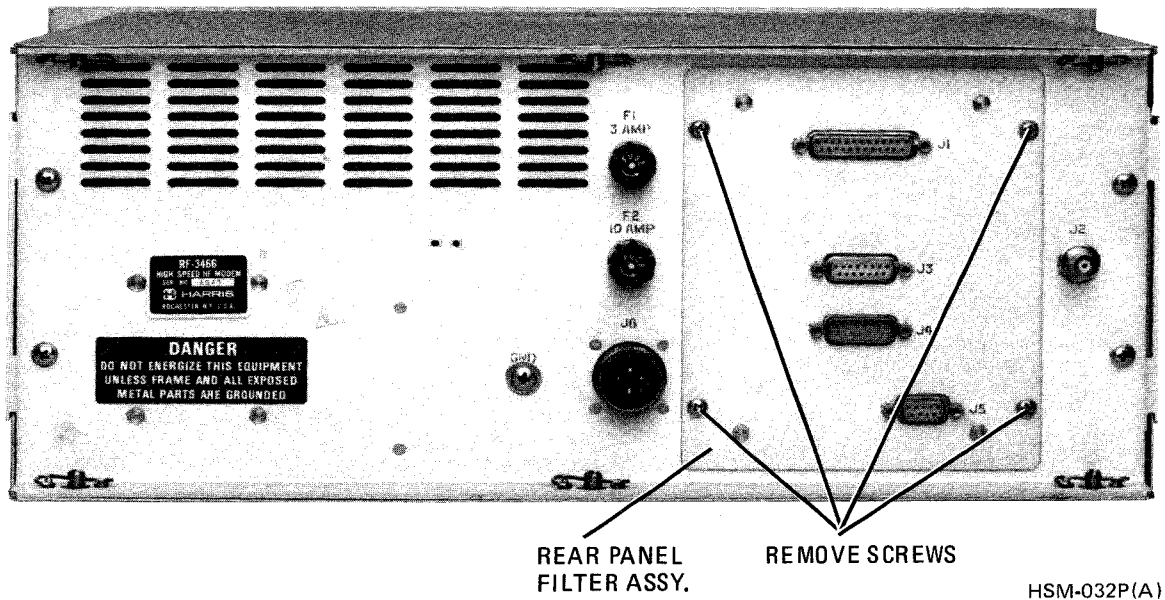


Figure 5-5. Filter Assembly Location and Removal

- c. Disconnect cables W1 and W2 and connector A10P2 from the filter assembly.
- d. Remove assembly.
- e. Position replacement assembly and connect cables W1 and W2, and connector A10P2.

- f. Secure the filter assembly to the rear panel with the screws removed in step b.
- g. Connect cables disconnected in step a and restore power to the modem.

#### **5.5.4 Cooling Fan Removal and Replacement**

- a. Turn POWER switch to the OFF position.
- b. Remove the four screws that secure the Front Panel assembly to the chassis.
- c. Pull the Front Panel assembly forward and position it so the fan can be accessed.
- d. Disconnect the red and black wires from the fan.
- e. Remove the four screws that secure the fan to the card cage.
- f. Separate the screen from the fan and position it on the replacement fan.
- g. Secure the replacement fan and the protective screen to the card cage with the screws removed in step b.
- h. Connect the red and black wires to the fan. Make sure the wires are connected to the correct terminals.
- i. Replace the front panel and secure it to the chassis using the screws removed in step b.
- j. Restore power to the modem and make sure air is being pulled through the filter. If not, turn power off, remove the front panel, and reverse the red and black wires.

#### **5.5.5 Fan Speed Control PWB Assembly Removal and Replacement**

- a. Turn POWER switch to the OFF position.
- b. Remove the top and bottom covers.
- c. Remove the four screws that secure the rear panel to the chassis.
- d. Tilt the rear panel to expose the Fan Speed Control PWB (see figure 5-6).
- e. Disconnect W6P1 from J1 and A9P3 from J2.
- f. Remove the four screws that secure the Fan Speed Control PWB to the rear panel (see figure 5-6).
- g. Remove the defective assembly.
- h. Position the replacement assembly on the rear panel and secure it with the four screws removed in step f.
- i. Connect W6P1 to J1 and A9P3 to J2 (see figure 5-6).
- j. Replace the Rear Panel assembly and secure it to the chassis with the screws removed in step c.
- k. Replace the top and bottom covers.

- l. Turn the POWER switch to the ON position.
- m. Make sure the fan is operating correctly.

#### **5.5.6 Power Supply Removal and Replacement**

- a. Turn POWER switch to OFF position.
- b. Remove the top cover.
- c. Disconnect P2 from J17 on A10, P2 from P1 at rear panel, and P3 from P2 on A2 (see figure 5-7).
- d. Loosen the two screws that hold the power supply in place. These screws are captive and cannot be removed completely (see figure 5-7).
- e. Lift the power supply from the chassis.
- f. Slide replacement into chassis and tighten the two screws.
- g. Reconnect cables disconnected in step c.
- h. Replace top cover and restore power to unit.

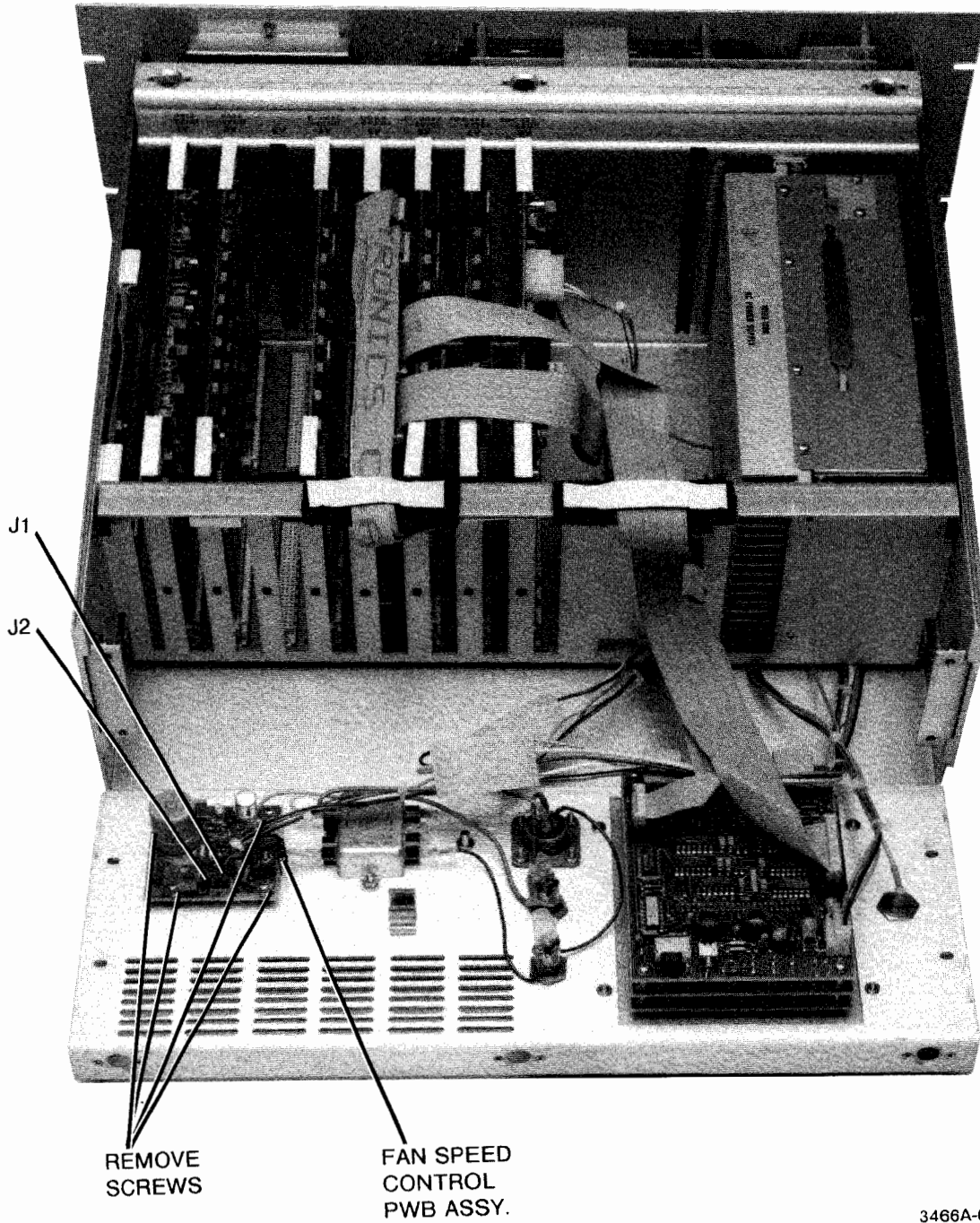
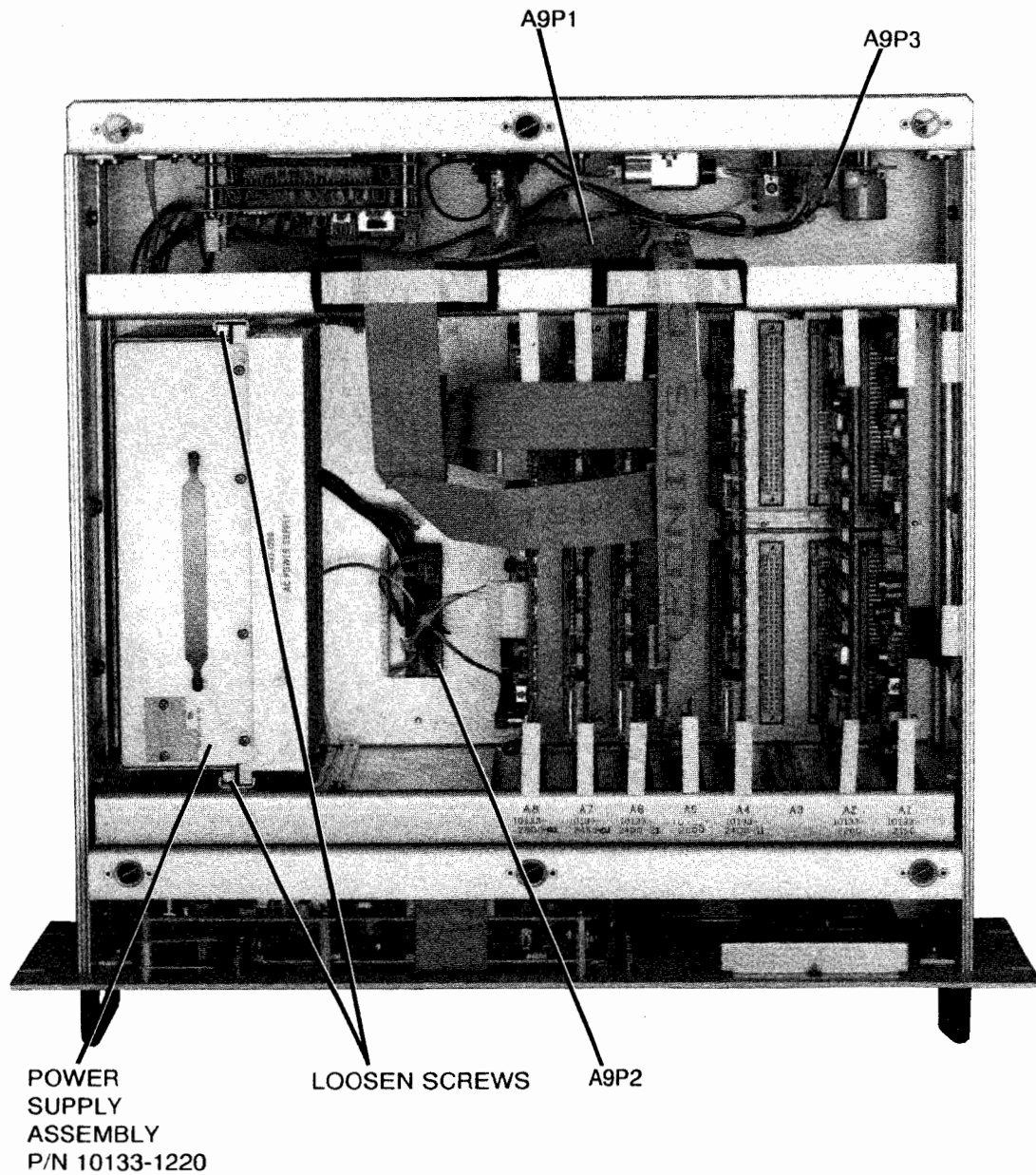


Figure 5-6. Fan Speed Control PWB Removal and Replacement



3466A-013(P)

Figure 5-7. Power Supply Removal and Replacement

**SECTION 6****PARTS LISTS, COMPONENT LOCATION DIAGRAMS, AND SCHEMATIC DIAGRAMS****6.1 INTRODUCTION**

This section contains parts lists, component location diagrams, and schematic diagrams for all major assemblies of the modem. The documents are arranged in alphanumeric order using the reference designators of the assemblies.

Users of these documents are cautioned that troubleshooting microprocessor-based circuits is difficult and requires special equipment and procedures. Troubleshooting should be attempted only by an experienced digital electronics technician with a properly equipped workstation and a working knowledge of the modem's operating software.

**Table 6-1. Main Chassis Assembly (10133-3500, Rev. B) Parts List**

Ref. Desig.	Part Number	Description
A1	10133-2150	ANALOG I/O PWB ASSY
A2	10133-2200	SIGNAL PROCESSOR PWB ASSY
A4	10133-2400-011	MOD/DEMOD PWB ASSY
A5	10133-2500-01	FSK PWB ASSY
A6	10133-2400-021	FEC I/O PWB ASSY
A7	10133-2450-01	DECODER PWB ASSY
A8	10133-2800-01	DIGITAL I/O PWB ASSY
A9	10133-1200	POWER SUPPLY ASSY
A10	10133-2900-01	INTERCONNECT PWB ASSY
A11	10133-1800	FRONT PANEL ASSY
A12	10133-1009	REAR PANEL ASSY
B1	B22-0007-001	FAN, 12V
W1	10133-4010	CBL ASSY
W2	10133-4014	CBL ASSY
W3	10133-4015	CBL ASSY
W5	10133-4016	CB, ASSY
W6	10133-4017	CBL ASSY
W7	10133-4018	CBL ASSY
W8	10133-4019	CBL ASSY
W9	10133-4020	CBL ASSY
W13	10133-4024	CBL ASSY
W14	10133-4025	CBL ASSY

- NOTES:  
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT  
NO. AND/OR ASSEMBLY NO. DESIGNATION.  
2. SEE 10133-2901 SCHEMATIC FOR ALL CONNECTOR FUNCTIONS  
NOT SHOWN IN A10 INTERCONNECT PWB.

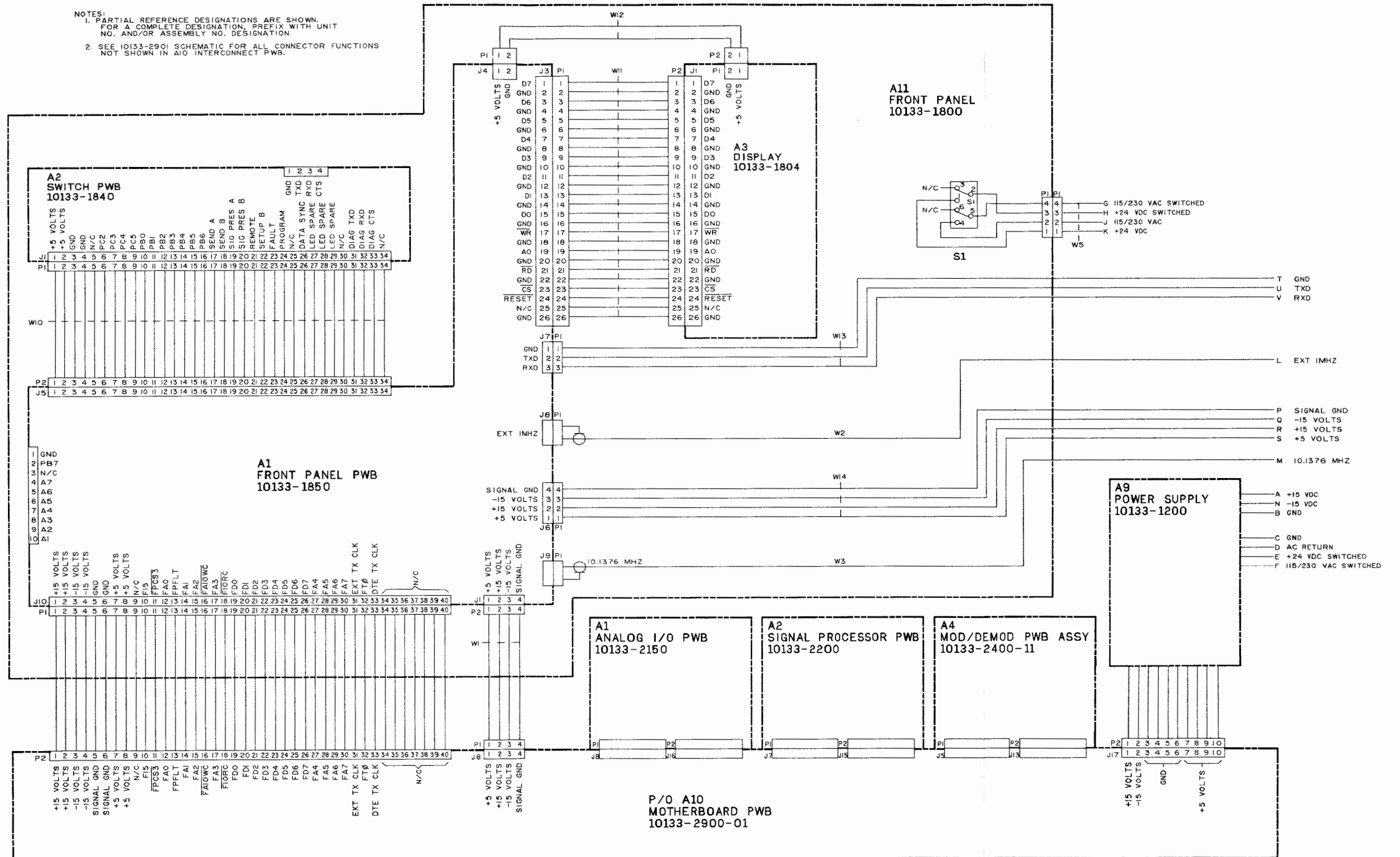


Figure 6-1. Main Chassis Interconnection Schematic Diagram (10133-3501, Rev. B) (Sheet 1 of 2)

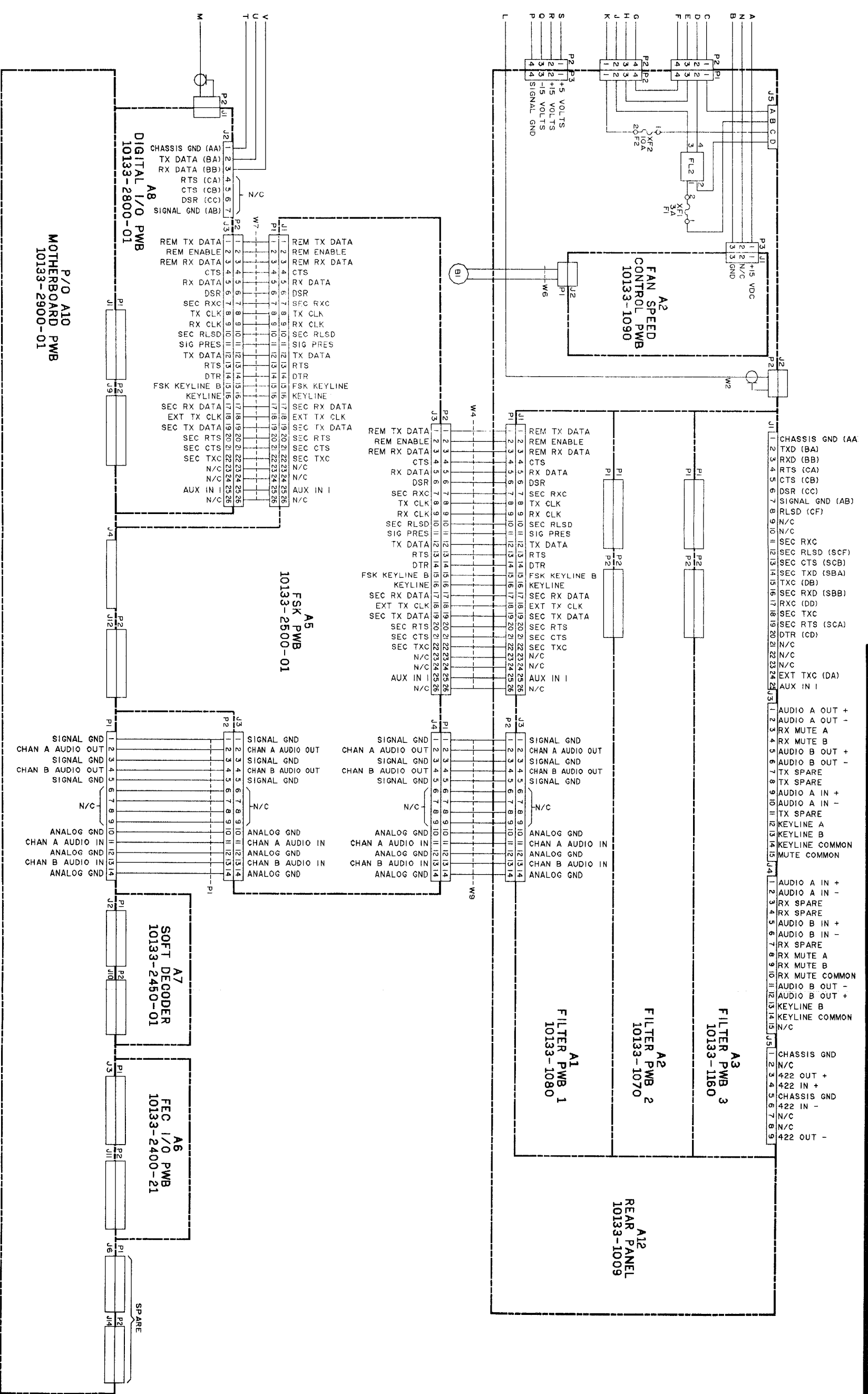


Figure 6-1. Main Chassis Interconnection Schematic Diagram (10133-3501, Rev. B) (Sheet 2 of 2)

Table 6-2. Analog I/O PWB Assembly A1 (10133-2150, Rev. N) Parts List

Ref. Desig.	Part Number	Description
	Z71-0001-001	CARD EXTRACTOR
	J46-0047-003	HEADER, 3 POS
C1	C10-0003-012	CAP, .1UF
C2	C10-0003-012	CAP, .1UF
C3	C10-0003-012	CAP, .1UF
C4	C10-0003-012	CAP, .1UF
C5	C10-0003-012	CAP, .1UF
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C10-0003-012	CAP, .1UF
C12	C10-0003-012	CAP, .1UF
C13	C10-0003-012	CAP, .1UF
C14	C10-0003-012	CAP, .1UF
C15	C10-0003-012	CAP, .1UF
C16	C10-0003-012	CAP, .1UF
C17	C10-0003-012	CAP, .1UF
C18	C10-0003-012	CAP, .1UF
C19	C10-0003-012	CAP, .1UF
C20	C10-0003-012	CAP, .1UF
C21	C10-0003-012	CAP, .1UF
C22	C10-0003-012	CAP, .1UF
C23	C10-0003-012	CAP, .1UF
C24	C10-0003-012	CAP, .1UF
C25	C10-0003-012	CAP, .1UF
C26	C10-0003-012	CAP, .1UF
C27	C10-0003-012	CAP, .1UF
C28	C10-0003-012	CAP, .1UF
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	C10-0003-012	CAP, .1UF
C33	C10-0003-012	CAP, .1UF
C34	C10-0003-012	CAP, .1UF
C35	M39014/02-1310	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	C10-0003-012	CAP, .1UF
C38	C25-0001-301	CAP 1.0UF 20% 20V TANT
C39	C10-0003-012	CAP, .1UF
C40	C25-0001-301	CAP 1.0UF 20% 20V TANT
C41	C25-0001-301	CAP 1.0UF 20% 20V TANT
C42	C25-0001-301	CAP 1.0UF 20% 20V TANT
C43	C25-0001-301	CAP 1.0UF 20% 20V TANT

Table 6-2. Analog I/O PWB Assembly A1 (10133-2150, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
C44	C61-0007-013	CAP .001UF 10% 100
C45	C10-0003-012	CAP, .1UF
C46	C10-0003-012	CAP, .1UF
C47	C10-0003-012	CAP, .1UF
C48	C26-0035-220	CAP 22UF 20% 35V TANT
C49	C26-0035-220	CAP 22UF 20% 35V TANT
C50	C26-0035-220	CAP 22UF 20% 35V TANT
C51	C10-0003-011	CAP, .01UF
C52	C10-0003-011	CAP, .01UF
C53	M39014/02-1318	CAP .33UF 10% 50V CER
C54	C26-0035-220	CAP 22UF 20% 35V TANT
C55	C26-0035-220	CAP 22UF 20% 35V TANT
C56	C26-0035-220	CAP 22UF 20% 35V TANT
C57	M39014/02-1320	CAP .47UF 10% 50V CER-R
C58	M39014/02-1320	CAP .47UF 10% 50V CER-R
C59	C10-0003-012	CAP, .1UF
C60	M39014/02-1318	CAP .33UF 10% 50V CER
C61	M39014/02-1320	CAP .47UF 10% 50V CER-R
C62	M39014/02-1320	CAP .47UF 10% 50V CER-R
C63	C10-0003-012	CAP, .1UF
C64	C10-0003-012	CAP, .1UF
C67	C10-0003-012	CAP, .1UF
C68	C10-0003-012	CAP, .1UF
C70	C25-0001-301	CAP 1.0UF 20% 20V TANT
C71	C10-0003-012	CAP, .1UF
C72	M39014/02-1320	CAP .47UF 10% 50V CER-R
C73	M39014/02-1320	CAP .47UF 10% 50V CER-R
C74	M39014/02-1320	CAP .47UF 10% 50V CER-R
C75	M39014/02-1320	CAP .47UF 10% 50V CER-R
CR1	1N4742A	ZENER,12V
CR2	1N5231B	DIODE 5.1V 5% 0.5W ZENER
CR3	1N6263	DIODE,HOT CARRIER
CR4	1N6263	DIODE,HOT CARRIER
CR5	1N6263	DIODE,HOT CARRIER
CR6	1N6263	DIODE,HOT CARRIER
CR7	1N6263	DIODE,HOT CARRIER
DS1	N21-0008-000	DIODE, LIGHT EMITTING
P1	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
P2	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-621	RES,620 5% 1/4W CAR FILM
R2	R65-0003-621	RES,620 5% 1/4W CAR FILM
R3	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R4	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R5	RN55D4641F	RES,4640 1% 1/8W MET FLM
R6	RN55D4641F	RES,4640 1% 1/8W MET FLM
R7	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R8	R65-0003-103	RES,10K 5% 1/4W CAR FILM

Table 6-2. Analog I/O PWB Assembly A1 (10133-2150, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R9	R65-0003-822	RES,8.2K 5% 1/4W CAR FILM
R10	R65-0003-822	RES,8.2K 5% 1/4W CAR FILM
R11	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R12	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R13	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R14	R65-0003-473	RES,47K 5% 1/4W CAR FILM
R15	RN55D1502F	RES,15.0K 1% 1/8W MET FLM
R16	RN55D3922F	RES,39.2K 1% 1/8W MET FLM
R17	R65-0003-473	RES,47K 5% 1/4W CAR FILM
R18	RN55D1502F	RES,15.0K 1% 1/8W MET FLM
R19	RN55D3922F	RES,39.2K 1% 1/8W MET FLM
R20	R65-0003-134	RES,130K 5% 1/4W CAR FILM
R21	R50-0010-123	RES,SIP, 12K 10PIN
R22	R30-0001-104	RES,VAR,100K 3/4W 20%
R23	R65-0003-561	RES,560 5% 1/4W CAR FILM
R24	R65-0003-561	RES,560 5% 1/4W CAR FILM
R25	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R26	R65-0003-133	RES,13K 5% 1/4W CAR FILM
R27	RN55D2432F	RES,24.3K 1% 1/8W MET FLM
R28	RN55D2432F	RES,24.3K 1% 1/8W MET FLM
R29	RN55D1622F	RES,16.2K 1% 1/8W MET FLM
R30	RN55D1622F	RES,16.2K 1% 1/8W MET FLM
R31	RCR07G562JM	RES,5.6K 5% 1/4W CAR COMP
R32	RCR07G181JM	RES,180 5% 1/4W CAR COMP
R33	RN55D1003F	RES,100K 1% 1/8W MET FLM
R34	RN55D1003F	RES,100K 1% 1/8W MET FLM
R35	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R36	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R37	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R38	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R39	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R40	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R41	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R42	R65-0003-154	RES,150K 5% 1/4W CAR FILM
R43	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R44	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R45	R30-0001-202	RES,VAR,2K 3/4W 20%
R46	RCR32G181JM	RES,180 5% 1W CAR COMP
R47	RCR20G470JM	RES,47 5% 1/2W CAR COMP
R48	R65-0003-121	RES,120 5% 1/4W CAR FILM
R49	RN55D4992F	RES, 49.9K 1% 1/8W MET FLM
R50	RN55D1001F	RES, 1.0K 1% 1/8W MET FLM
S1	S10-0026-001	SW,SP,ON-NONE-OFF,TOG,PCM
TP1	J65-0009-002	TEST POINT
TP2	J65-0009-002	TEST POINT
TP3	J65-0009-002	TEST POINT
TP4	J65-0009-002	TEST POINT
TP5	J65-0009-002	TEST POINT

Table 6-2. Analog I/O PWB Assembly A1 (10133-2150, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
TP6	J65-0009-002	TEST POINT
U1	I01-0000-252	IC 4053B PLASTIC CMOS
U2	I53-0004-001	INTEL PCM FILTER
U3	I53-0004-001	INTEL PCM FILTER
U4	I30-0038-002	IC LF347BN
U5	I13-0002-001	IC MULTIPLIER
U6	I13-0002-001	IC MULTIPLIER
U7	I30-0010-001	OP AMP
U8	I26-0015-001	AMD FIFO
U9	I26-0015-001	AMD FIFO
U10	I26-0015-001	AMD FIFO
U11	I15-0000-259	ADD ,LATCH
U12	I15-0000-138	IC 74HC138 PLASTIC CMOS
U13	I15-0000-368	IC 74HC368 PLASTIC CMOS
U14	I15-0000-386	EXCLUSIVE
U15	I09-0012-001	ANALOG DEV. ANALOG MUX
U16	I15-0000-004	IC 74HC04 PLASTIC CMOS
U17	I15-0000-163	BINARY COUNTER
U18	I03-0017-001	DAC
U19	I08-0001-000	IC 74120 PLASTIC TTL
U20	I08-0001-000	IC 74120 PLASTIC TTL
U21	I15-0000-164	SHIFT REGISTER
U22	I05-0000-244	IC 74LS244 PLASTIC TTL
U23	I05-0000-244	IC 74LS244 PLASTIC TTL
U24	I15-0000-008	IC 74HC08 PLASTIC CMOS
U25	I54-0002-001	SAMPLE AND HOLD
U26	I15-0000-074	IC 74HC74 PLASTIC CMOS
U27	I03-0016-001	A/D CONVERTER
U28	I64-0001-001	IC RMS TO DC CONVERTER

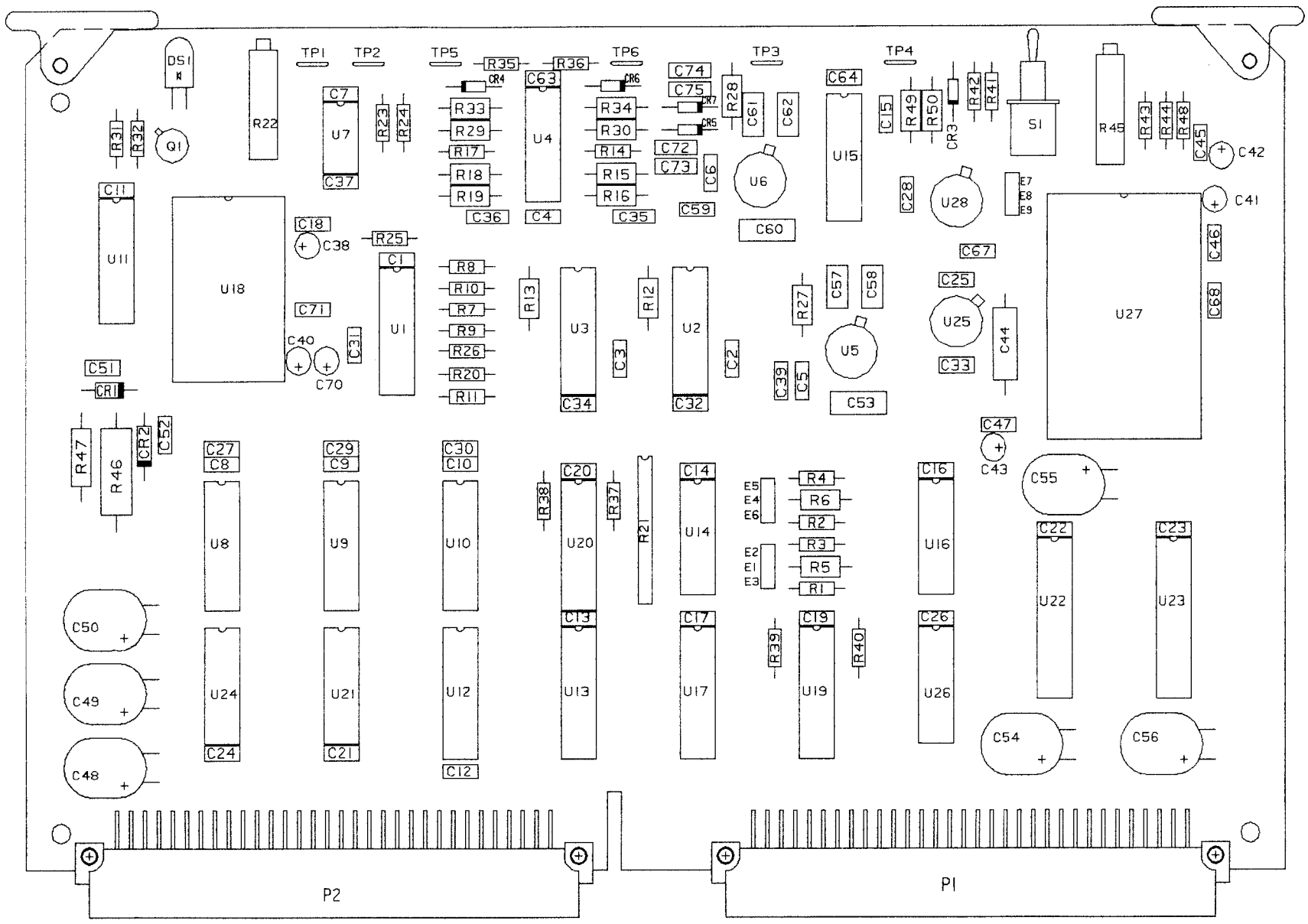
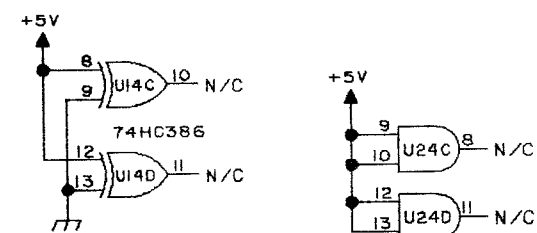


Figure 6-2. Analog I/O PWB Assembly A1 Component Locations (10133-2150, Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
- ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
- ALL CAPACITOR VALUES ARE IN MICROFARADS.
- VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
- FOR NORMAL INPUT AUDIO RANGE (-50DBM TO -25DBM), JUMPER E1 TO E2 AND E4 TO E5. FOR ALTERNATE INPUT AUDIO RANGE (-50DBM TO -35DBM), JUMPER E1 TO E3 AND E4 TO E6.
- JUMPER E7 TO E8 TO ENABLE MODEM AGC (NORMAL OPERATION). TO DISABLE MODEM AGC, JUMPER E8 TO E9. WHEN AGC IS DISABLED AND NORMAL INPUT AUDIO RANGE IS SELECTED (NOTE 5), A 0DBM NOMINAL INPUT LEVEL IS REQUIRED. ALTERNATELY, WHEN AGC IS DISABLED AND ALTERNATE INPUT AUDIO RANGE IS SELECTED, A -10DB NOMINAL INPUT LEVEL IS REQUIRED.



HIGHEST REFERENCE DESIGNATION				
C75	CR7	DS1	Q1	R48
SI	U28			
REFERENCE DESIGNATIONS NOT USED				
C65	C66	C69		

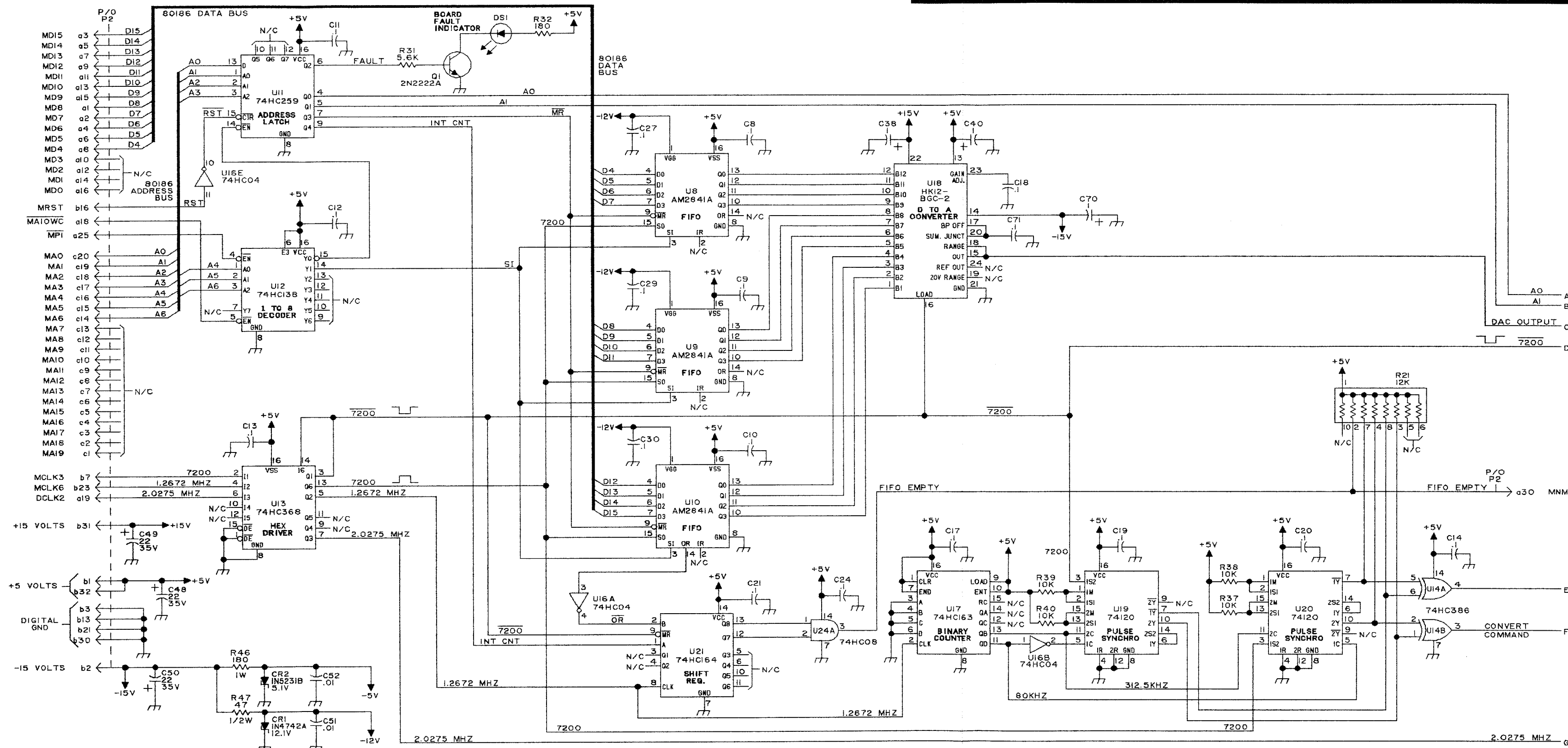


Figure 6-3. Analog I/O PWB Assembly A1 Schematic Diagram (10133-2151, Rev. F) (Sheet 1 of 2)

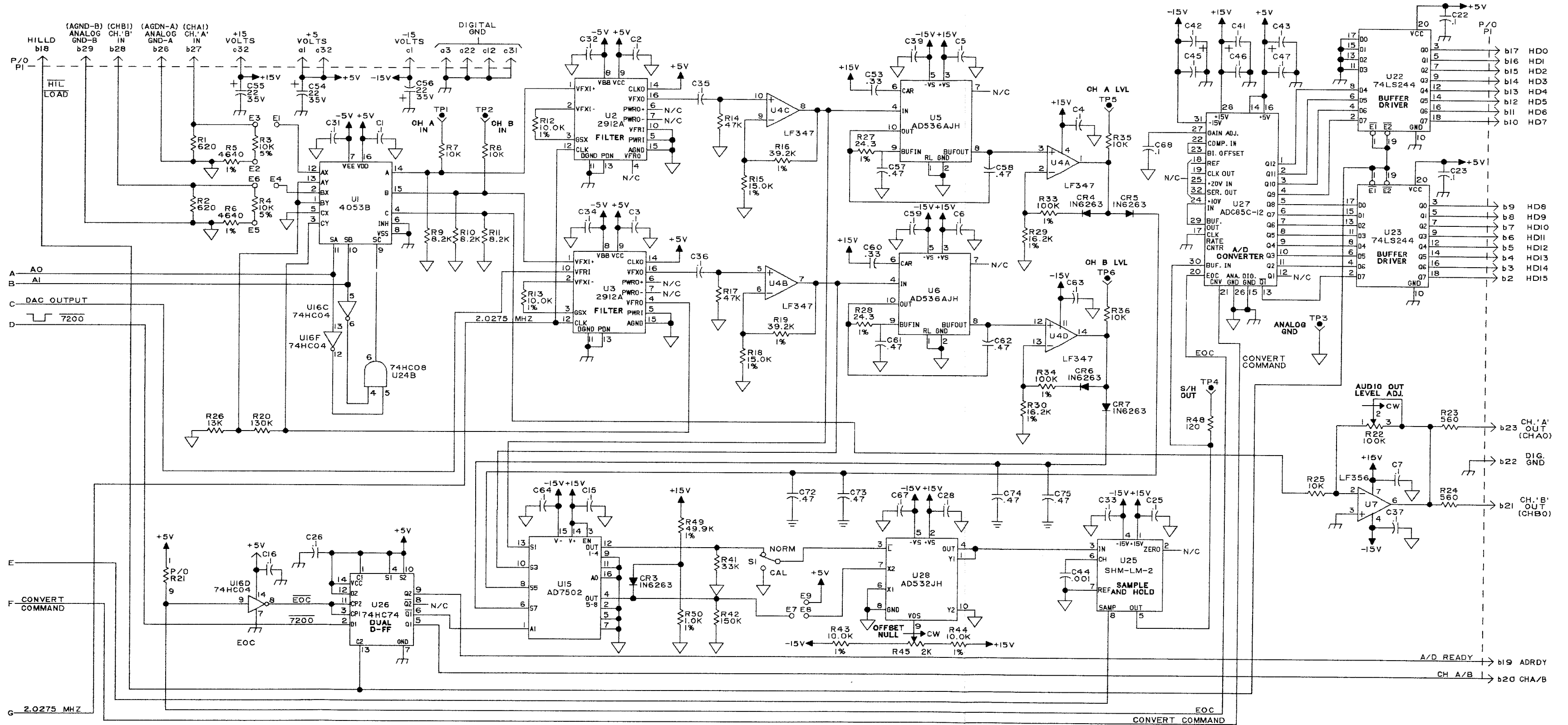


Figure 6-3. Analog I/O PWB Assembly A1 Schematic Diagram (10133-2151, Rev. F) (Sheet 2 of 2)

Table 6-3. Signal Processor PWB Assembly A2 (10133-2200, Rev. N) Parts List

Ref. Desig.	Part Number	Description
	Z71-0001-001	CARD EXTRACTOR
	J46-0047-003	HEADER, 3 POS
C1	C10-0003-012	CAP, .1UF
C2	C10-0003-012	CAP, .1UF
C3	C10-0003-012	CAP, .1UF
C4	C10-0003-012	CAP, .1UF
C5	C10-0003-012	CAP, .1UF
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C10-0003-012	CAP, .1UF
C12	C10-0003-012	CAP, .1UF
C13	C10-0003-012	CAP, .1UF
C14	C10-0003-012	CAP, .1UF
C15	C10-0003-012	CAP, .1UF
C16	C10-0003-012	CAP, .1UF
C17	C10-0003-012	CAP, .1UF
C18	C10-0003-012	CAP, .1UF
C19	C10-0003-012	CAP, .1UF
C20	C10-0003-012	CAP, .1UF
C21	C10-0003-012	CAP, .1UF
C22	C10-0003-012	CAP, .1UF
C23	C10-0003-012	CAP, .1UF
C24	C10-0003-012	CAP, .1UF
C25	C10-0003-012	CAP, .1UF
C26	C10-0003-012	CAP, .1UF
C27	C10-0003-012	CAP, .1UF
C28	C10-0003-012	CAP, .1UF
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	C10-0003-012	CAP, .1UF
C33	C10-0003-012	CAP, .1UF
C34	C10-0003-012	CAP, .1UF
C35	C10-0003-012	CAP, .1UF
C36	C10-0003-012	CAP, .1UF
C37	C10-0003-012	CAP, .1UF
C38	C10-0003-012	CAP, .1UF
C39	C10-0003-012	CAP, .1UF
C40	CK05BX100K	CAP 10PF 10% 200V CER
C41	CK05BX100K	CAP 10PF 10% 200V CER
C42	C26-0035-220	CAP 22UF 20% 35V TANT
C43	C26-0035-220	CAP 22UF 20% 35V TANT
C44	CK05BX100K	CAP 10PF 10% 200V CER
C45	CK05BX100K	CAP 10PF 10% 200V CER

Table 6-3. Signal Processor PWB Assembly A2 (10133-2200, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
DS1	N21-0008-000	DIODE, LIGHT EMITTING
P1	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
P2	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R50-0010-102	RESISTOR,1K, SIP
R3	RCR07G562JM	RES,5.6K 5% 1/4W CAR COMP
R4	RCR07G181JM	RES,180 5% 1/4W CAR COMP
R5	R50-0010-123	RES,SIP, 12K 10PIN
R6	R50-0010-123	RES,SIP, 12K 10PIN
R7	R50-0010-123	RES,SIP, 12K 10PIN
R8	R50-0006-123	RES,SIP,12K, 6PIN
R9	R50-0006-123	RES,SIP,12K, 6PIN
R10	R50-0006-123	RES,SIP,12K, 6PIN
R11	R50-0010-123	RES,SIP, 12K 10PIN
R12	R50-0010-123	RES,SIP, 12K 10PIN
R13	R50-0010-123	RES,SIP, 12K 10PIN
U1	I27-0010-001	DIGITAL SIGNAL PROCESSOR
U2	I27-0010-001	DIGITAL SIGNAL PROCESSOR
U3,U4	*SEE NOTE	
U7,U8	*SEE NOTE	
U11	I15-0000-244	IC 74HC244 PLASTIC CMOS
U12	I15-1000-259	IC,74HCT259
U13	I15-0000-374	IC 74HC374 PLASTIC CMOS
U14	I15-0000-374	IC 74HC374 PLASTIC CMOS
U15	I05-0000-352	74LS352
U16	I15-0000-352	IC,DUAL 4 TO 1 MUX
U17	10075-1025	74S74
U18	I15-1000-074	IC,74HCT74
U19	I15-1000-374	IC,74HCT374
U20	I15-1000-374	IC,74HCT374
U21	I15-1000-374	IC,74HCT374
U22	I15-1000-374	IC,74HCT374
U23	I15-1000-374	IC,74HCT374
U24	I15-1000-374	IC,74HCT374
U25	I15-1000-374	IC,74HCT374
U26	I15-1000-374	IC,74HCT374
U27	I15-0000-138	IC 74HC138 PLASTIC CMOS
U28	I15-0000-138	IC 74HC138 PLASTIC CMOS
U29	I15-0000-074	IC 74HC74 PLASTIC CMOS
U30	IC-0314	SN7425N
U31	10075-1023	74S05
U32	I15-0000-032	IC 74HC32 PLASTIC CMOS
U33	I15-0000-032	IC 74HC32 PLASTIC CMOS
U34	10075-1024	74S32
U35	I15-0000-138	IC 74HC138 PLASTIC CMOS
U36	10075-1024	74S32
U37	10075-1022	IC,74S02
U38	I15-0000-074	IC 74HC74 PLASTIC CMOS

\*NOTE: When ordering replacement PROMs, refer to the part number (P/N) and the four-digit firmware number located on the PROM label.

Table 6-3. Signal Processor PWB Assembly A2 (10133-2200, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
U39	I15-0000-074	IC 74HC74 PLASTIC CMOS
U40	I15-0000-974	IC 74HCT74 PLASTIC CMOS
XU1	J77-0008-007	SOCKET, 40PIN
XU2	J77-0008-007	SOCKET, 40PIN
XU3	J77-0008-005	SOCKET, 24PIN
XU4	J77-0008-005	SOCKET, 24PIN
XU5	J77-0008-005	SOCKET, 24PIN
XU6	J77-0008-005	SOCKET, 24PIN
XU7	J77-0008-005	SOCKET, 24PIN
XU8	J77-0008-005	SOCKET, 24PIN
XU9	J77-0008-005	SOCKET, 24PIN
XU10	J77-0008-005	SOCKET, 24PIN
Y1	Y15-0004-200	CRYSTAL (SERIES) 20 MHZ
Y2	Y15-0004-200	CRYSTAL (SERIES) 20 MHZ

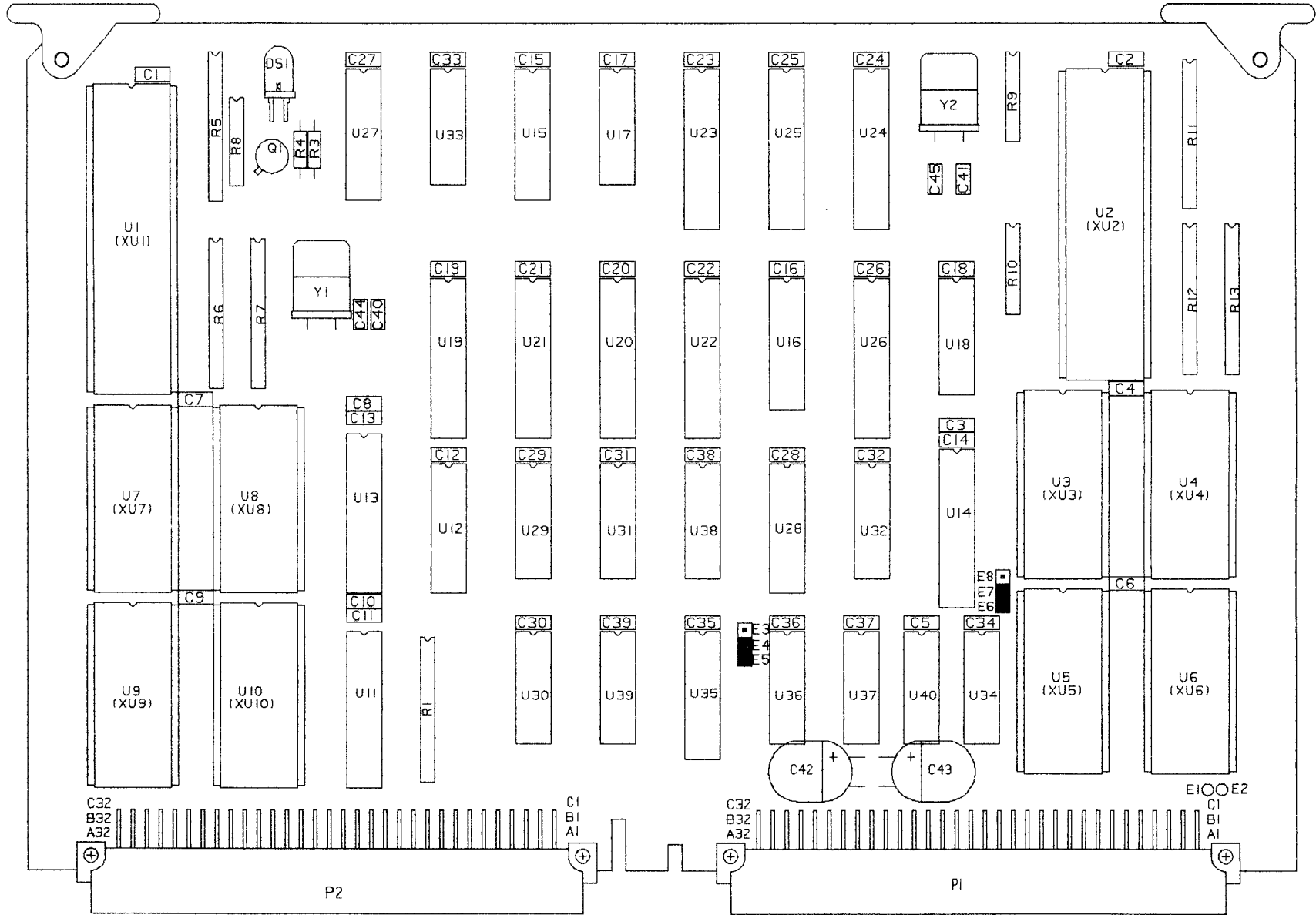


Figure 6-4. Signal Processor PWB Assembly A2 Component Locations (10133-2200, Rev. E)

- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  5. WHEN USING THIS ASSY WITH A REVISION 'A' 10133-2400-1 A4 ASSY, JUMPER E6 TO E7, AND E4 TO E5. FOR USE WITH REVISION 'B' 10133-2400-1 A4 ASSY AND UP, JUMPER E7 TO E8 AND E3 TO E4.

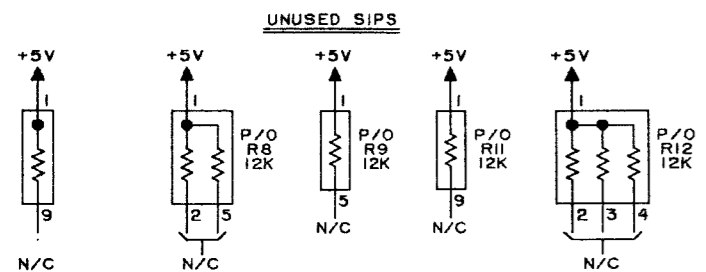


TABLE 1

FUNCTION	USED	NOT USED
SPARE	NONE	E1 TO E2

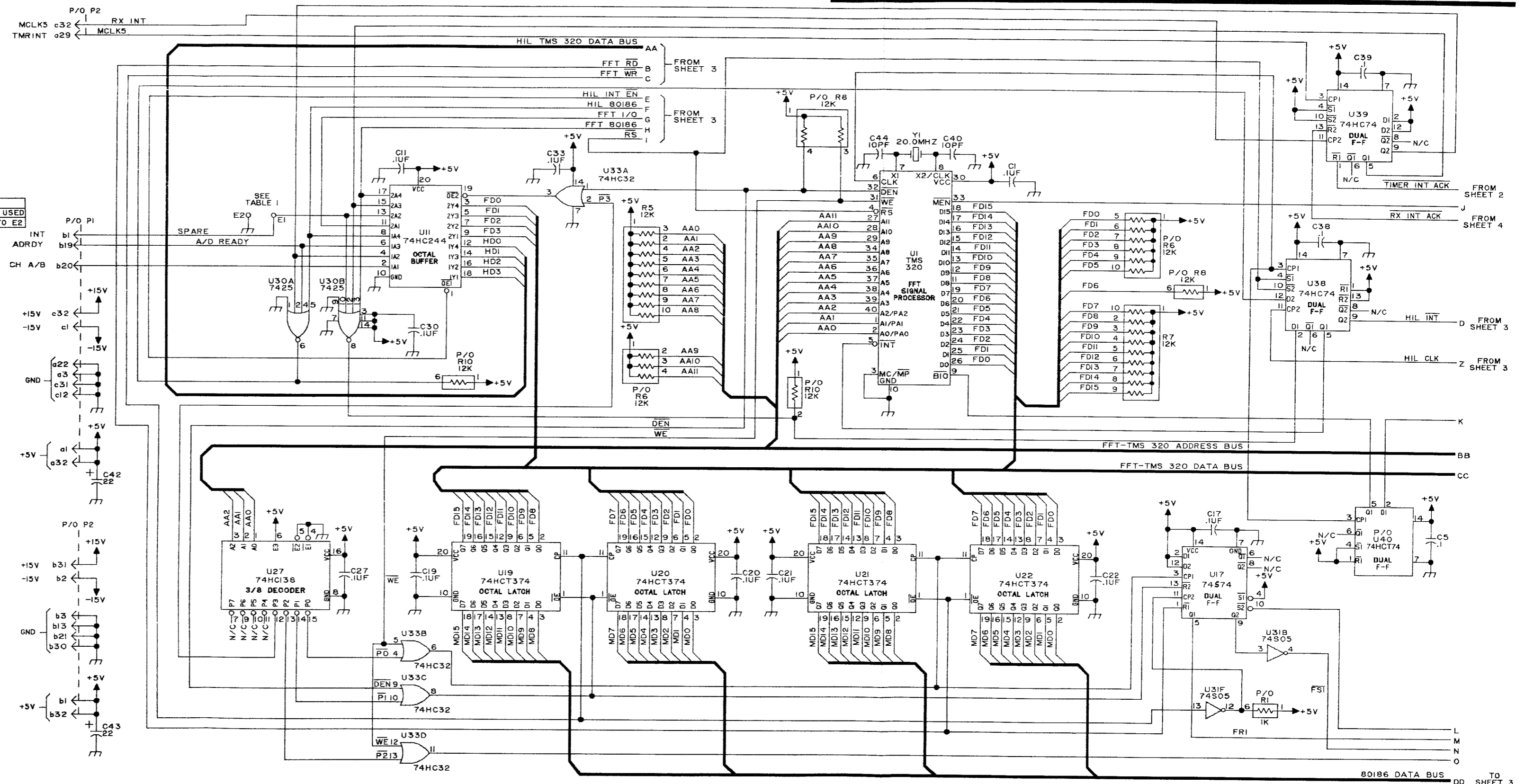
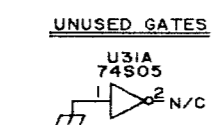


Figure 6-5. Signal Processor PWB Assembly A2 Schematic Diagram (10133-2201, Rev. F) (Sheet 1 of 4)

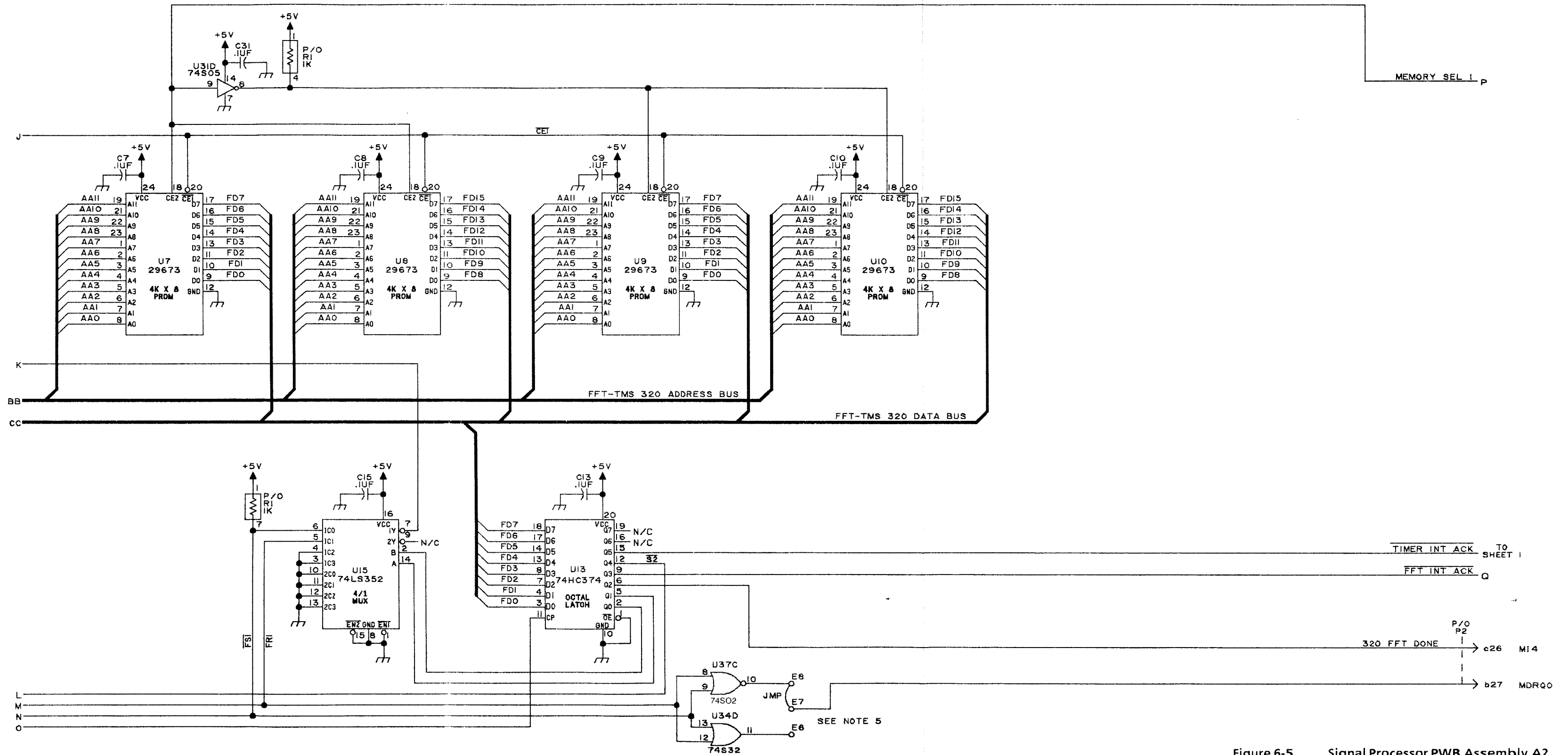


Figure 6-5. Signal Processor PWB Assembly A2 Schematic Diagram (10133-2201, Rev. F) (Sheet 2 of 4)

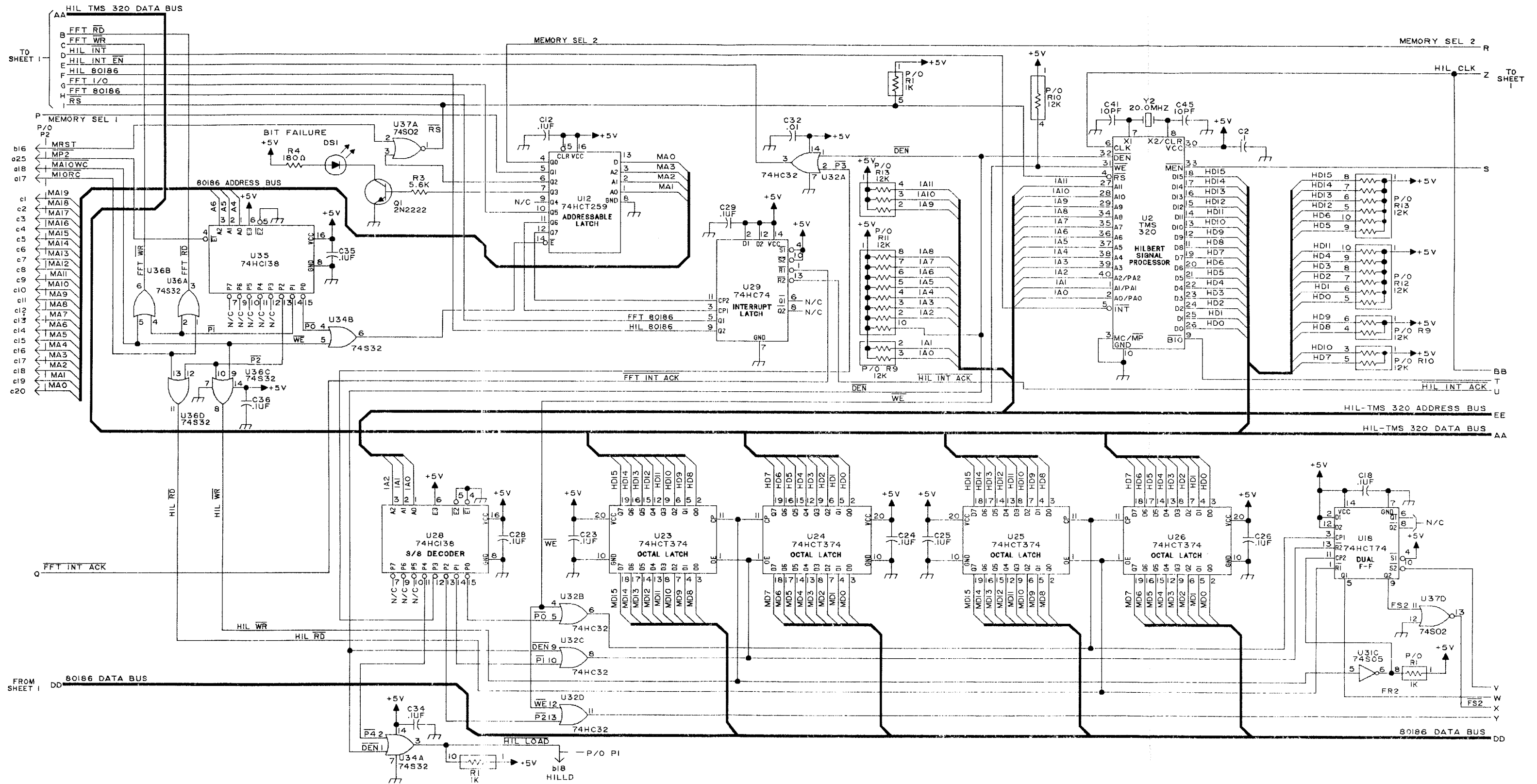


Figure 6-5. Signal Processor PWB Assembly A2 Schematic Diagram (10133-2201, Rev. F) (Sheet 3 of 4)

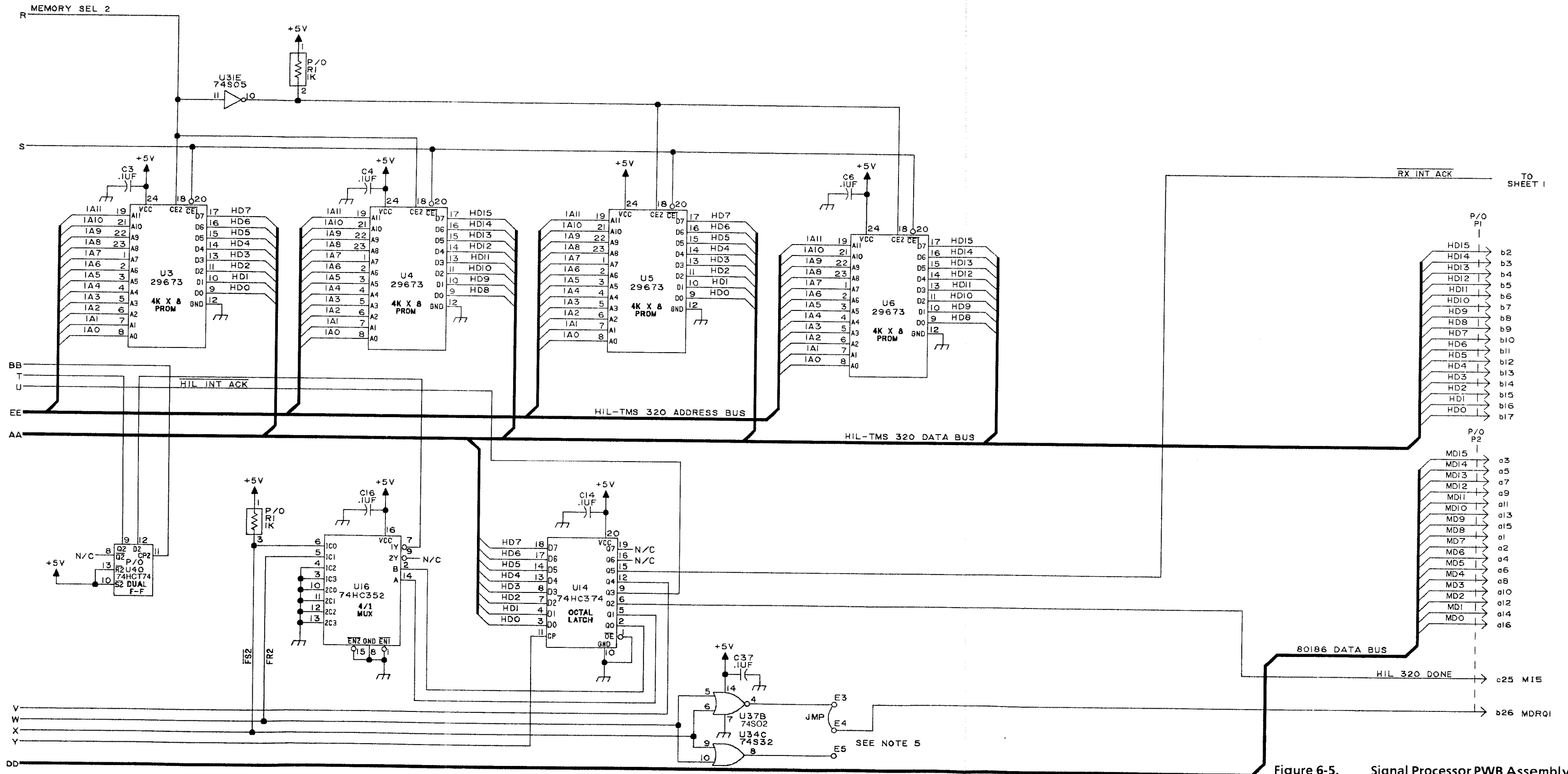


Figure 6-5. Signal Processor PWB Assembly A2 Schematic Diagram (10133-2201, Rev. F) (Sheet 4 of 4)

Table 6-4. MOD/DEMOM PWB Assembly A4 (10133-2400-011, Rev. B) Parts List

Ref. Desig.	Part Number	Description
	Z71-0001-001	CARD EXTRACTOR
	J46-0047-003	HEADER, 3 POS
C1	C10-0003-012	CAP, .1UF
C2	CK05BX220K	CAP 22PF 10% 200V CER
C3	CK05BX220K	CAP 22PF 10% 200V CER
C4	C26-0035-220	CAP 22UF 20% 35V TANT
C5	C26-0035-220	CAP 22UF 20% 35V TANT
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C10-0003-012	CAP, .1UF
C12	C10-0003-012	CAP, .1UF
C13	C10-0003-012	CAP, .1UF
C14	C10-0003-012	CAP, .1UF
C15	C10-0003-012	CAP, .1UF
C16	C10-0003-012	CAP, .1UF
C17	C10-0003-012	CAP, .1UF
C18	C10-0003-012	CAP, .1UF
C19	C10-0003-012	CAP, .1UF
C20	C10-0003-012	CAP, .1UF
C21	C10-0003-012	CAP, .1UF
C22	C10-0003-012	CAP, .1UF
C23	C10-0003-012	CAP, .1UF
C24	C10-0003-012	CAP, .1UF
C25	C10-0003-012	CAP, .1UF
C26	C10-0003-012	CAP, .1UF
C27	C10-0003-012	CAP, .1UF
C28	C10-0003-012	CAP, .1UF
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	C10-0003-012	CAP, .1UF
C33	C10-0003-012	CAP, .1UF
C34	C10-0003-012	CAP, .1UF
C35	C10-0003-012	CAP, .1UF
DS1	N21-0008-000	DIODE, LIGHT EMITTING
P1	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
P2	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R50-0010-123	RES,SIP, 12K 10PIN
R2	R50-0010-123	RES,SIP, 12K 10PIN
R3	R50-0008-123	RES,SIP,12K, 8PIN
R4	R50-0006-102	RES,6 SIP, 1K,2.0%, 5RES
R5	RCR07G243JM	RES,24K 5% 1/4W CAR COMP

Table 6-4. MOD/DEMOP PWB Assembly A4 (10133-2400-011, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R6	R50-0008-123	RES,SIP,12K, 8PIN
R7	R50-0008-123	RES,SIP,12K, 8PIN
R8	R50-0008-123	RES,SIP,12K, 8PIN
R9	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R10	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R11	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R12	R50-0010-472	RES,10SIP,4.7K,2.0%, 9RES
R13	R50-0008-102	RES,8 SIP, 1K,2.0%, 7RES
R14	R50-0010-123	RES,SIP, 12K 10PIN
R15	R50-0010-123	RES,SIP, 12K 10PIN
R16	R50-0010-123	RES,SIP, 12K 10PIN
R17	R50-0010-123	RES,SIP, 12K 10PIN
R18	R50-0010-123	RES,SIP, 12K 10PIN
R19	R50-0010-123	RES,SIP, 12K 10PIN
R21	R50-0010-472	RES,10SIP,4.7K,2.0%, 9RES
R22	RCR07G562JM	RES,5.6K 5% 1/4W CAR COMP
R23	RCR07G181JM	RES,180 5% 1/4W CAR COMP
R24	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
R25	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
U1	I27-0011-001	DIGITAL SIGNAL PROCESSOR
U2	I15-0000-244	IC 74HC244 PLASTIC CMOS
U3	I15-0000-244	IC 74HC244 PLASTIC CMOS
U4	I15-0000-373	IC 74HC373 PLASTIC CMOS
U5	I15-0000-373	IC 74HC373 PLASTIC CMOS
U6	I15-0000-373	IC 74HC373 PLASTIC CMOS
U7	I15-0000-373	IC 74HC373 PLASTIC CMOS
U8	I15-0000-245	IC 74HC245 PLASTIC CMOS
U9	I15-0000-245	IC 74HC245 PLASTIC CMOS
U10	I15-0000-373	IC 74HC373 PLASTIC CMOS
U11	I58-0007-001	IC,BUS ARBITER
U12	I58-0008-001	BUS CONTROLLER
U13	I58-0008-001	BUS CONTROLLER
U14	I15-0000-373	IC 74HC373 PLASTIC CMOS
U15	I15-0000-245	IC 74HC245 PLASTIC CMOS
U16	I15-0000-245	IC 74HC245 PLASTIC CMOS
U17	I15-0000-138	IC 74HC138 PLASTIC CMOS
U18	I28-0001-001	IC 8259 INTERRUPT CONTROL
U19	I28-0001-001	IC 8259 INTERRUPT CONTROL
U20	I26-0017-001	IC STATIC RAM CMOS 8KX8
U21	I26-0017-001	IC STATIC RAM CMOS 8KX8
U26,U27	*SEE NOTE	
U28	I35-0008-001	SYSTEM TIMING CONTROLLER
U29	I15-0000-000	IC 74HC00 PLASTIC CMOS
U30	I15-0000-032	IC 74HC32 PLASTIC CMOS
U31	I15-0000-004	IC 74HC04 PLASTIC CMOS
XU1	J75-0011-068	IC SOCKET/COVER, 68 PIN
XU20	J77-0008-006	SOCKET, IC, 28 PIN
XU21	J77-0008-006	SOCKET, IC, 28 PIN

\*NOTE: When ordering replacement PROMs, refer to the part number (P/N) and the four-digit firmware number located on the PROM label.

**Table 6-4. MOD/DEMODO PWB Assembly A4 (10133-2400-011, Rev. B) Parts List (Cont.)**

<b>Ref. Desig.</b>	<b>Part Number</b>	<b>Description</b>
XU22	J77-0008-006	SOCKET, IC, 28 PIN
XU23	J77-0008-006	SOCKET, IC, 28 PIN
XU24	J77-0008-006	SOCKET, IC, 28 PIN
XU25	J77-0008-006	SOCKET, IC, 28 PIN
XU26	J77-0008-006	SOCKET, IC, 28 PIN
XU27	J77-0008-006	SOCKET, IC, 28 PIN
XU28	J77-0008-007	SOCKET, 40PIN
Y1	Y15-0004-160	CRYSTAL, 16 MHZ

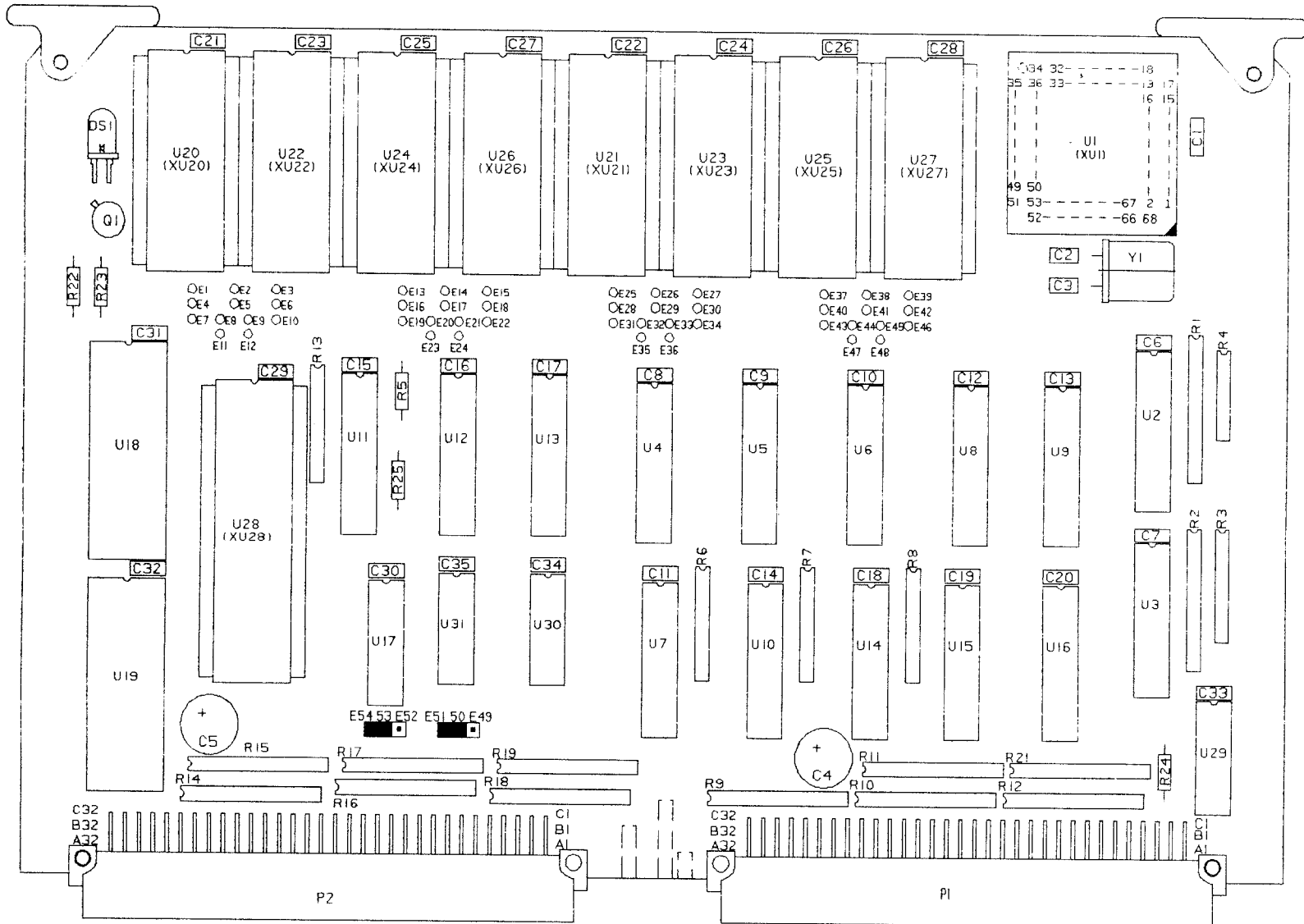


Figure 6-6. MOD/DEMOD A4 and FEC I/O A6 PWB Assembly Component Locations (10133-2400-01/02, Rev. G)

- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  5. WHEN USED WITH AN A2 ASSY (10133-2200 REV 'A'), JUMPER E50 TO E49 AND E52 TO E53. WHEN USED WITH AN A2 ASSY (10133-2200 REV 'B') AND UP, JUMPER E50 TO E51 AND E53 TO E54.

HIGHEST REFERENCE DESIGNATION			
C35	D51	D1	R25 U31
Y1			
REFERENCE DESIGNATIONS NOT USED			
R20			

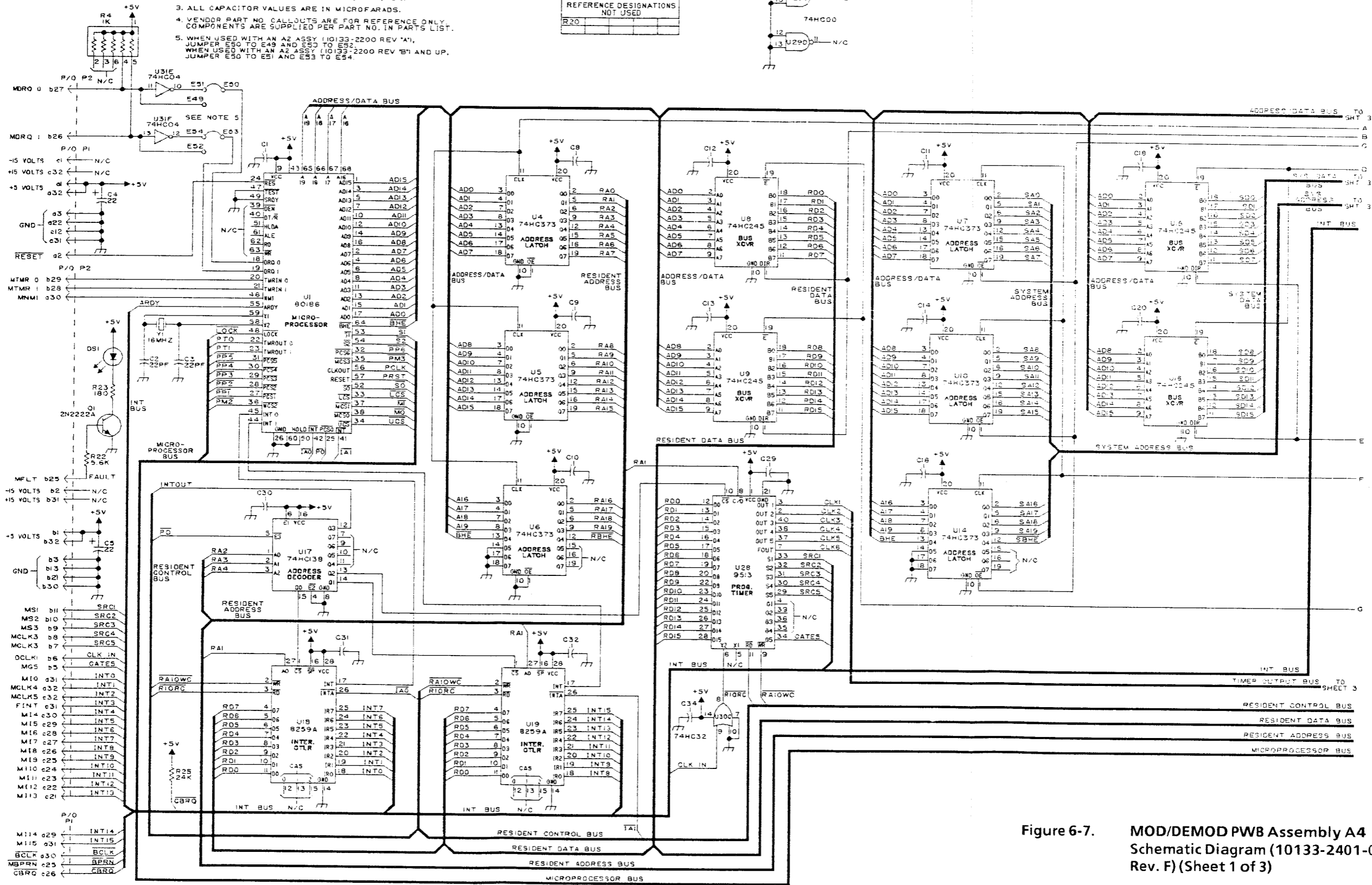
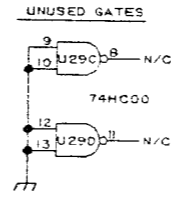


Figure 6-7. MOD/DEMOM PWB Assembly A4 Schematic Diagram (10133-2401-01, Rev. F) (Sheet 1 of 3)

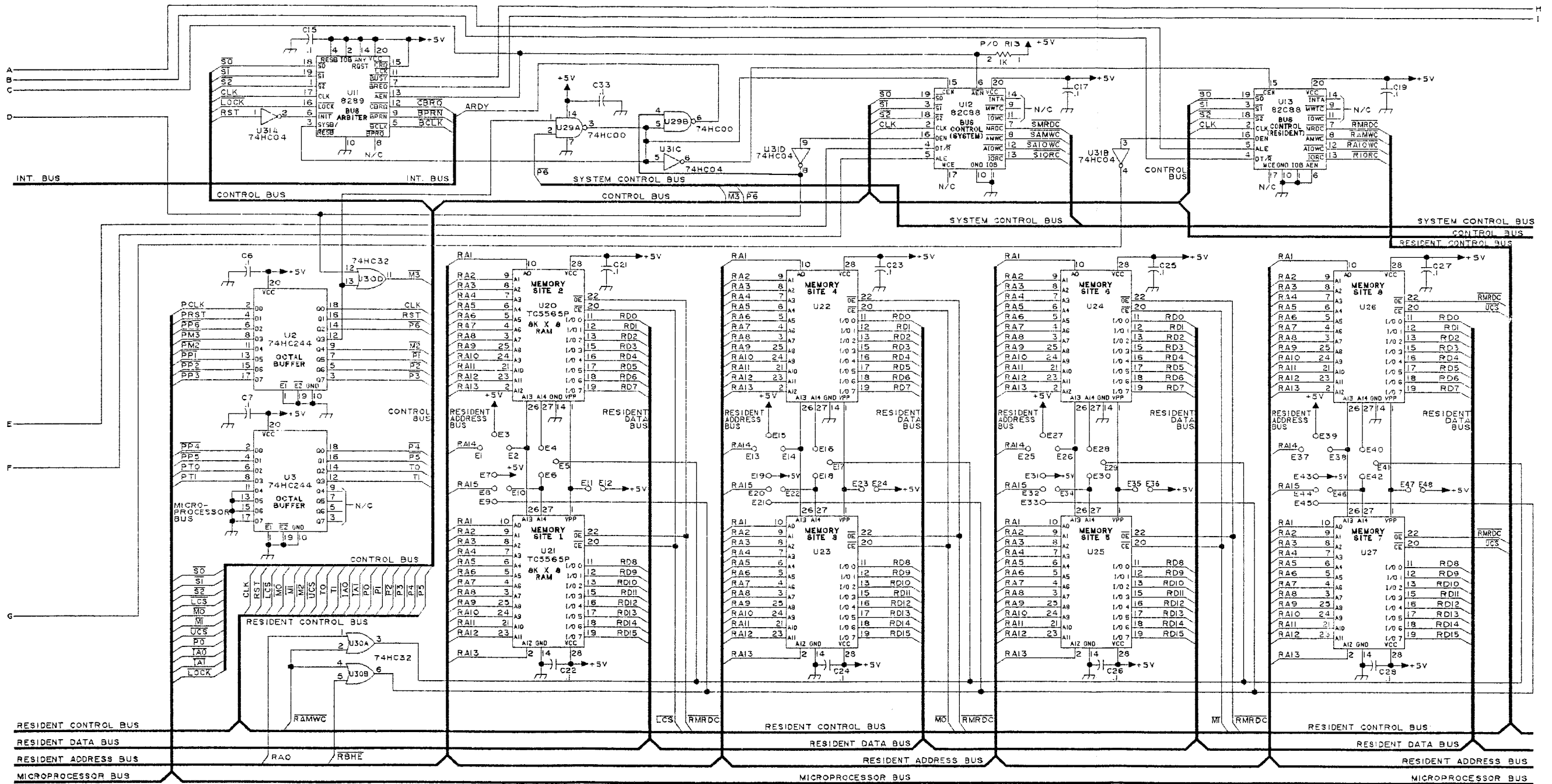


Figure 6-7. MOD/DEMOD PWB Assembly A4 Schematic Diagram (10133-2401-01, Rev. F) (Sheet 2 of 3)

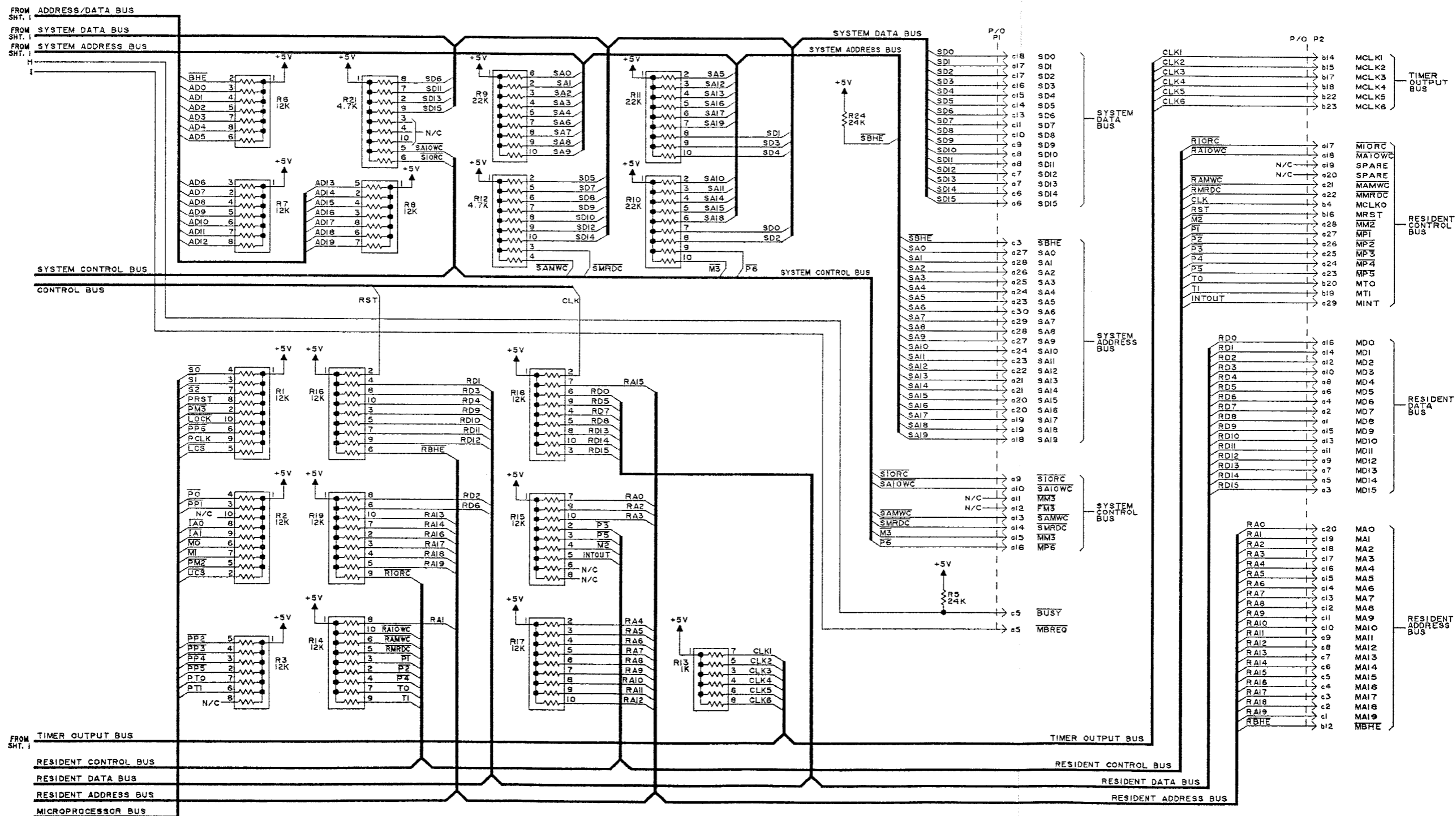


Figure 6-7. MOD/DEMOD PWB Assembly A4 Schematic Diagram (10133-2401-01, Rev. F) (Sheet 3 of 3)

Table 6-5. A5 FSK PWB Assembly Parts List (10133-2500-01, Rev. C)

Ref. Desig.	Part Number	Description
	Z71-0001-001	CARD EXTRACTOR
C1	C10-0003-012	CAP, .1UF
C2	C10-0003-012	CAP, .1UF
C3	C10-0003-012	CAP, .1UF
C4	C10-0003-012	CAP, .1UF
C5	C10-0003-012	CAP, .1UF
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C11-0012-332	CAP CER 3300PF
C11	C11-0012-102	CAP, CER .001UF 10%
C12	C11-0012-472	CAP CER, 4700PF 100V
C13	C11-0012-222	CAP FXD CER, 5%, 100V, .0022
C14	C11-0012-563	CAP .056UF 5% 100V CER
C15	C10-0003-012	CAP, .1UF
C16	C10-0003-012	CAP, .1UF
C17	C11-0012-102	CAP, CER .001UF 10%
C18	C10-0003-012	CAP, .1UF
C19	C10-0003-012	CAP, .1UF
C20	C26-0025-470	CAP 47UF 20% 25V TANT
C21	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1316	CAP, .22UF, 10%, 50V, CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	C26-0025-470	CAP 47UF 20% 25V TANT
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	M39014/02-1316	CAP, .22UF, 10%, 50V, CER-R
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	C10-0003-012	CAP, .1UF
C33	C11-0012-102	CAP, CER .001UF 10%
C34	C10-0003-012	CAP, .1UF
C35	C11-0012-682	CAP CER, 6800PF 100V
C36	C10-0003-012	CAP, .1UF
C37	C11-0012-102	CAP, CER .001UF 10%
C38	C11-0012-332	CAP CER 3300PF
C39	C11-0012-222	CAP FXD CER, 5%, 100V, .0022
C40	C11-0012-472	CAP CER, 4700PF 100V
C41	C11-0012-102	CAP, CER .001UF 10%
C42	C11-0012-102	CAP, CER .001UF 10%
C43	C11-0012-563	CAP .056UF 5% 100V CER
C44	C11-0012-682	CAP CER, 6800PF 100V
C45	C26-0050-109	CAP 1.0UF 20% 50V TANT
C46	C10-0003-012	CAP, .1UF

Table 6-5. A5 FSK PWB Assembly Parts List (10133-2500-01, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
C47	M39014/01-1535	CAP
C48	C10-0003-012	CAP, .1UF
C49	C10-0003-012	CAP, .1UF
C50	C10-0003-012	CAP, .1UF
C51	C10-0003-012	CAP, .1UF
C52	C10-0003-012	CAP, .1UF
C53	C10-0003-012	CAP, .1UF
C54	C10-0003-012	CAP, .1UF
C55	C10-0003-012	CAP, .1UF
C56	C10-0003-012	CAP, .1UF
C57	C10-0003-012	CAP, .1UF
C58	C10-0003-012	CAP, .1UF
C59	C10-0003-012	CAP, .1UF
C60	C10-0003-012	CAP, .1UF
C61	C10-0003-012	CAP, .1UF
C62	C10-0003-012	CAP, .1UF
C63	C11-0012-562	CAP CER, 5600PF 100V
C64	C11-0012-562	CAP CER, 5600PF 100V
C65	C11-0012-473	CAP CER, .047UF 100V
C66	C11-0012-332	CAP CER 3300PF
C67	C10-0003-012	CAP, .1UF
C68	C11-0012-102	CAP, CER .001UF 10%
C69	C11-0012-222	CAP FXD CER, 5%, 100V, .0022
C70	C11-0012-102	CAP, CER .001UF 10%
C71	C10-0003-012	CAP, .1UF
C72	C10-0003-012	CAP, .1UF
C73	C10-0003-012	CAP, .1UF
C74	C10-0003-012	CAP, .1UF
C75	C26-0025-470	CAP 47UF 20% 25V TANT
C76	C11-0012-473	CAP CER, .047UF 100V
C77	C11-0012-102	CAP, CER .001UF 10%
C78	C11-0012-562	CAP CER, 5600PF 100V
C79	C11-0012-102	CAP, CER .001UF 10%
C80	C11-0012-562	CAP CER, 5600PF 100V
C81	C11-0012-222	CAP FXD CER, 5%, 100V, .0022
C82	C11-0012-332	CAP CER 3300PF
C83	C10-0003-012	CAP, .1UF
C84	C10-0003-012	CAP, .1UF
C85	C10-0003-012	CAP, .1UF
C86	C10-0003-012	CAP, .1UF
C87	C10-0003-012	CAP, .1UF
CR1	1N4148	DIODE, SILICON
DS1	N21-0008-000	DIODE, LIGHT EMITTING
J1	J46-0013-026	HEADER ASSY, 26 PIN
J2	J46-0013-026	HEADER ASSY, 26 PIN
J3	J46-0013-014	CONNECTOR, 14 PIN
J4	J46-0013-014	CONNECTOR, 14 PIN
P2	J71-9600-196	CONN, 96PIN, RT, ANGLE, MALE

Table 6-5. A5 FSK PWB Assembly Parts List (10133-2500-01, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
Q1	JAN2N2222A	XSTR SS/GP NPN TO-18
Q2	JAN2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R2	RN55D5111F	RES,5110 1% 1/8W MET FLM
R3	RN55D2872F	RES,28.7K 1% 1/8W MET FLM
R4	RN55D2322F	RES,23.2K 1% 1/8W MET FLM
R5	RN55D9091F	RES,9090 1% 1/8W MET FLM
R6	RN55D2372F	RES,23.7K 1% 1/8W MET FLM
R7	RN55D6191F	RES,6190 1% 1/8W MET FLM
R8	RN55D3482F	RES,34.8K 1% 1/8W MET FLM
R9	RN55D2262F	RES,22.6K 1% 1/8W MET FLM
R10	RN55D2262F	RES,22.6K 1% 1/8W MET FLM
R11	RN55D8251F	RES,8250 1% 1/8W MET FLM
R12	RN55D1102F	RES,11.0K 1% 1/8W MET FLM
R13	RN55D1872F	RES,18.7K 1% 1/8W MET FLM
R14	RN55D1542F	RES,15.4K 1% 1/8W MET FLM
R15	RN55D1542F	RES,15.4K 1% 1/8W MET FLM
R16	R65-0003-100	RES,10 5% 1/4W CAR FILM
R17	R65-0003-100	RES,10 5% 1/4W CAR FILM
R18	RN55D6191F	RES,6190 1% 1/8W MET FLM
R19	RN55D9091F	RES,9090 1% 1/8W MET FLM
R20	RN55D2322F	RES,23.2K 1% 1/8W MET FLM
R21	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R22	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R23	RN55D3321F	RES,3320 1% 1/8W MET FLM
R24	RN55D2872F	RES,28.7K 1% 1/8W MET FLM
R25	RN55D2872F	RES,28.7K 1% 1/8W MET FLM
R26	RN55D2262F	RES,22.6K 1% 1/8W MET FLM
R27	RN55D2262F	RES,22.6K 1% 1/8W MET FLM
R28	RN55D3482F	RES,34.8K 1% 1/8W MET FLM
R29	RN55D2372F	RES,23.7K 1% 1/8W MET FLM
R30	RN55D1542F	RES,15.4K 1% 1/8W MET FLM
R31	RN55D1542F	RES,15.4K 1% 1/8W MET FLM
R32	RN55D1872F	RES,18.7K 1% 1/8W MET FLM
R33	RN55D1102F	RES,11.0K 1% 1/8W MET FLM
R34	RN55D6191F	RES,6190 1% 1/8W MET FLM
R35	RN55D2872F	RES,28.7K 1% 1/8W MET FLM
R36	RN55D5111F	RES,5110 1% 1/8W MET FLM
R37	RN55D8251F	RES,8250 1% 1/8W MET FLM
R38	RN55D6191F	RES,6190 1% 1/8W MET FLM
R39	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R40	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R41	R65-0003-471	RES,470 5% 1/4W CAR FILM
R42	R65-0003-223	RES,22K 5% 1/4W CAR FILM
R43	RN55D1001F	RES,1000 1% 1/8W MET FLM
R44	R30-0007-104	POTENTIOMETER, 100K
R45	R30-0007-104	POTENTIOMETER, 100K
R46	R30-0007-104	POTENTIOMETER, 100K

Table 6-5. A5 FSK PWB Assembly Parts List (10133-2500-01, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
R47	R30-0007-104	POTENTIOMETER, 100K
R48	R65-0003-561	RES,560 5% 1/4W CAR FILM
R49	R65-0003-561	RES,560 5% 1/4W CAR FILM
R50	RN55D6811F	RES,6810 1% 1/8W MET FLM
R52	RN55D12R4F	RESISTOR,FILM,12.4K
R53	RN55D2002F	RES,20.0K 1% 1/8W MET FLM
R54	RN55D2002F	RES,20.0K 1% 1/8W MET FLM
R55	RN55D6811F	RES,6810 1% 1/8W MET FLM
R56	RN55D9091F	RES,9090 1% 1/8W MET FLM
R57	RN55D3242F	RES,32.4K 1% 1/8W MET FLM
R58	RN55D12R4F	RESISTOR,FILM,12.4K
R59	RN55D2871F	RES,2870 1% 1/8W MET FLM
R60	RN55D3242F	RES,32.4K 1% 1/8W MET FLM
R61	RN55D12R4F	RESISTOR,FILM,12.4K
R62	RN55D1692F	RES,16.9K 1% 1/8W MET FLM
R63	RN55D2552F	RES,25.5K 1% 1/8W MET FLM
R64	RN55D9091F	RES,9090 1% 1/8W MET FLM
R65	RN55D12R4F	RESISTOR,FILM,12.4K
R66	RN55D2002F	RES,20.0K 1% 1/8W MET FLM
R67	RN55D2002F	RES,20.0K 1% 1/8W MET FLM
R68	RN55D9091F	RES,9090 1% 1/8W MET FLM
R69	RN55D3242F	RES,32.4K 1% 1/8W MET FLM
R70	RN55D12R4F	RESISTOR,FILM,12.4K
R71	RN55D2871F	RES,2870 1% 1/8W MET FLM
R72	RN55D12R4F	RESISTOR,FILM,12.4K
R73	RN55D1692F	RES,16.9K 1% 1/8W MET FLM
R74	RN55D2552F	RES,25.5K 1% 1/8W MET FLM
R75	RN55D9091F	RES,9090 1% 1/8W MET FLM
R76	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R77	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R78	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R79	RN55D1003F	RES,100K 1% 1/8W MET FLM
R80	RN55D2003F	RES,200K 1% 1/8W MET FLM
R81	RN55D5622F	RES,56.2K 1% 1/8W MET FLM
R82	RN55D1003F	RES,100K 1% 1/8W MET FLM
R83	RN55D2003F	RES,200K 1% 1/8W MET FLM
R84	RN55D5622F	RES,56.2K 1% 1/8W MET FLM
R85	RN55D3242F	RES,32.4K 1% 1/8W MET FLM
R86	RN55D5623F	RES,562K 1% 1/8W MET FLM
R87	RN55D1003F	RES,100K 1% 1/8W MET FLM
R88	RN55D5623F	RES,562K 1% 1/8W MET FLM
R89	RN55D1003F	RES,100K 1% 1/8W MET FLM
R90	RN55D5623F	RES,562K 1% 1/8W MET FLM
R91	RN55D5623F	RES,562K 1% 1/8W MET FLM
R92	RN55D1001F	RES,1000 1% 1/8W MET FLM
R93	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R94	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R95	R65-0003-103	RES,10K 5% 1/4W CAR FILM

Table 6-5. A5 FSK PWB Assembly Parts List (10133-2500-01, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
R96	R65-0003-472	RES, 4.7K 5% 1/4W CAR FILM
TP1	J46-0047-001	HEADER, 1 POS
TP2	J46-0047-001	HEADER, 1 POS
TP3	J46-0047-001	HEADER, 1 POS
TP4	J46-0047-001	HEADER, 1 POS
TP5	J46-0047-001	HEADER, 1 POS
TP6	J46-0047-001	HEADER, 1 POS
TP7	J46-0047-001	HEADER, 1 POS
TP8	J46-0047-001	HEADER, 1 POS
TP9	J46-0047-001	HEADER, 1 POS
TP10	J46-0047-001	HEADER, 1 POS
TP11	J46-0047-001	HEADER, 1 POS
TP12	J46-0047-001	HEADER, 1 POS
TP13	J46-0047-001	HEADER, 1 POS
TP14	J46-0047-001	HEADER, 1 POS
TP15	J46-0047-001	HEADER, 1 POS
TP16	J46-0047-001	HEADER, 1 POS
TP17	J46-0047-001	HEADER, 1 POS
U1	I15-1000-004	HEX CMOS INVERTER
U2	I15-1000-155	IC 74HCT155 PLASTIC CMOS
U3	I03-1000-074	IC 74F74 FAST TTL PLAS
U4	I03-1000-652	IC 74F652 FAST TTL PLAS
U5	I03-1000-652	IC 74F652 FAST TTL PLAS
U6	I15-1000-259	IC, 74HCT259
U7	I03-1000-244	IC 74F244 FAST TTL PLAS
U8	I15-1000-074	IC, 74HCT74
U9	I03-1000-008	IC 74F08 FAST TTL PLAS
U10	I30-0041-002	IC 074 OP AMP PLASTIC
U11	I30-0041-002	IC 074 OP AMP PLASTIC
U12	I30-0041-002	IC 074 OP AMP PLASTIC
U13	I06-0002-001	IC DG211 PLASTIC CMOS
U14	I03-0022-001	IC A/D CONV CSZ5116-JC16
U15	I15-1000-074	IC, 74HCT74
U16	I03-1000-032	IC 74F32 FAST TTL PLAS
U17	I03-1000-004	IC 74F04 FAST TTL PLAS
U18	I12-0006-005	IC VR 78L05A +5V .10A 4%
U19	I12-0010-005	IC VR 79L05A -5V .10A 4%
U20	I15-1000-393	IC 74HCT393 PLASTIC CMOS
U21	I15-1000-000	IC 74HCT00 PLASTIC CMOS
U22	I03-1000-374	IC 74F374 FAST TTL PLAS
U23	10133-8021	IC PROGRAMMED
U24	I26-0017-003	IC RAM, 8K IDT7164S35P
U25	10133-8022	IC PROGRAMMED
U26	I26-0017-003	IC RAM, 8K IDT7164S35P
U27	I15-1000-174	IC 74HCT174 PLASTIC CMOS
U28	I03-1000-138	IC 74F138 FAST TTL PLAS
U29	I27-0019-001	IC DIG PRCR 40MHZ CLK
U30	I35-0004-000	IC 555 TIMER PLASTIC

Table 6-5. A5 FSK PWB Assembly Parts List (10133-2500-01, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
U31	I03-0021-001	IC D/A CONV, PCM53KP-V
U32	I30-0041-002	IC 074 OP AMP PLASTIC
U33	I30-0041-002	IC 074 OP AMP PLASTIC
U34	I06-0002-001	IC DG211 PLASTIC CMOS
U35	I03-1000-374	IC 74F374 FAST TTL PLAS
U36	I03-1000-374	IC 74F374 FAST TTL PLAS
U37	I03-1000-374	IC 74F374 FAST TTL PLAS
U38	I15-1000-157	IC 74HCT157 PLASTIC CMOS
U39	I15-1000-157	IC 74HCT157 PLASTIC CMOS
U40	I15-1000-157	IC 74HCT157 PLASTIC CMOS
U41	I14-0010-008	IC 5.0V REF 2% LM336 COM
XU14	J77-0008-007	SOCKET, 40PIN
XU23	J77-0008-006	SOCKET, IC, 28 PIN
XU24	J77-0008-006	SOCKET, IC, 28 PIN
XU25	J77-0008-006	SOCKET, IC, 28 PIN
XU26	J77-0008-006	SOCKET, IC, 28 PIN
XU29	J77-0010-068	SKT IC PGA 68 PIN
XU31	J77-0008-005	SOCKET, 24PIN
Y1	10075-1088	XTAL OSC, 3.6864MHZ
Y2	10075-1087	XTAL OSC, 40MHZ

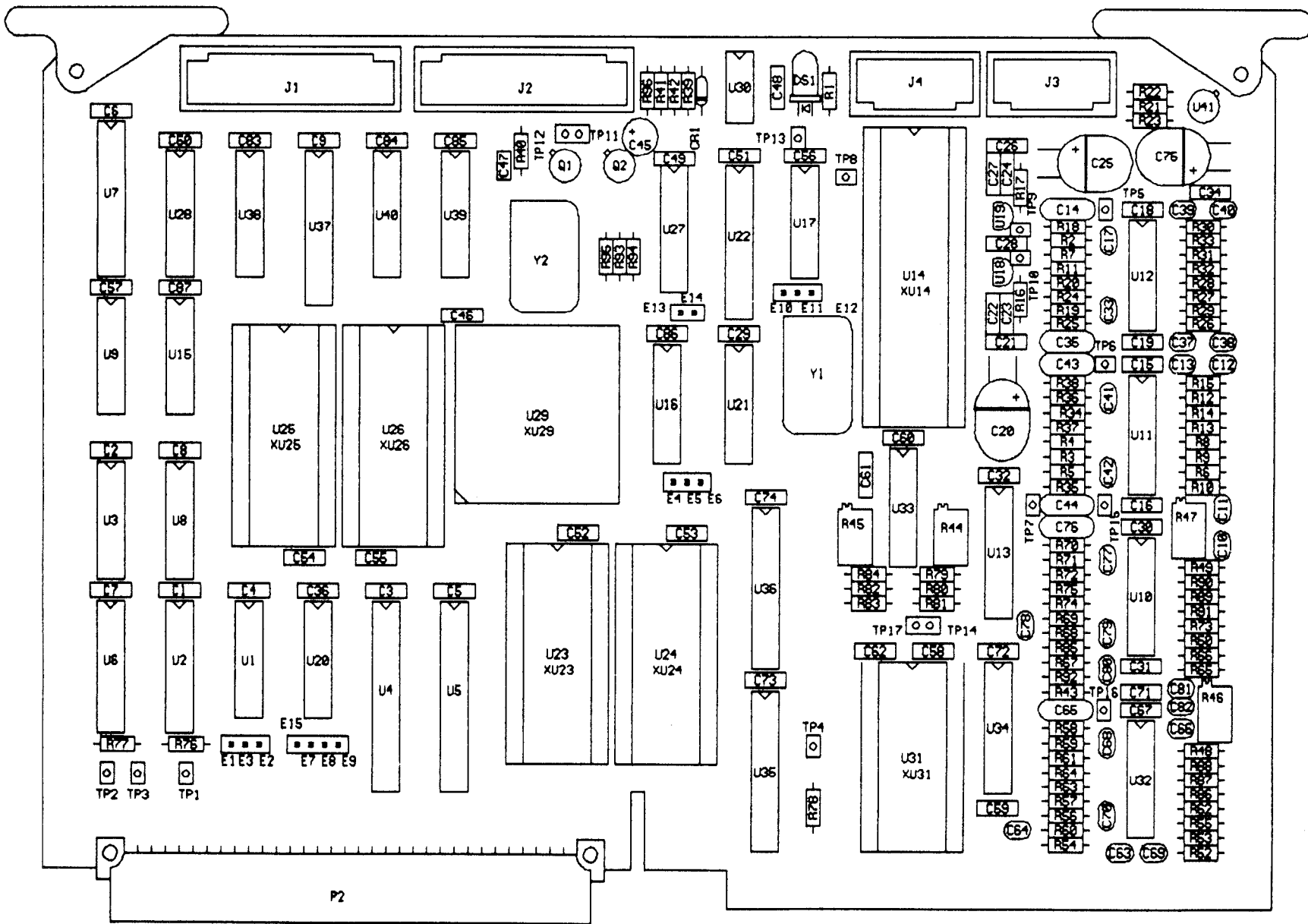


Figure 6-8. A5 FSK PWB Assembly Component Location Diagram (10133-2500, Rev. D)

- NOTE: UNLESS OTHERWISE SPECIFIED:
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  - ALL RESISTOR VALUES ARE IN OHMS, 1/4W, +/-5%.
  - ALL CAPACITOR VALUES ARE IN MICROFARADS.
  - VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

AS FIRMWARE		JUMPERING				
ALL		E3 TO E1	E6 TO E5	E8 TO E7	E11 TO E10	E13 TO E14

HIGHEST REFERENCE DESIGNATION					
C89	CR1	DS1	J4	P2	
Q2	R95	TP17	U41	V2	
REF. DESIGNATIONS NOT USED					

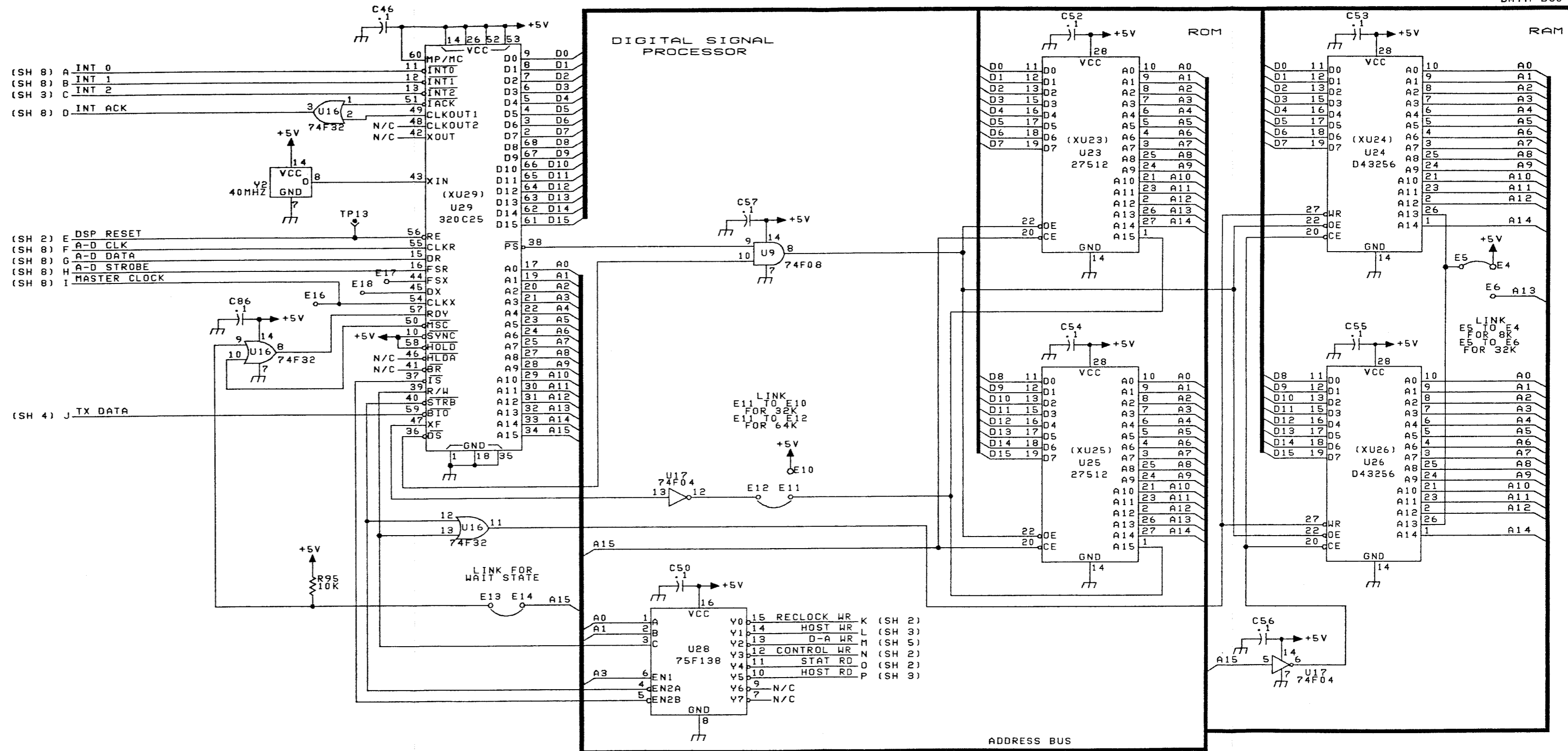
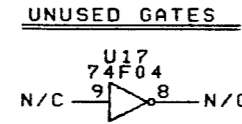


Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 1 of 8)

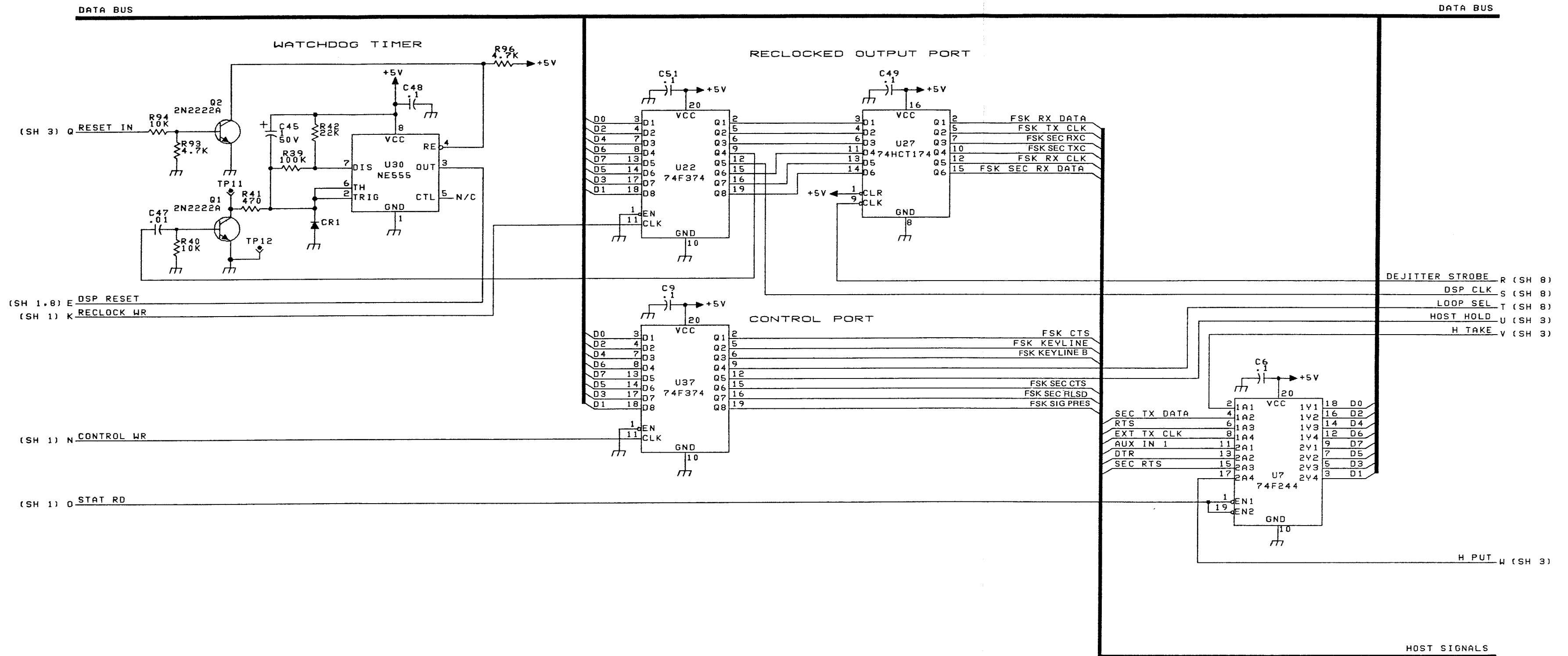


Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 2 of 8)

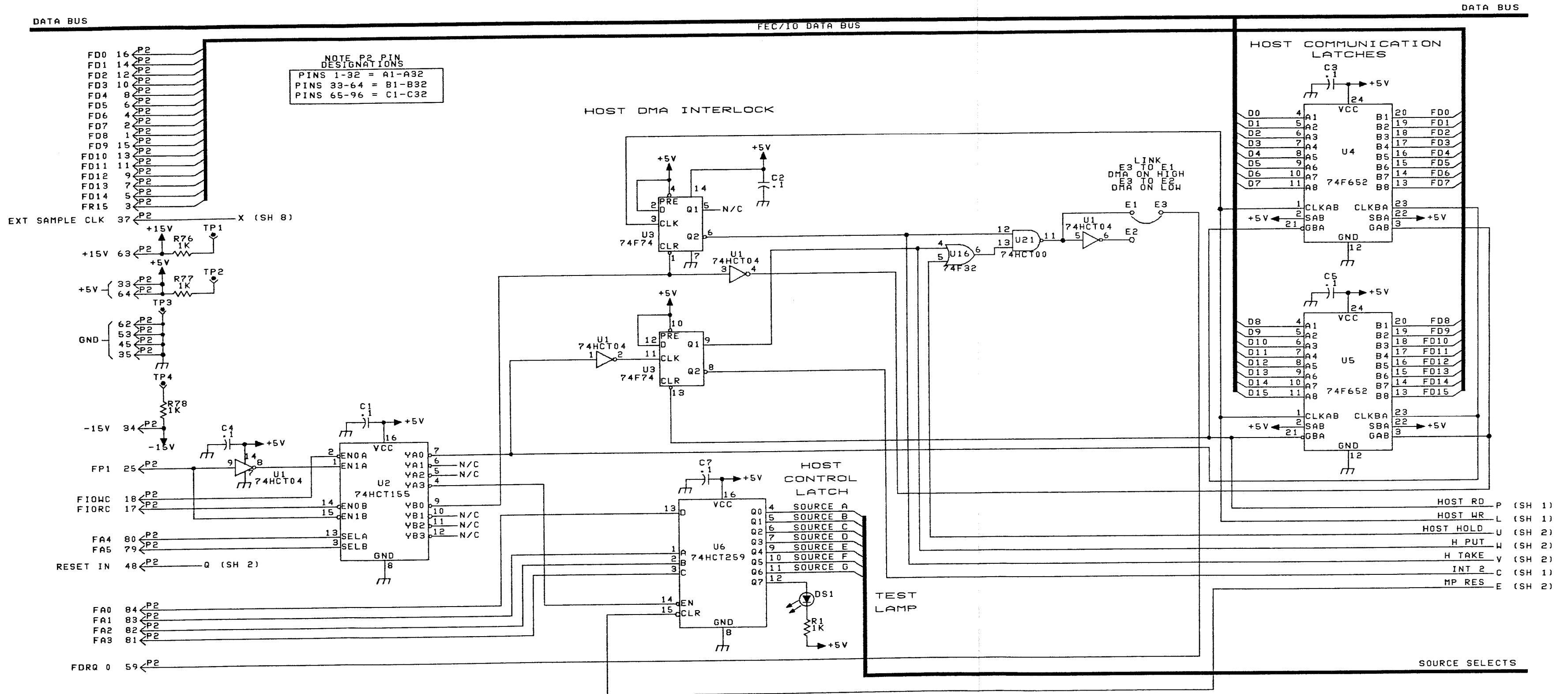
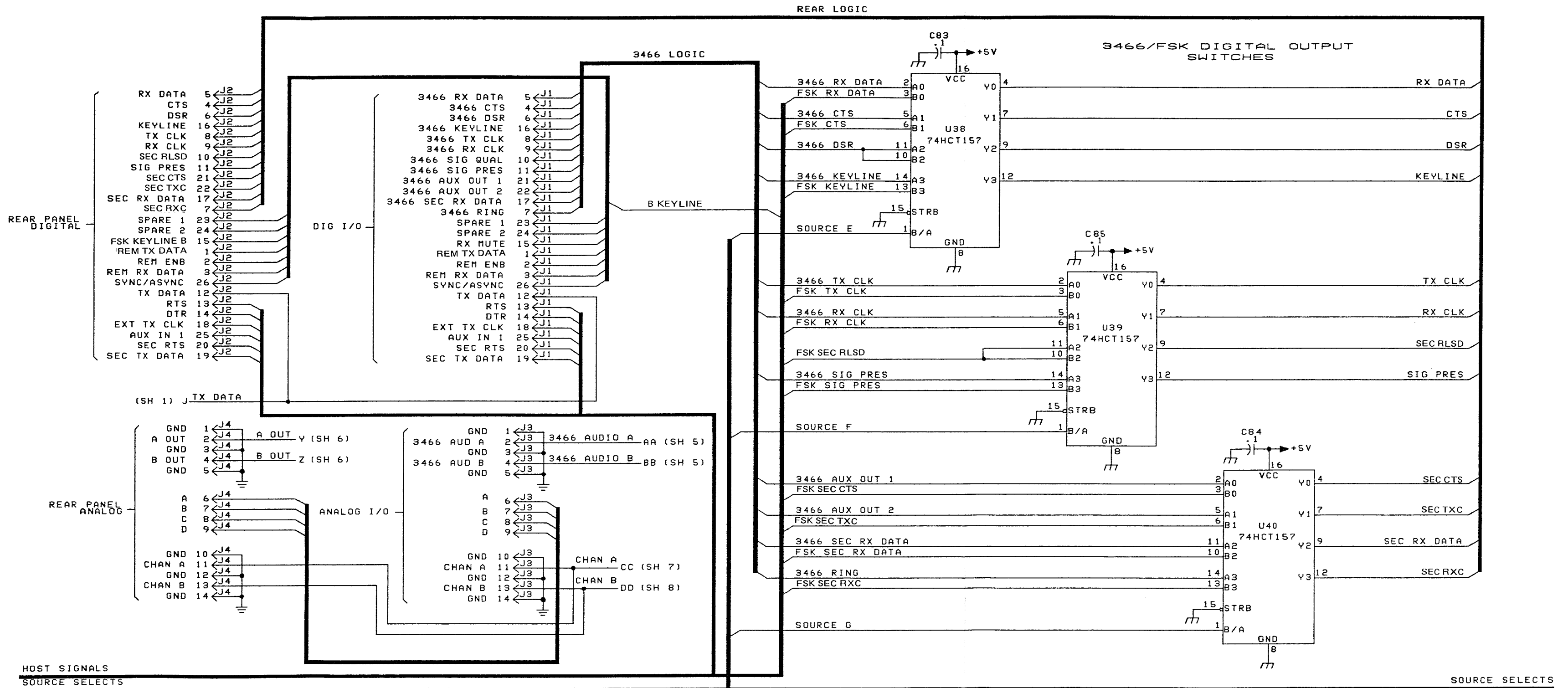


Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 3 of 8)



HOST SIGNALS  
SOURCE SELECTS

SOURCE SELECTS

Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 4 of 8)

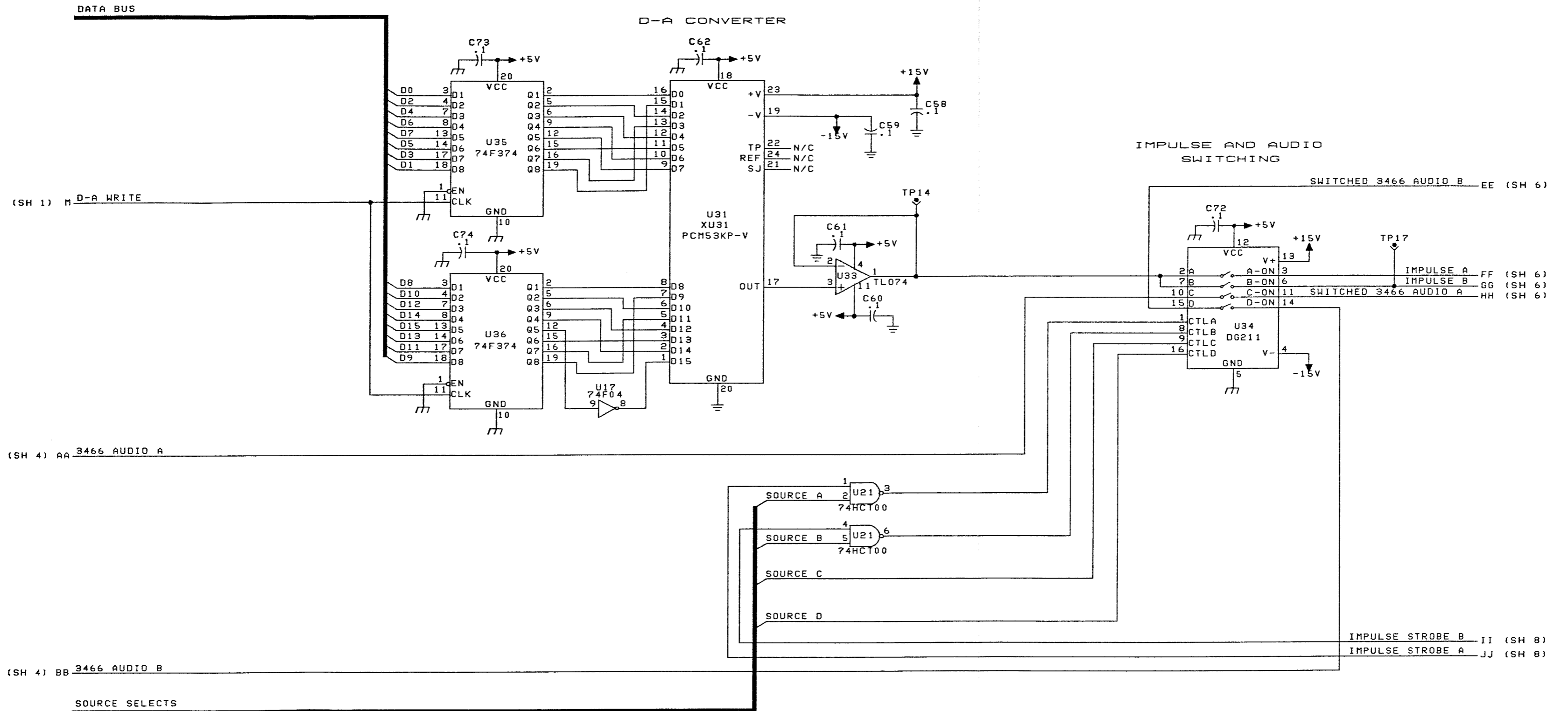


Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 5 of 8)

ANTI-IMAGE FILTERS

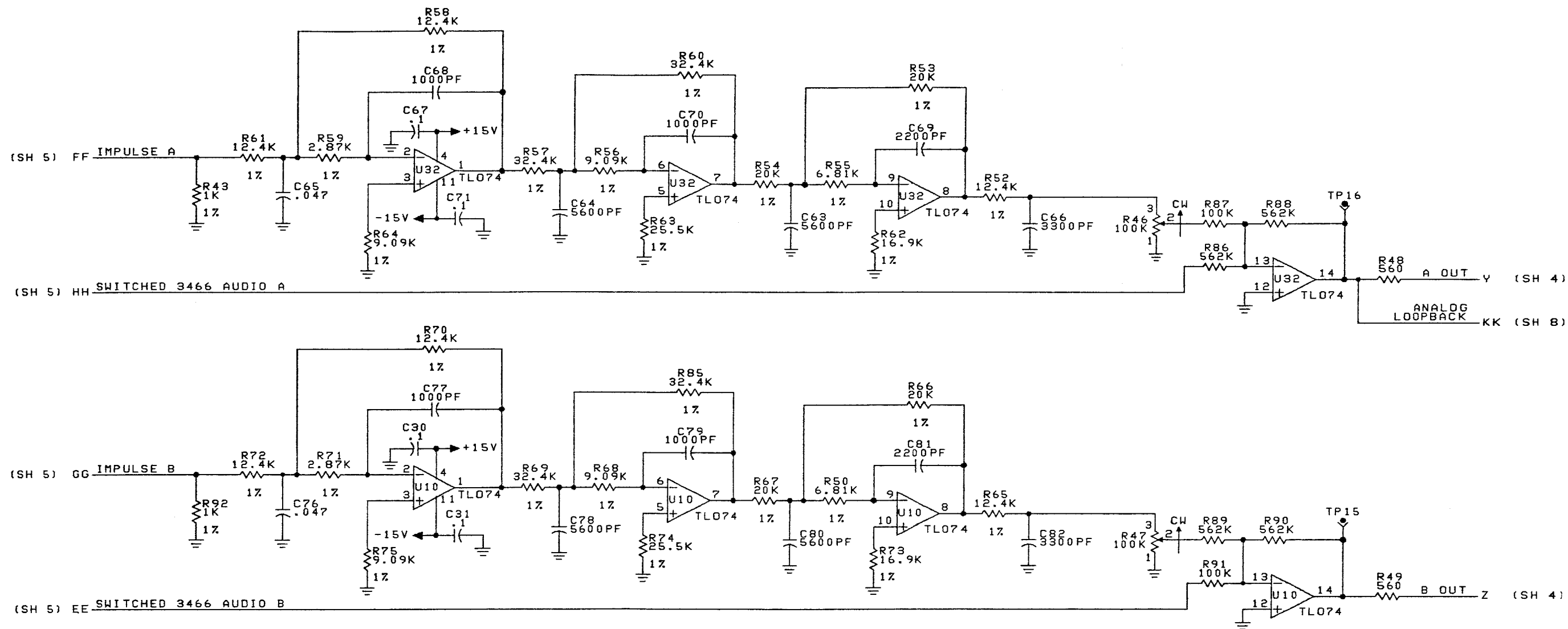


Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 6 of 8)

ANTI-ALIAS FILTERS

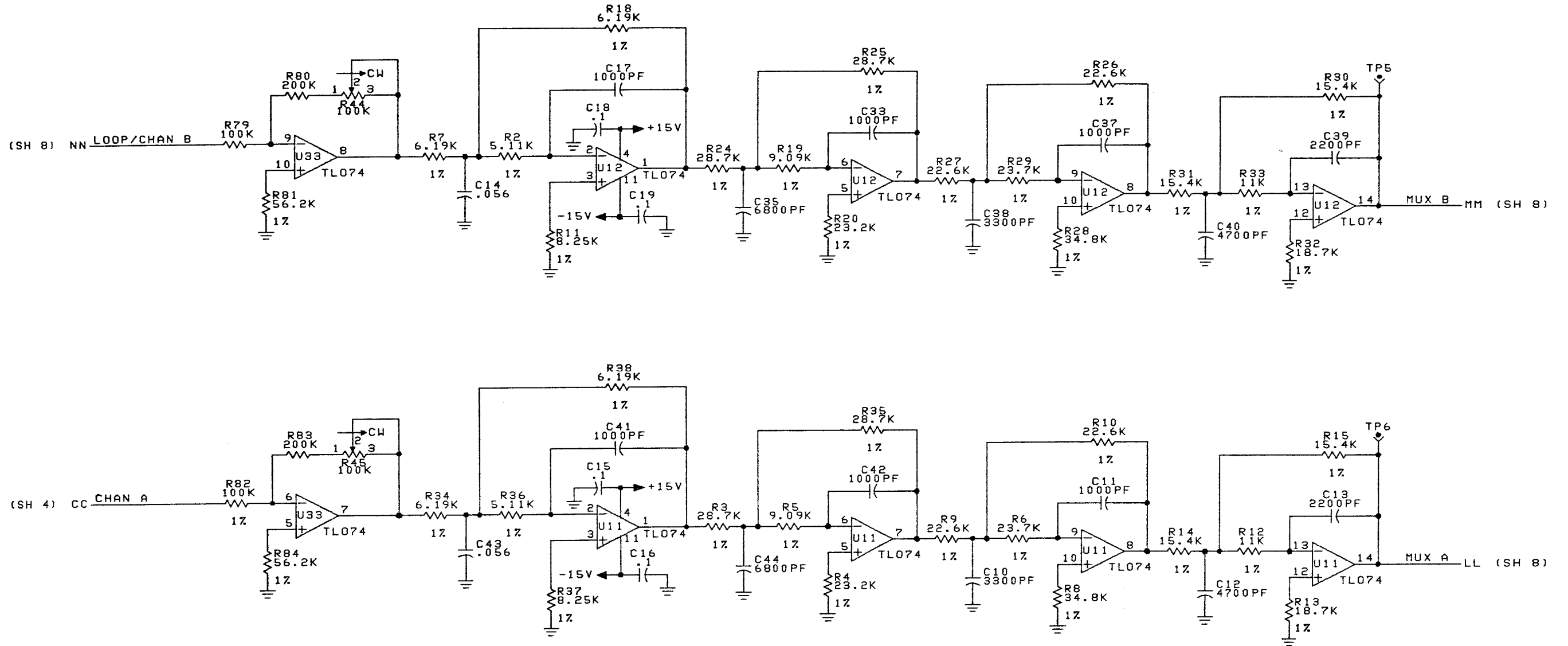


Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 7 of 8)

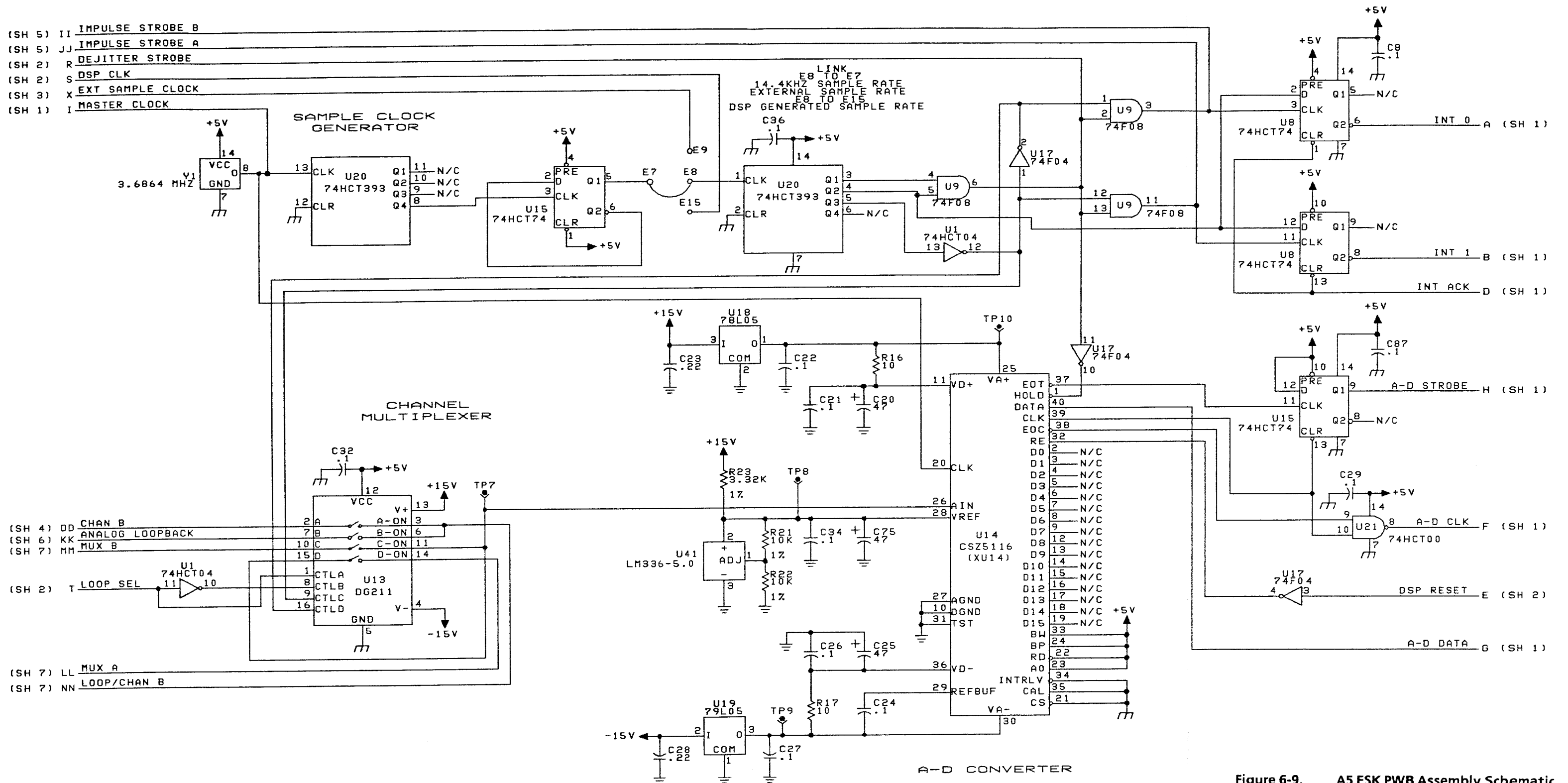


Figure 6-9. A5 FSK PWB Assembly Schematic Diagram (10133-2501, Rev. D) (Sheet 8 of 8)

Table 6-6. FEC I/O PWB Assembly A6 (10133-2400-021, Rev. B) Parts List

Ref. Desig.	Part Number	Description
	Z71-0001-001	CARD EXTRACTOR
	J46-0047-003	HEADER, 3 POS
C1	C10-0003-012	CAP, .1UF
C2	CK05BX220K	CAP 22PF 10% 200V CER
C3	CK05BX220K	CAP 22PF 10% 200V CER
C4	C26-0035-220	CAP 22UF 20% 35V TANT
C5	C26-0035-220	CAP 22UF 20% 35V TANT
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C10-0003-012	CAP, .1UF
C12	C10-0003-012	CAP, .1UF
C13	C10-0003-012	CAP, .1UF
C14	C10-0003-012	CAP, .1UF
C15	C10-0003-012	CAP, .1UF
C16	C10-0003-012	CAP, .1UF
C17	C10-0003-012	CAP, .1UF
C18	C10-0003-012	CAP, .1UF
C19	C10-0003-012	CAP, .1UF
C20	C10-0003-012	CAP, .1UF
C21	C10-0003-012	CAP, .1UF
C22	C10-0003-012	CAP, .1UF
C23	C10-0003-012	CAP, .1UF
C24	C10-0003-012	CAP, .1UF
C25	C10-0003-012	CAP, .1UF
C26	C10-0003-012	CAP, .1UF
C27	C10-0003-012	CAP, .1UF
C28	C10-0003-012	CAP, .1UF
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	C10-0003-012	CAP, .1UF
C33	C10-0003-012	CAP, .1UF
C34	C10-0003-012	CAP, .1UF
C35	C10-0003-012	CAP, .1UF
DS1	N21-0008-000	DIODE, LIGHT EMITTING
P1	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
P2	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R50-0010-123	RES,SIP, 12K 10PIN
R2	R50-0010-123	RES,SIP, 12K 10PIN
R3	R50-0008-123	RES,SIP,12K, 8PIN
R4	R50-0006-102	RES,6 SIP, 1K,2.0%, 5RES

Table 6-6. FEC I/O PWB Assembly A6 (10133-2400-021, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R5	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
R6	R50-0008-123	RES,SIP,12K, 8PIN
R7	R50-0008-123	RES,SIP,12K, 8PIN
R8	R50-0008-123	RES,SIP,12K, 8PIN
R9	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R10	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R11	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R12	R50-0010-472	RES,10SIP,4.7K,2.0%, 9RES
R13	R50-0008-102	RES,8 SIP, 1K,2.0%, 7RES
R14	R50-0010-123	RES,SIP, 12K 10PIN
R15	R50-0010-123	RES,SIP, 12K 10PIN
R16	R50-0010-123	RES,SIP, 12K 10PIN
R17	R50-0010-123	RES,SIP, 12K 10PIN
R18	R50-0010-123	RES,SIP, 12K 10PIN
R19	R50-0010-123	RES,SIP, 12K 10PIN
R21	R50-0010-472	RES,10SIP,4.7K,2.0%, 9RES
R22	RCR07G562JM	RES,5.6K 5% 1/4W CAR COMP
R23	RCR07G181JM	RES,180 5% 1/4W CAR COMP
R24	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
R25	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
U1	I27-0011-001	DIGITAL SIGNAL PROCESSOR
U2	I15-0000-244	IC 74HC244 PLASTIC CMOS
U3	I15-0000-244	IC 74HC244 PLASTIC CMOS
U4	I15-0000-373	IC 74HC373 PLASTIC CMOS
U5	I15-0000-373	IC 74HC373 PLASTIC CMOS
U6	I15-0000-373	IC 74HC373 PLASTIC CMOS
U7	I15-0000-373	IC 74HC373 PLASTIC CMOS
U8	I15-0000-245	IC 74HC245 PLASTIC CMOS
U9	I15-0000-245	IC 74HC245 PLASTIC CMOS
U10	I15-0000-373	IC 74HC373 PLASTIC CMOS
U11	I58-0007-001	IC,BUS ARBITER
U12	I58-0008-001	BUS CONTROLLER
U13	I58-0008-001	BUS CONTROLLER
U14	I15-0000-373	IC 74HC373 PLASTIC CMOS
U15	I15-0000-245	IC 74HC245 PLASTIC CMOS
U16	I15-0000-245	IC 74HC245 PLASTIC CMOS
U17	I15-0000-138	IC 74HC138 PLASTIC CMOS
U18	I28-0001-001	IC 8259 INTERRUPT CONTROL
U19	I28-0001-001	IC 8259 INTERRUPT CONTROL
U22	I26-0021-002	IC, RAM 32K X 8A
U23	I26-0021-002	IC, RAM 32K X 8A
U24-U27	*SEE NOTE	

\*NOTE: When ordering replacement PROMs, refer to the part number (P/N) and the four-digit firmware number located on the PROM label.

Table 6-6. FEC I/O PWB Assembly A6 (10133-2400-021, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
U28	I35-0008-001	SYSTEM TIMING CONTROLLER
U29	I15-0000-000	IC 74HC00 PLASTIC CMOS
U30	I15-0000-032	IC 74HC32 PLASTIC CMOS
U31	I15-0000-004	IC 74HC04 PLASTIC CMOS
XU1	J75-0011-068	IC SOCKET/COVER, 68 PIN
XU20	J77-0008-006	SOCKET, IC, 28 PIN
XU21	J77-0008-006	SOCKET, IC, 28 PIN
XU22	J77-0008-006	SOCKET, IC, 28 PIN
XU23	J77-0008-006	SOCKET, IC, 28 PIN
XU24	J77-0008-006	SOCKET, IC, 28 PIN
XU25	J77-0008-006	SOCKET, IC, 28 PIN
XU26	J77-0008-006	SOCKET, IC, 28 PIN
XU27	J77-0008-006	SOCKET, IC, 28 PIN
XU28	J77-0008-007	SOCKET, 40PIN
Y1	Y15-0004-160	CRYSTAL, 16 MHZ

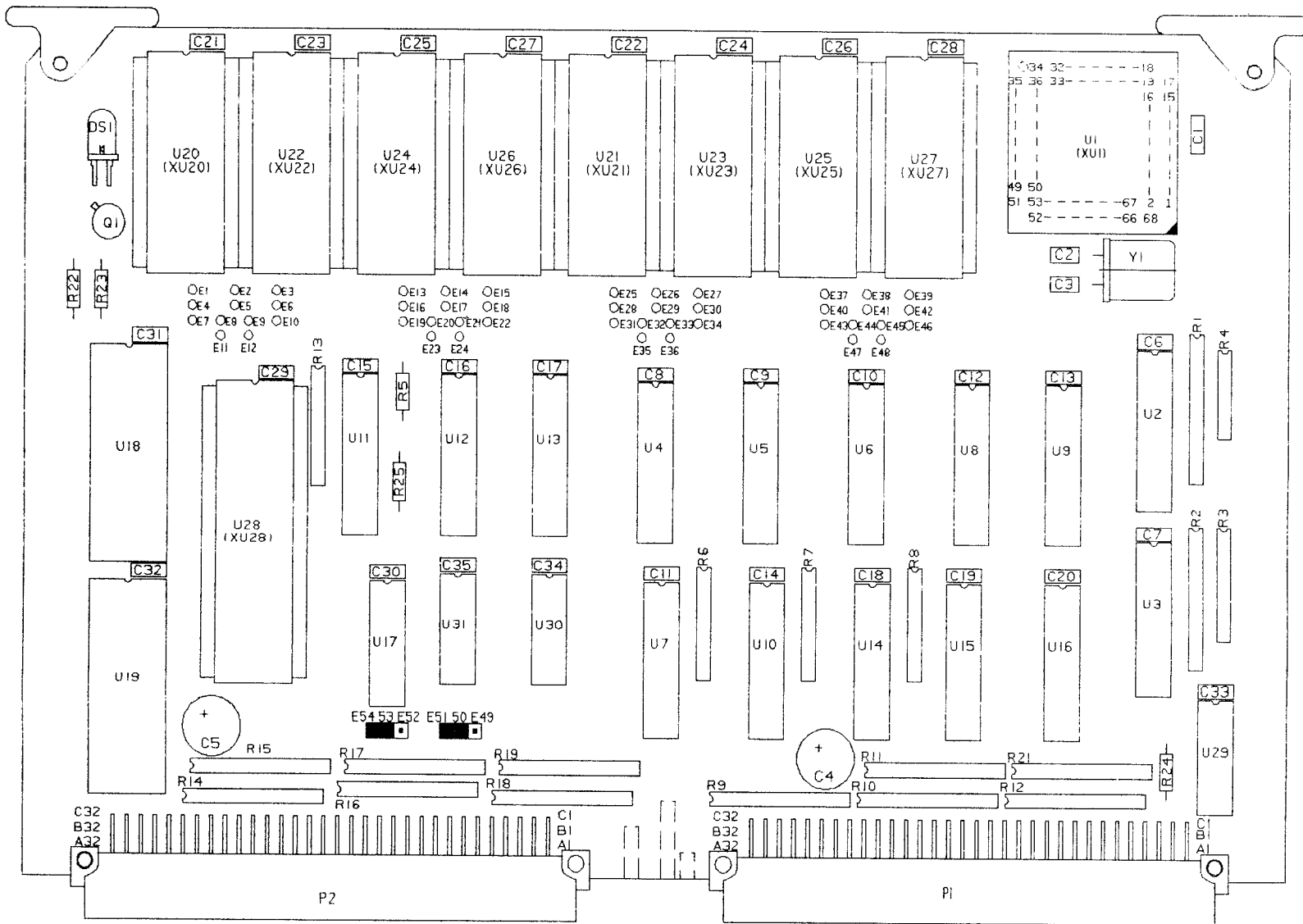


Figure 6-10. MOD/DEMOD A4 and FEC I/O PWB Assembly Component Locations (10133-2400-01/-02 Rev. G)

- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  5. WHEN USED WITH AN A2 ASSY (10133-2200 REV 'A'), JUMPER E50 TO E49 AND E53 TO E52. WHEN USED WITH AN A2 ASSY (10133-2200 REV 'B') AND UP, JUMPER E50 TO E51 AND E53 TO E54.

HIGHEST REFERENCE DESIGNATION			
C35	DS1	Q1	R25 U31
Y1			
REFERENCE DESIGNATIONS NOT USED			
R20			

UNUSED GATES

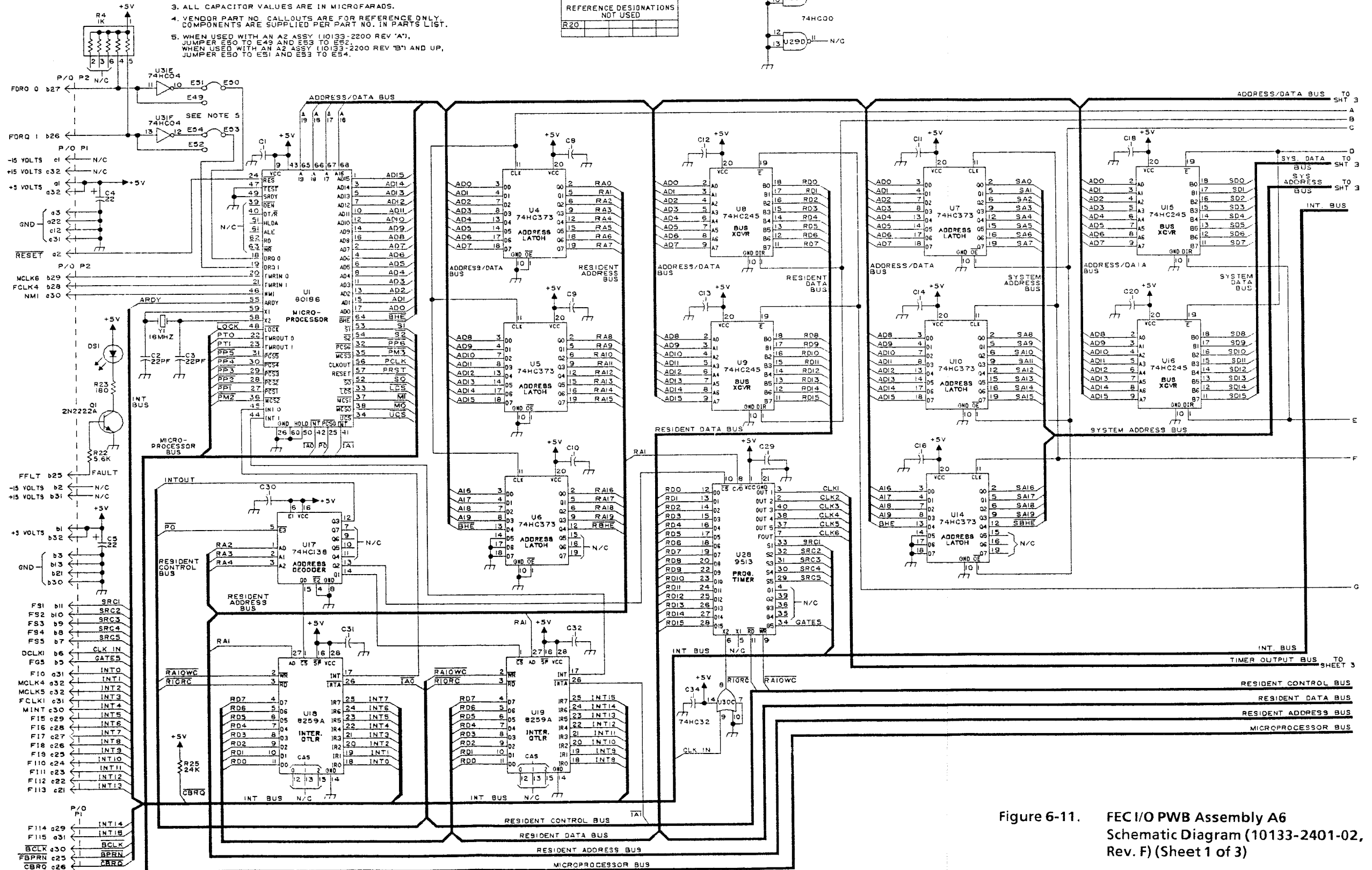
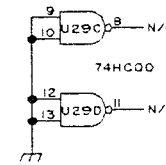
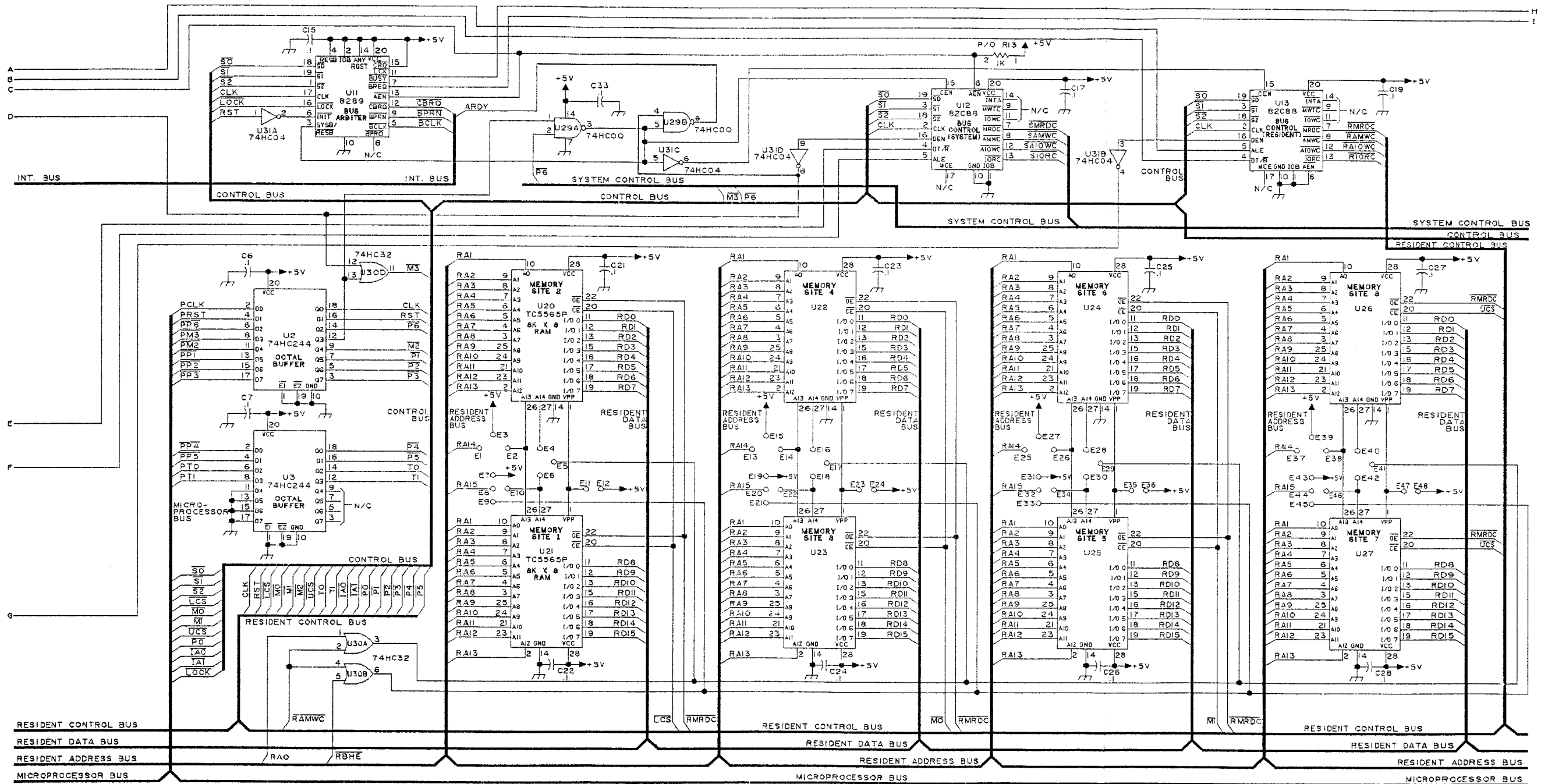


Figure 6-11. FEC I/O PWB Assembly A6  
Schematic Diagram (10133-2401-02,  
Rev. F) (Sheet 1 of 3)



HSM-901

Figure 6-11. FEC I/O PWB Assembly A6  
Schematic Diagram (10133-2401-02,  
Rev. F) (Sheet 2 of 3)

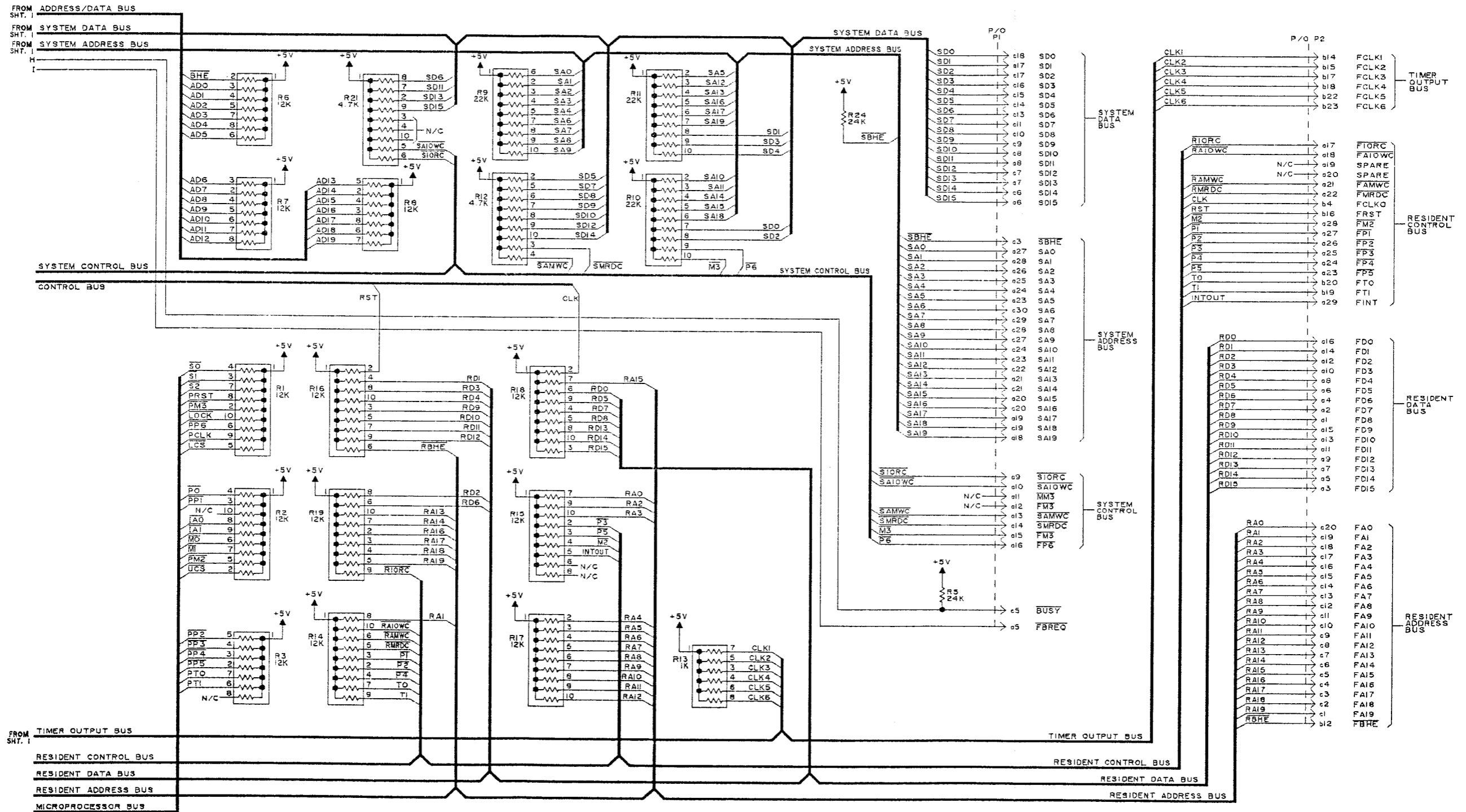


Figure 6-11. FEC I/O PWB Assembly A6  
Schematic Diagram (10133-2401-02,  
Rev. F) (Sheet 3 of 3)

Table 6-7. Decoder PWB Assembly A7 (10133-2450-01, Rev. B) Parts List

Ref. Desig.	Part Number	Description
	Z71-0001-001	CARD EXTRACTOR
	J46-0047-003	HEADER, 3 POS
C1	C10-0003-012	CAP, .1UF
C2	CK05BX220K	CAP 22PF 10% 200V CER
C3	CK05BX220K	CAP 22PF 10% 200V CER
C4	C26-0035-220	CAP 22UF 20% 35V TANT
C5	C26-0035-220	CAP 22UF 20% 35V TANT
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C10-0003-012	CAP, .1UF
C12	C10-0003-012	CAP, .1UF
C13	C10-0003-012	CAP, .1UF
C14	C10-0003-012	CAP, .1UF
C15	C10-0003-012	CAP, .1UF
C16	C10-0003-012	CAP, .1UF
C17	C10-0003-012	CAP, .1UF
C18	C10-0003-012	CAP, .1UF
C19	C10-0003-012	CAP, .1UF
C20	C10-0003-012	CAP, .1UF
C21	C10-0003-012	CAP, .1UF
C22	C10-0003-012	CAP, .1UF
C23	C10-0003-012	CAP, .1UF
C24	C10-0003-012	CAP, .1UF
C25	C10-0003-012	CAP, .1UF
C26	C10-0003-012	CAP, .1UF
C27	C10-0003-012	CAP, .1UF
C28	C10-0003-012	CAP, .1UF
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	C10-0003-012	CAP, .1UF
C33	C10-0003-012	CAP, .1UF
C34	C10-0003-012	CAP, .1UF
C35	C10-0003-012	CAP, .1UF
DS1	N21-0008-000	DIODE, LIGHT EMITTING
P1	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
P2	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R50-0010-123	RES,SIP, 12K 10PIN
R2	R50-0010-123	RES,SIP, 12K 10PIN
R3	R50-0008-123	RES,SIP,12K, 8PIN

Table 6-7. Decoder PWB Assembly A7 (10133-2450-01, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R4	R50-0006-102	RES,6 SIP, 1K,2.0%, 5RES
R5	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
R6	R50-0008-123	RES,SIP,12K, 8PIN
R7	R50-0008-123	RES,SIP,12K, 8PIN
R8	R50-0008-123	RES,SIP,12K, 8PIN
R9	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R10	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R11	R50-0010-223	RES,10SIP, 22K,2.0%, 9RES
R12	R50-0010-472	RES,10SIP,4.7K,2.0%, 9RES
R13	R50-0008-102	RES,8 SIP, 1K,2.0%, 7RES
R14	R50-0010-123	RES,SIP, 12K 10PIN
R15	R50-0010-123	RES,SIP, 12K 10PIN
R16	R50-0010-123	RES,SIP, 12K 10PIN
R17	R50-0010-123	RES,SIP, 12K 10PIN
R18	R50-0010-123	RES,SIP, 12K 10PIN
R19	R50-0010-123	RES,SIP, 12K 10PIN
R21	R50-0010-472	RES,10SIP,4.7K,2.0%, 9RES
R22	RCR07G562JM	RES,5.6K 5% 1/4W CAR COMP
R23	RCR07G181JM	RES,180 5% 1/4W CAR COMP
R24	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
R25	RCR07G243JM	RES,24K 5% 1/4W CAR COMP
U1	I27-0011-001	DIGITAL SIGNAL PROCESSOR
U2	I15-0000-244	IC 74HC244 PLASTIC CMOS
U3	I15-0000-244	IC 74HC244 PLASTIC CMOS
U4	I15-0000-373	IC 74HC373 PLASTIC CMOS
U5	I15-0000-373	IC 74HC373 PLASTIC CMOS
U6	I15-0000-373	IC 74HC373 PLASTIC CMOS
U7	I15-0000-373	IC 74HC373 PLASTIC CMOS
U8	I15-0000-245	IC 74HC245 PLASTIC CMOS
U9	I15-0000-245	IC 74HC245 PLASTIC CMOS
U10	I15-0000-373	IC 74HC373 PLASTIC CMOS
U11	I58-0007-001	IC,BUS ARBITER
U12	I58-0008-001	BUS CONTROLLER
U13	I58-0008-001	BUS CONTROLLER
U14	I15-0000-373	IC 74HC373 PLASTIC CMOS
U15	I15-0000-245	IC 74HC245 PLASTIC CMOS
U16	I15-0000-245	IC 74HC245 PLASTIC CMOS
U17	I15-0000-138	IC 74HC138 PLASTIC CMOS
U18	I28-0001-001	IC 8259 INTERRUPT CONTROL
U19	I15-0000-259	ADD ,LATCH
U20	I26-0017-001	IC STATIC RAM CMOS 8KX8
U21	I26-0017-001	IC STATIC RAM CMOS 8KX8
U26,U27	*SEE NOTE	
U28	I35-0008-001	SYSTEM TIMING CONTROLLER
U29	I15-0000-000	IC 74HC00 PLASTIC CMOS
U30	I15-0000-032	IC 74HC32 PLASTIC CMOS
U31	I15-0000-004	IC 74HC04 PLASTIC CMOS
XU1	J75-0011-068	IC SOCKET/COVER, 68 PIN

\*NOTE: When ordering replacement PROMs, refer to the part number (P/N) and the four-digit firmware number on the PROM label.

**Table 6-7. Decoder PWB Assembly A7 (10133-2450-01, Rev. B) Parts List (Cont.)**

Ref. Desig.	Part Number	Description
XU20	J77-0008-006	SOCKET, IC, 28 PIN
XU21	J77-0008-006	SOCKET, IC, 28 PIN
XU22	J77-0008-006	SOCKET, IC, 28 PIN
XU23	J77-0008-006	SOCKET, IC, 28 PIN
XU24	J77-0008-006	SOCKET, IC, 28 PIN
XU25	J77-0008-006	SOCKET, IC, 28 PIN
XU26	J77-0008-006	SOCKET, IC, 28 PIN
XU27	J77-0008-006	SOCKET, IC, 28 PIN
XU28	J77-0008-007	SOCKET, 40PIN
Y1	Y15-0004-160	CRYSTAL, 16 MHZ

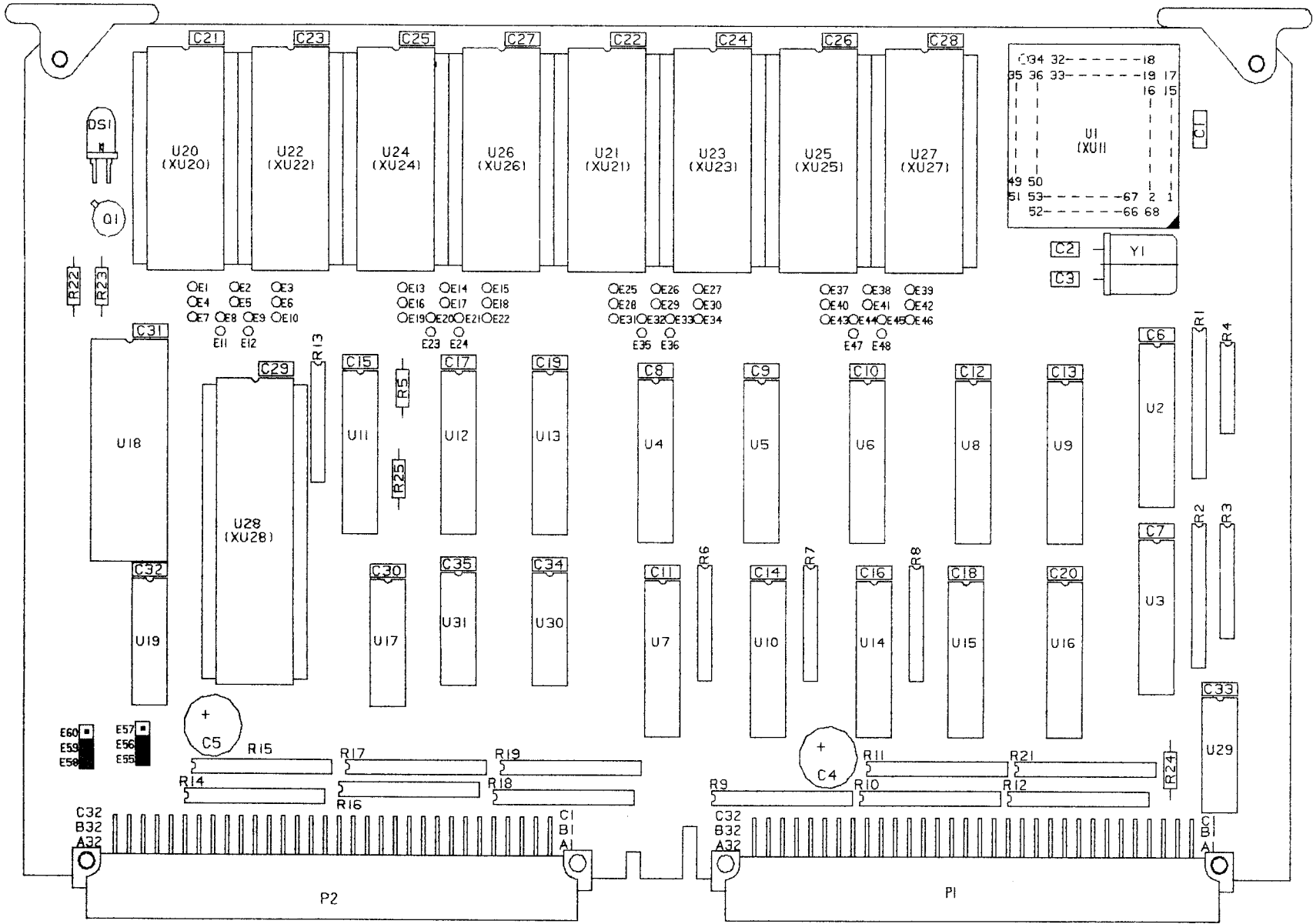


Figure 6-12. Decoder PWB Assembly A7 (10133-2450, Rev. E)

NOTE: UNLESS OTHERWISE SPECIFIED:

- 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR A COMPLETE DESIGNATION. PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
- 2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W,  $\pm 5\%$ .
- 3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
- 4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

UNUSED GATES

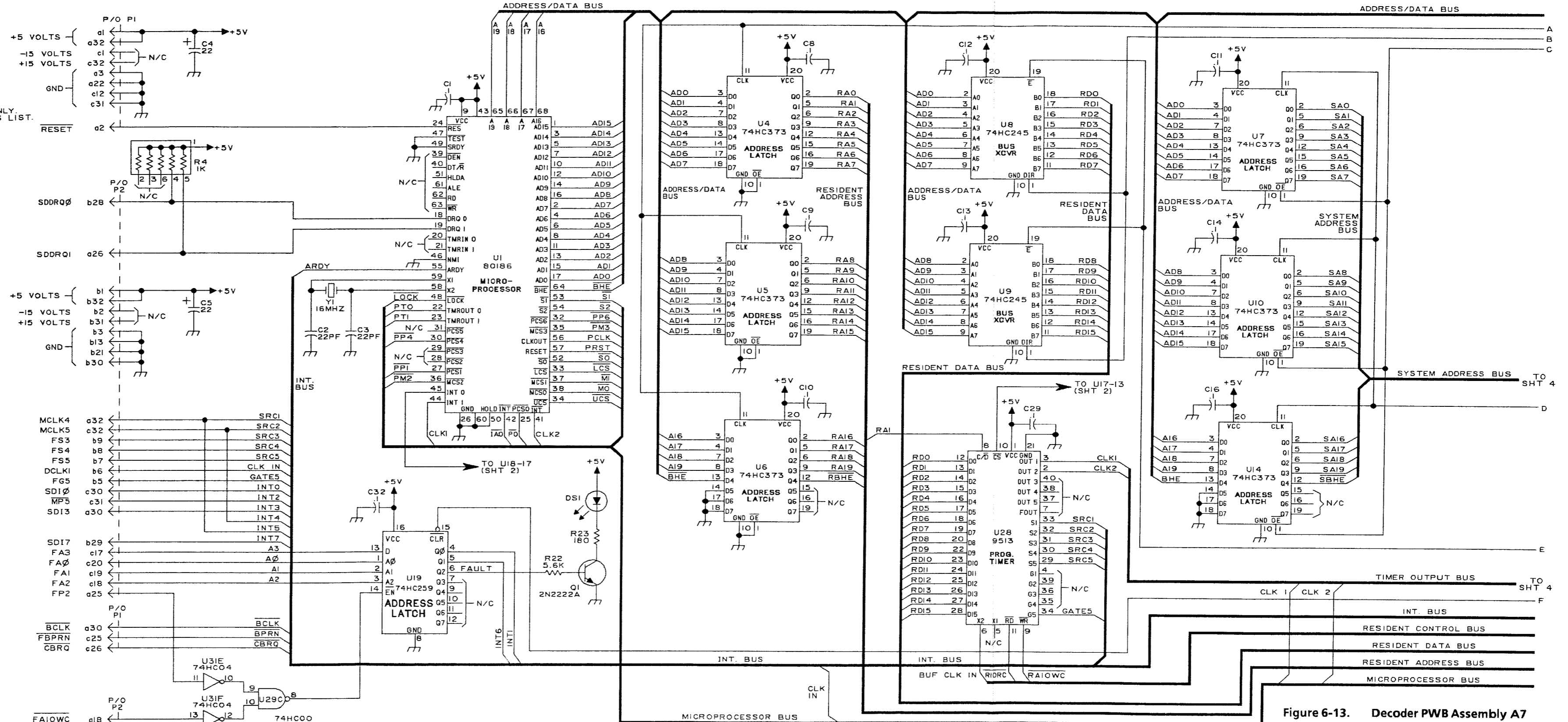
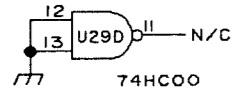


Figure 6-13. Decoder PWB Assembly A7 Schematic Diagram (10133-2451, Rev. D) (Sheet 1 of 4)

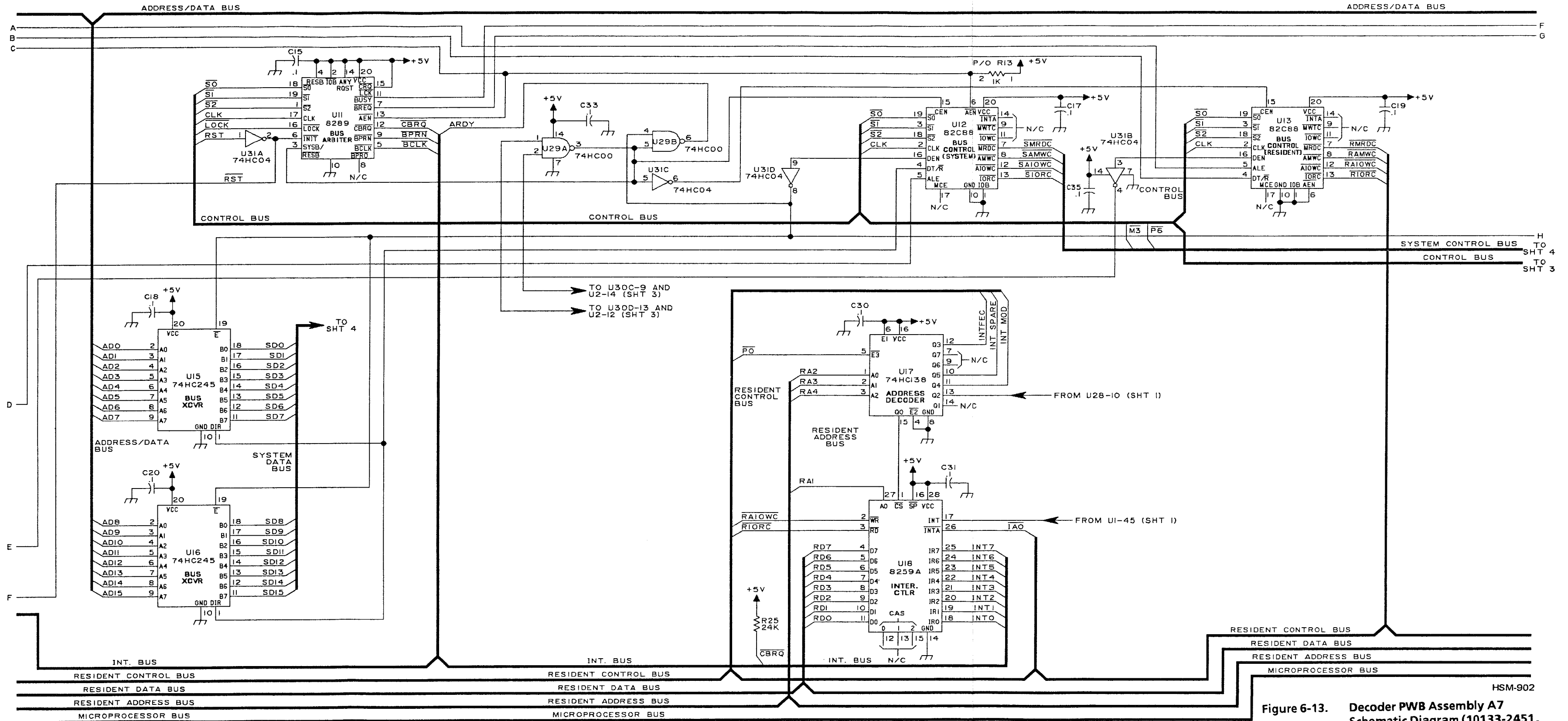


Figure 6-13. Decoder PWB Assembly A7 Schematic Diagram (10133-2451, Rev. D) (Sheet 2 of 4)

HSM-902

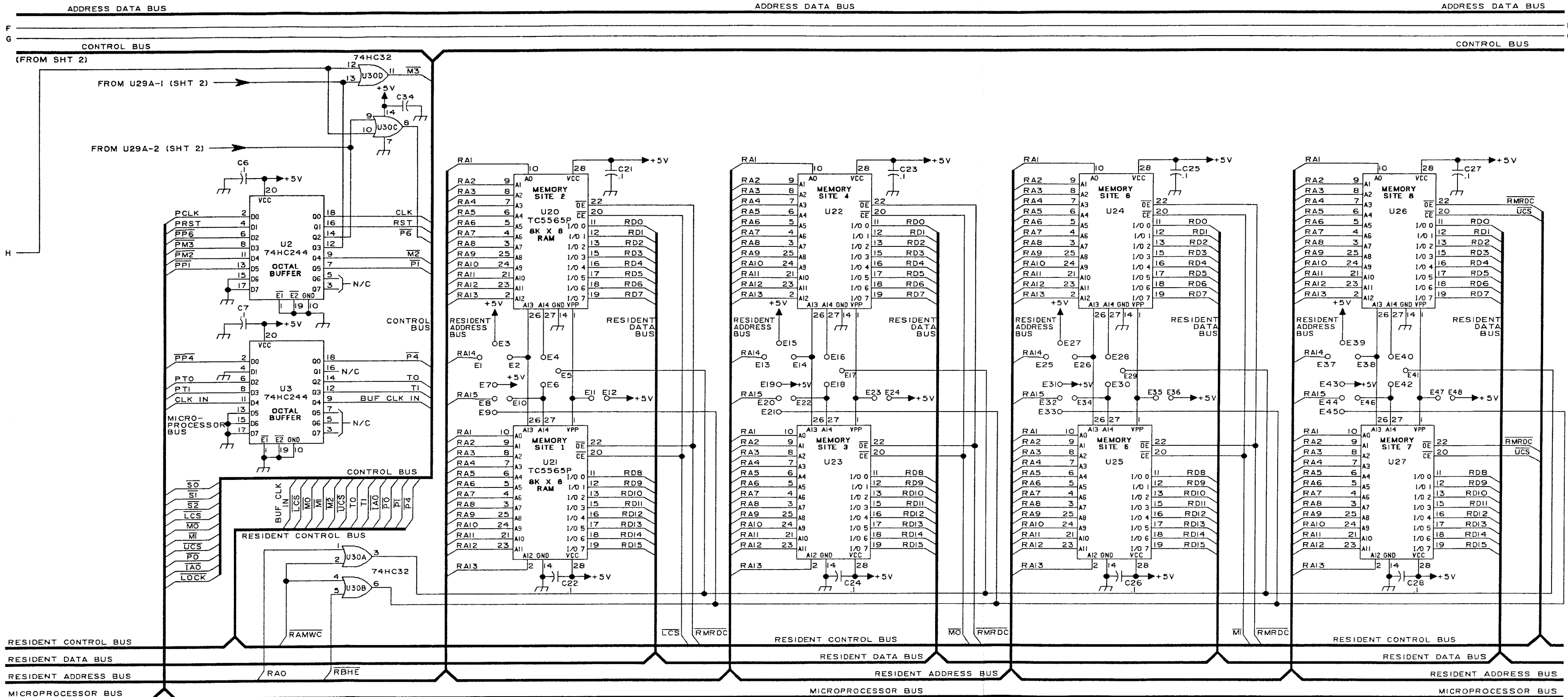


Figure 6-13. Decoder PWB Assembly A7 Schematic Diagram (10133-2451, Rev. D) (Sheet 3 of 4)

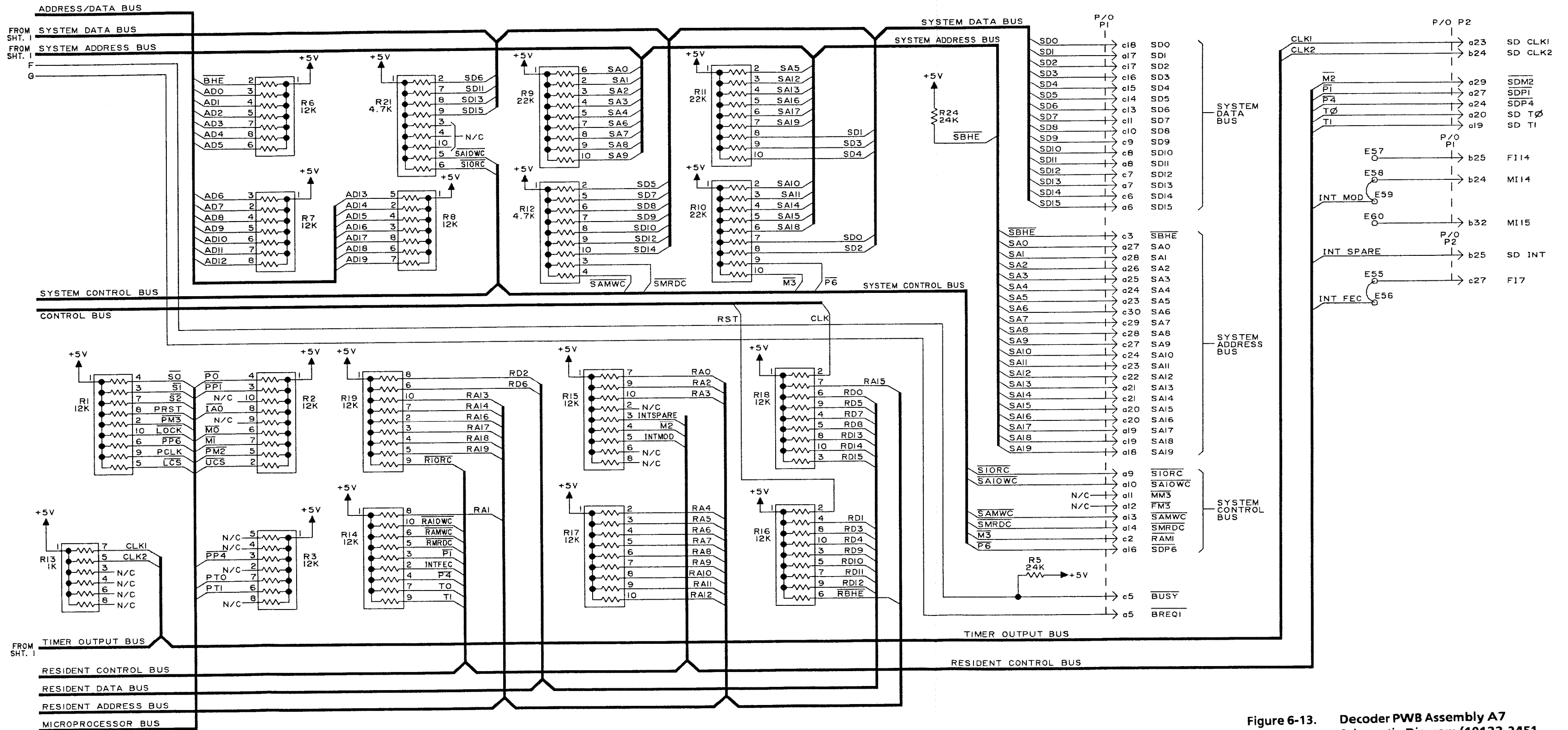


Figure 6-13. Decoder PWB Assembly A7 Schematic Diagram (10133-2451, Rev. D) (Sheet 4 of 4)

Table 6-8. Digital I/O PWB Assembly A8 (10133-2800-01, Rev. B) Parts List

Ref. Desig.	Part Number	Description
	Z71-0001-001	CARD EXTRACTOR
C1	C10-0003-012	CAP, .1UF
C2	C10-0003-012	CAP, .1UF
C4	C10-0003-012	CAP, .1UF
C5	C10-0003-012	CAP, .1UF
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C10-0003-012	CAP, .1UF
C12	C10-0003-012	CAP, .1UF
C14	C10-0003-012	CAP, .1UF
C16	C10-0003-012	CAP, .1UF
C17	C10-0003-012	CAP, .1UF
C18	C10-0003-012	CAP, .1UF
C19	C10-0003-012	CAP, .1UF
C20	C10-0003-012	CAP, .1UF
C21	C10-0003-012	CAP, .1UF
C22	C10-0003-012	CAP, .1UF
C23	C10-0003-012	CAP, .1UF
C24	C10-0003-012	CAP, .1UF
C25	C10-0003-012	CAP, .1UF
C26	C10-0003-012	CAP, .1UF
C27	C10-0003-012	CAP, .1UF
C28	C10-0003-012	CAP, .1UF
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	M39014/02-1298	CAP, .01UF, 10%200V, CER-R
C33	M39014/02-1298	CAP, .01UF, 10%200V, CER-R
C34	C26-0035-220	CAP 22UF 20% 35V TANT
C35	C26-0035-220	CAP 22UF 20% 35V TANT
C36	C26-0035-220	CAP 22UF 20% 35V TANT
C37	C26-0035-220	CAP 22UF 20% 35V TANT
C38	C26-0035-220	CAP 22UF 20% 35V TANT
C39	C26-0035-220	CAP 22UF 20% 35V TANT
C40	C26-0010-100	CAP 10UF 20% 10V TANT
C41	C10-0003-012	CAP, .1UF
C42	CK05BX331K	CAP 330PF 10% 200V CER
C43	CK05BX331K	CAP 330PF 10% 200V CER
C44	C10-0003-012	CAP, .1UF
C45	C10-0003-012	CAP, .1UF
C46	C10-0003-012	CAP, .1UF
CR1	1N3611	DIODE, GP, 1A, 200V

Table 6-8. Digital I/O PWB Assembly A8 (10133-2800-01, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
CR2	JAN1N914	DIODE
CR3	JAN1N914	DIODE
CR4	1N4148	DIODE,SILICON
CR5	1N4148	DIODE,SILICON
DS1	N21-0008-000	DIODE, LIGHT EMITTING
J1	J-0031	CONNECTOR, COAX, SNAP-ON
J2	J42-0003-004	CONN, 7 PIN, MALE
J3	J46-0013-026	HEADER ASSY, 26 PIN
P1	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
P2	J71-9600-196	CONN,96PIN,RT,ANGLE,MALE
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	RCR07G181JM	RES,180 5% 1/4W CAR COMP
R2	RCR07G562JM	RES,5.6K 5% 1/4W CAR COMP
R3	RN55D1212F	RES,12.1K 1% 1/8W MET FLM
R4	RN55D1212F	RES,12.1K 1% 1/8W MET FLM
R5	RCR07G563JM	RES,56K 5% 1/4W CAR COMP
R6	R50-0006-123	RES,SIP,12K, 6PIN
R7	R50-0008-123	RES,SIP,12K, 8PIN
R8	R50-0006-123	RES,SIP,12K, 6PIN
R9	R50-0006-123	RES,SIP,12K, 6PIN
R10	R50-0010-123	RES,SIP, 12K 10PIN
R11	R50-0010-123	RES,SIP, 12K 10PIN
R12	R50-0010-123	RES,SIP, 12K 10PIN
R13	R50-0010-123	RES,SIP, 12K 10PIN
R14	R50-0010-123	RES,SIP, 12K 10PIN
R15	R50-0010-123	RES,SIP, 12K 10PIN
R16	R50-0006-123	RES,SIP,12K, 6PIN
R17	R50-0006-123	RES,SIP,12K, 6PIN
S1	S06-0002-116	SW,PB,SPST,NO,MOM,RA,PCMT
S2	S50-0001-008	SW,SPST, 8SEC,.1A,SLD,DIP
S3	S50-0001-008	SW,SPST, 8SEC,.1A,SLD,DIP
S4	S50-0001-008	SW,SPST, 8SEC,.1A,SLD,DIP
S5	S50-0001-008	SW,SPST, 8SEC,.1A,SLD,DIP
S6	S50-0001-008	SW,SPST, 8SEC,.1A,SLD,DIP
S7	S50-0001-008	SW,SPST, 8SEC,.1A,SLD,DIP
TP1	J65-0009-002	TEST POINT
TP2	J65-0009-002	TEST POINT
TP3	J65-0009-002	TEST POINT
U1	I15-0000-259	ADD ,LATCH
U2	I15-0000-004	IC 74HC04 PLASTIC CMOS
U4	I15-0000-074	IC 74HC74 PLASTIC CMOS
U5	I15-0000-000	IC 74HC00 PLASTIC CMOS
U6	I15-0000-004	IC 74HC04 PLASTIC CMOS
U7	I15-0000-032	IC 74HC32 PLASTIC CMOS
U8	I15-0000-032	IC 74HC32 PLASTIC CMOS
U9	I15-0000-032	IC 74HC32 PLASTIC CMOS
U10	I15-0000-008	IC 74HC08 PLASTIC CMOS
U11	I15-0000-161	IC,BINARY COUNTER

Table 6-8. Digital I/O PWB Assembly A8 (10133-2800-01, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
U12	I26-0028-002	IC, RAM 32K X 8
U14	I26-0028-002	IC, RAM 32K X 8
U16	I15-0000-138	IC 74HC138 PLASTIC CMOS
U17	I15-0000-138	IC 74HC138 PLASTIC CMOS
U18	I36-0003-000	ENCODER
U19	I59-0002-000	IC 8251A
U20	I59-0002-000	IC 8251A
U21	I59-0002-000	IC 8251A
U22	I15-0000-157	IC 74HC157 PLASTIC CMOS
U23	I59-0011-001	IC, PROG, INTERFACE
U24	I15-0000-163	BINARY COUNTER
U25	I15-0000-163	BINARY COUNTER
U26	I15-0000-244	IC 74HC244 PLASTIC CMOS
U27	I15-0000-244	IC 74HC244 PLASTIC CMOS
U28	I15-0000-244	IC 74HC244 PLASTIC CMOS
U29	I15-0000-244	IC 74HC244 PLASTIC CMOS
U30	I15-0000-244	IC 74HC244 PLASTIC CMOS
U31	I15-0000-244	IC 74HC244 PLASTIC CMOS
U32	I16-0001-000	IC 1488 CERAMIC DTL
U33	I17-0001-000	IC 1489 CERAMIC DTL
U34	I15-0000-011	IC 74HC11 PLASTIC CMOS
XU12	J77-0008-006	SOCKET, IC, 28 PIN
XU14	J77-0008-006	SOCKET, IC, 28 PIN
XU23	J77-0008-007	SOCKET, 40PIN

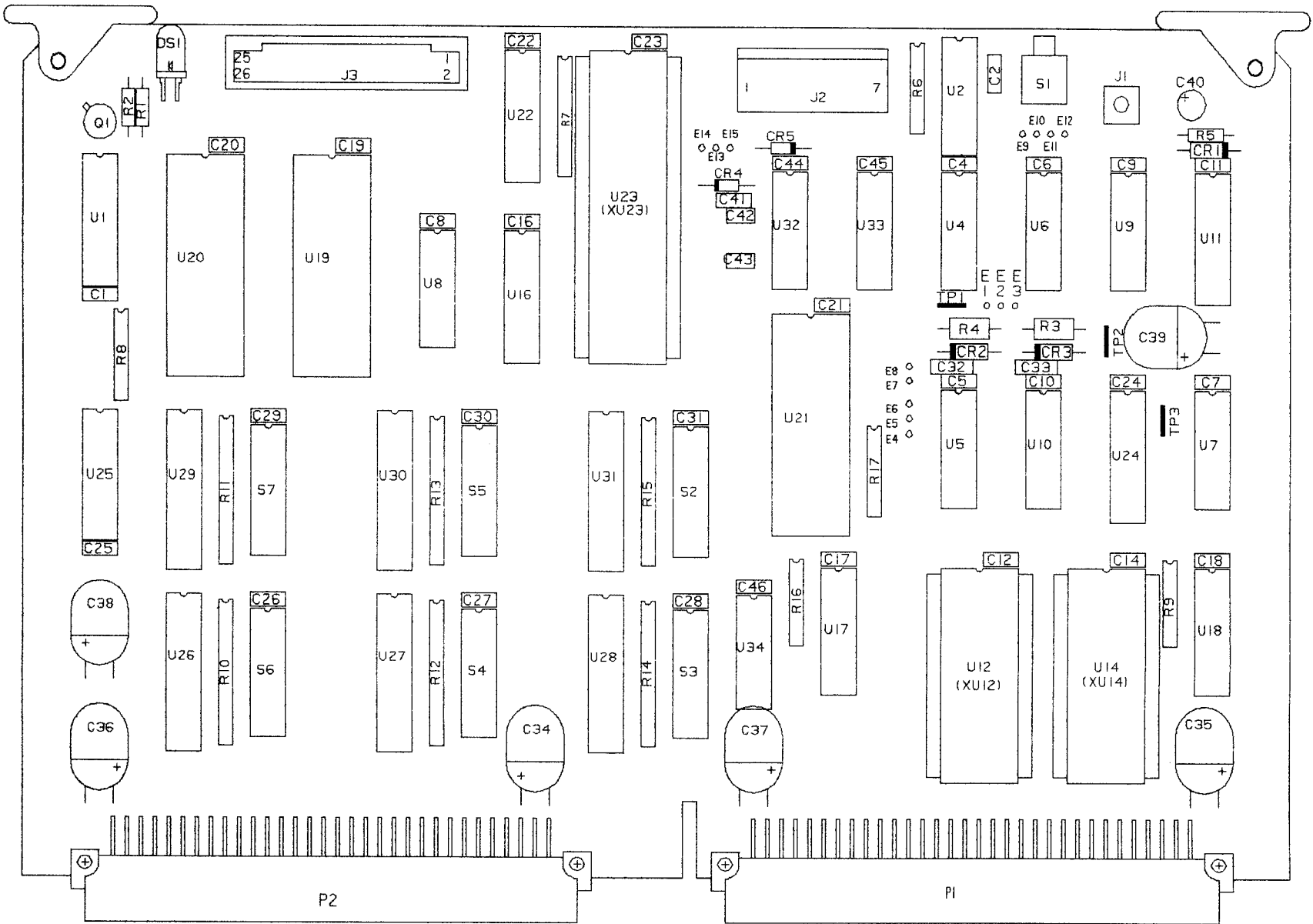


Figure 6-14. Digital I/O PWB Assembly A8 Component Locations (10133-2800, Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
- ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
- ALL CAPACITOR VALUES ARE IN MICROFARADS.
- VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
- JUMPERING CONFIGURATION:

A6 FIRMWARE		JUMPERING			
210B AND EARLIER	E9 TO E10	E11 TO E12	E13 TO E15	E5 TO E6	
213B AND LATER	E9 TO E12	E13 TO E14	E5 TO E6		
251B AND LATER	E4 TO E5	E7 TO E8	E9 TO E12	E13 TO E14	

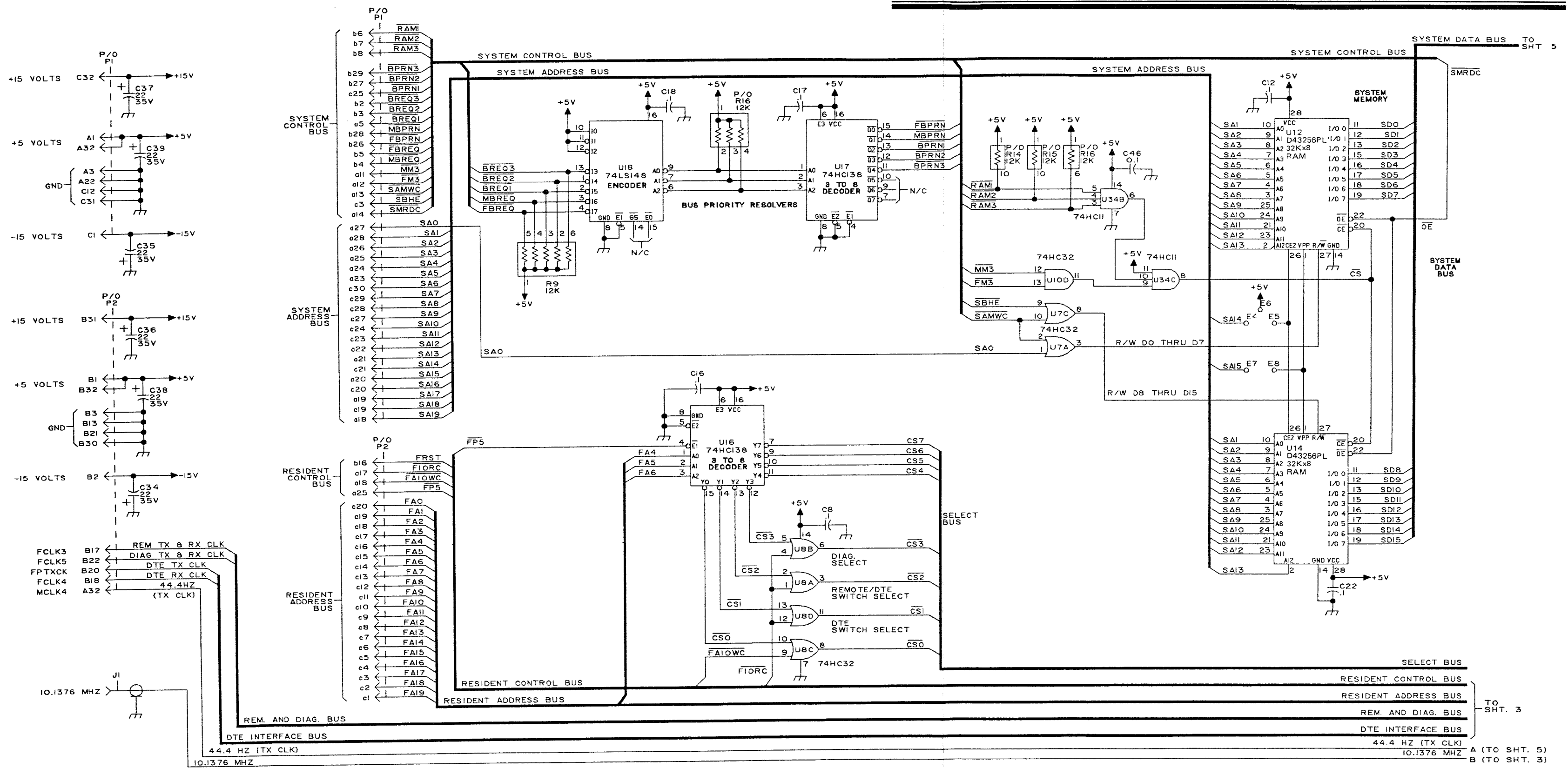
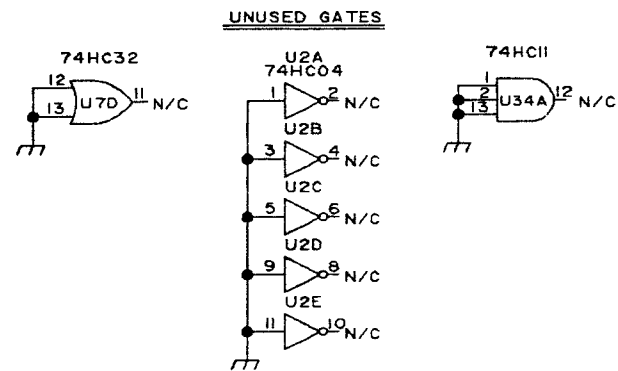


Figure 6-15. Digital I/O PWB Assembly A8 Schematic Diagram (10133-2801, Rev. J) (Sheet 1 of 5)

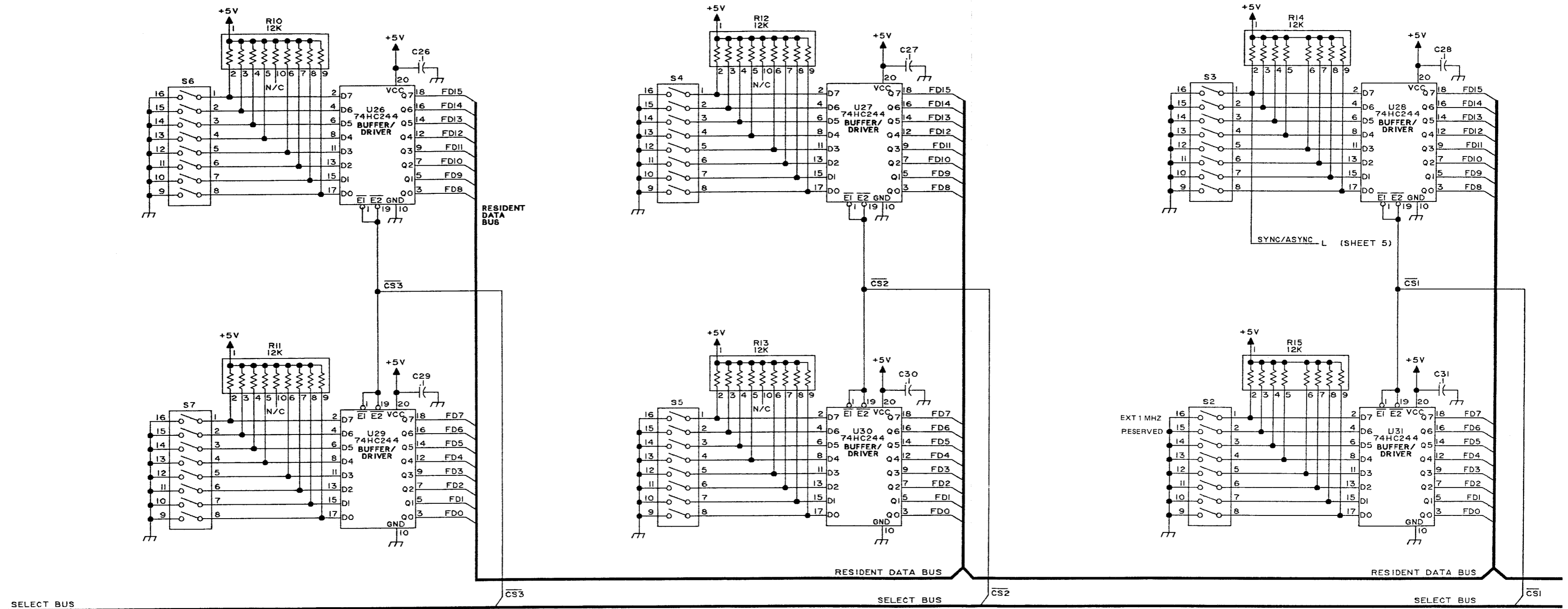


Figure 6-15. Digital I/O PWB Assembly A8  
Schematic Diagram (10133-2801,  
Rev. J) (Sheet 2 of 5)

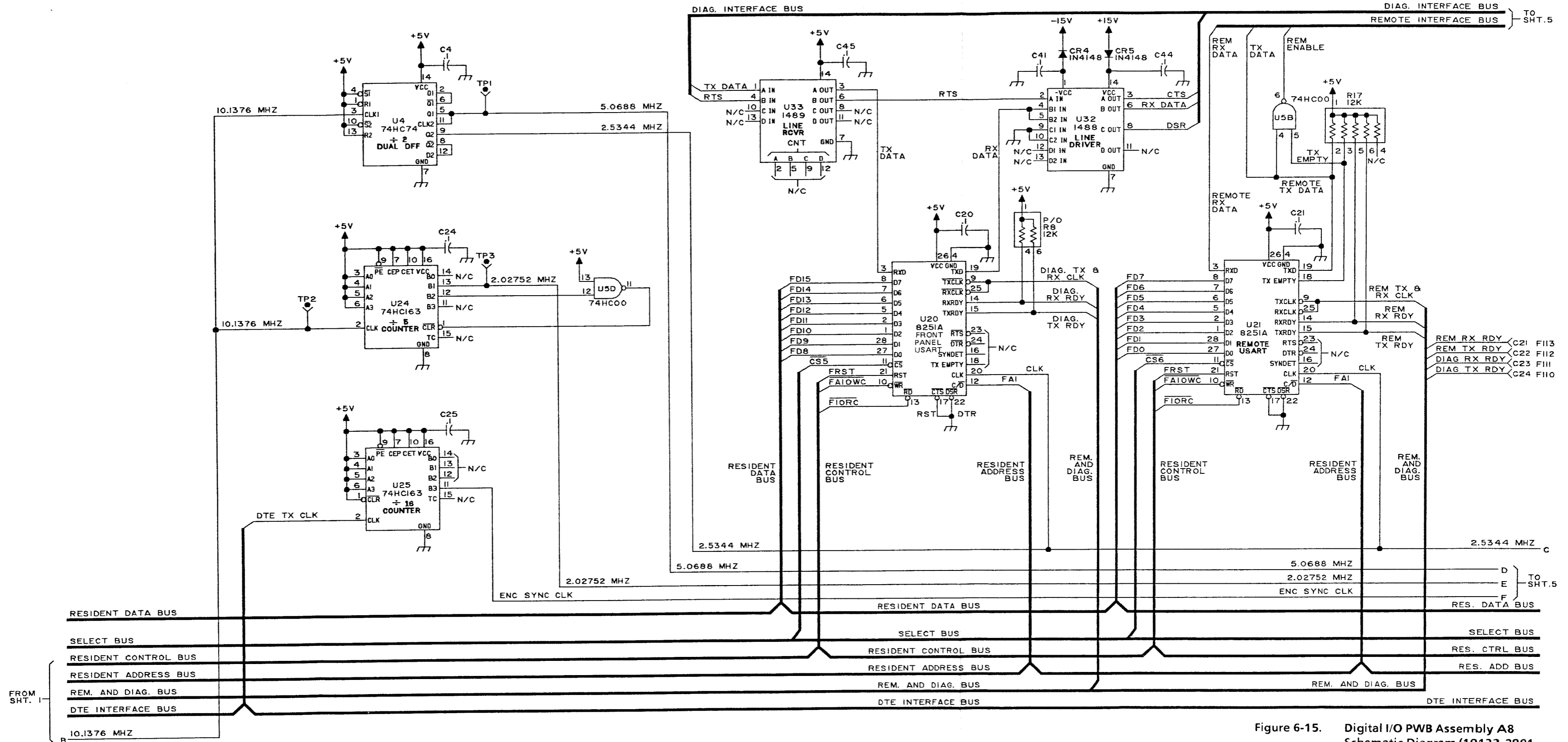


Figure 6-15. Digital I/O PWB Assembly A8 Schematic Diagram (10133-2801, Rev. J) (Sheet 3 of 5)

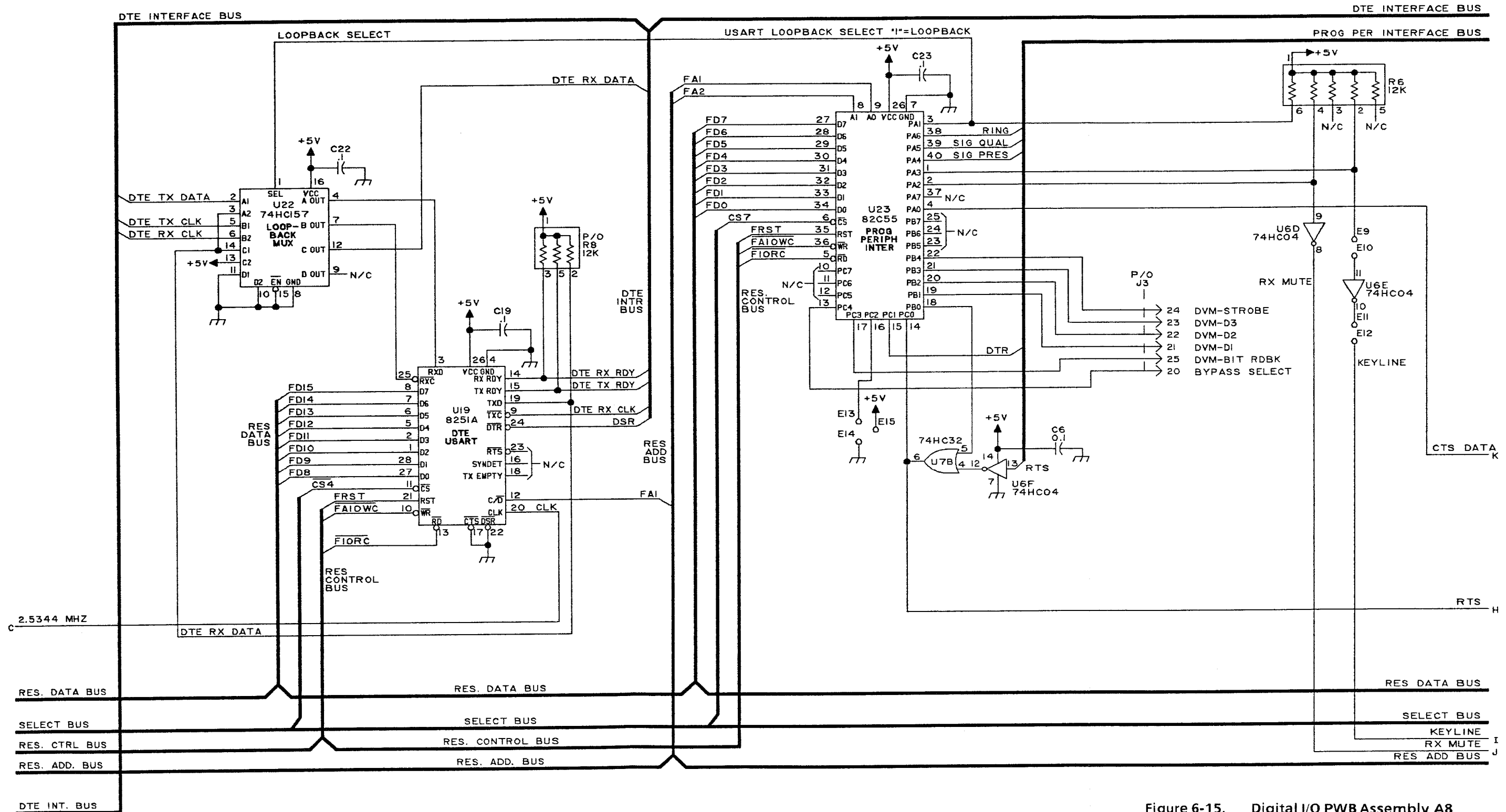


Figure 6-15. Digital I/O PWB Assembly A8 Schematic Diagram (10133-2801, Rev. J) (Sheet 4 of 5)

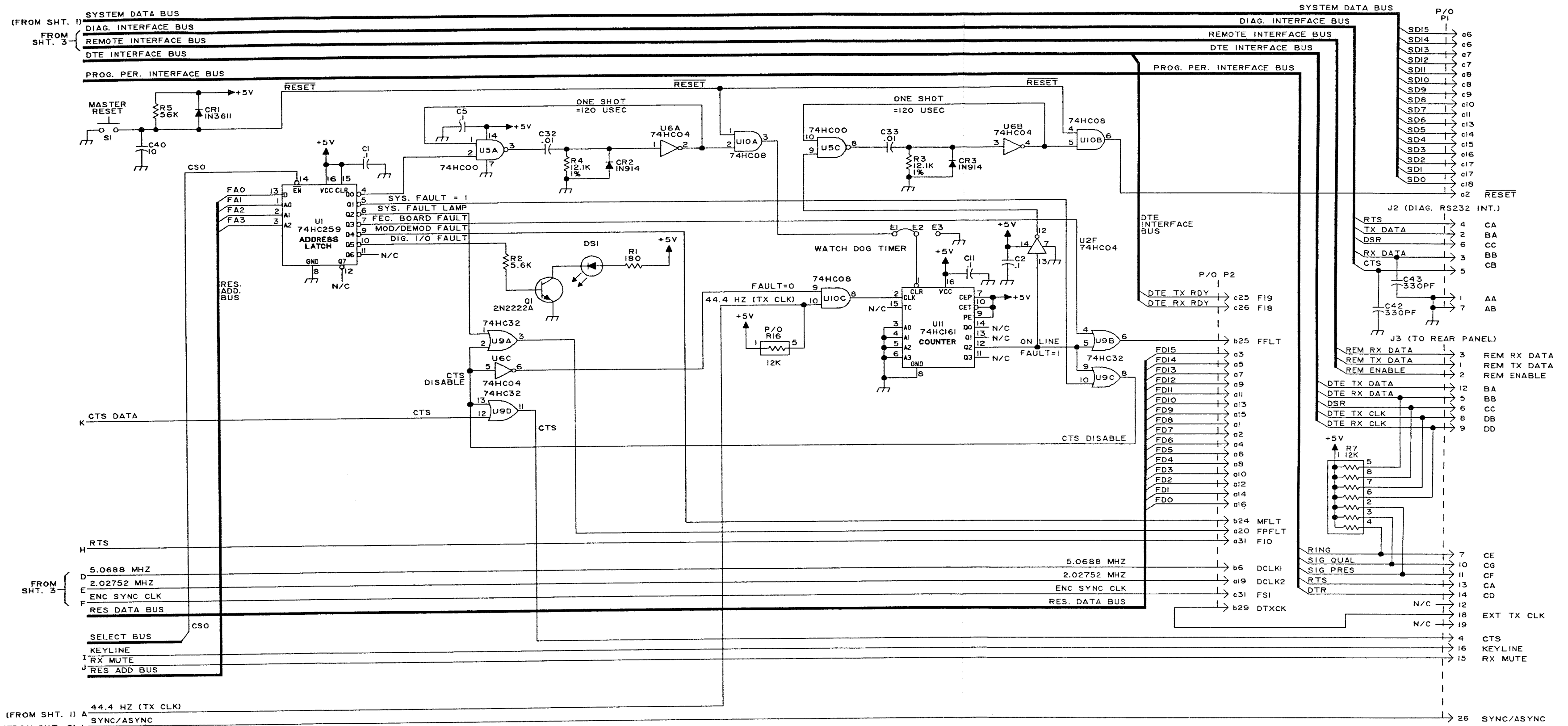


Figure 6-15. Digital I/O PWB Assembly A8 Schematic Diagram (10133-2801, Rev. J) (Sheet 5 of 5)

Table 6-9. Power Supply Assembly A9 (10133-1200, Rev. E) Parts List

Ref. Desig.	Part Number	Description
A1	10133-1220	POWER SUPPLY AC
A2	10133-1320	EMI FILTER ASSV
CR1	D24-0001-002	RECTIFIER,30,A HIGH EFFIC
CR2	D24-0001-002	RECTIFIER,30,A HIGH EFFIC

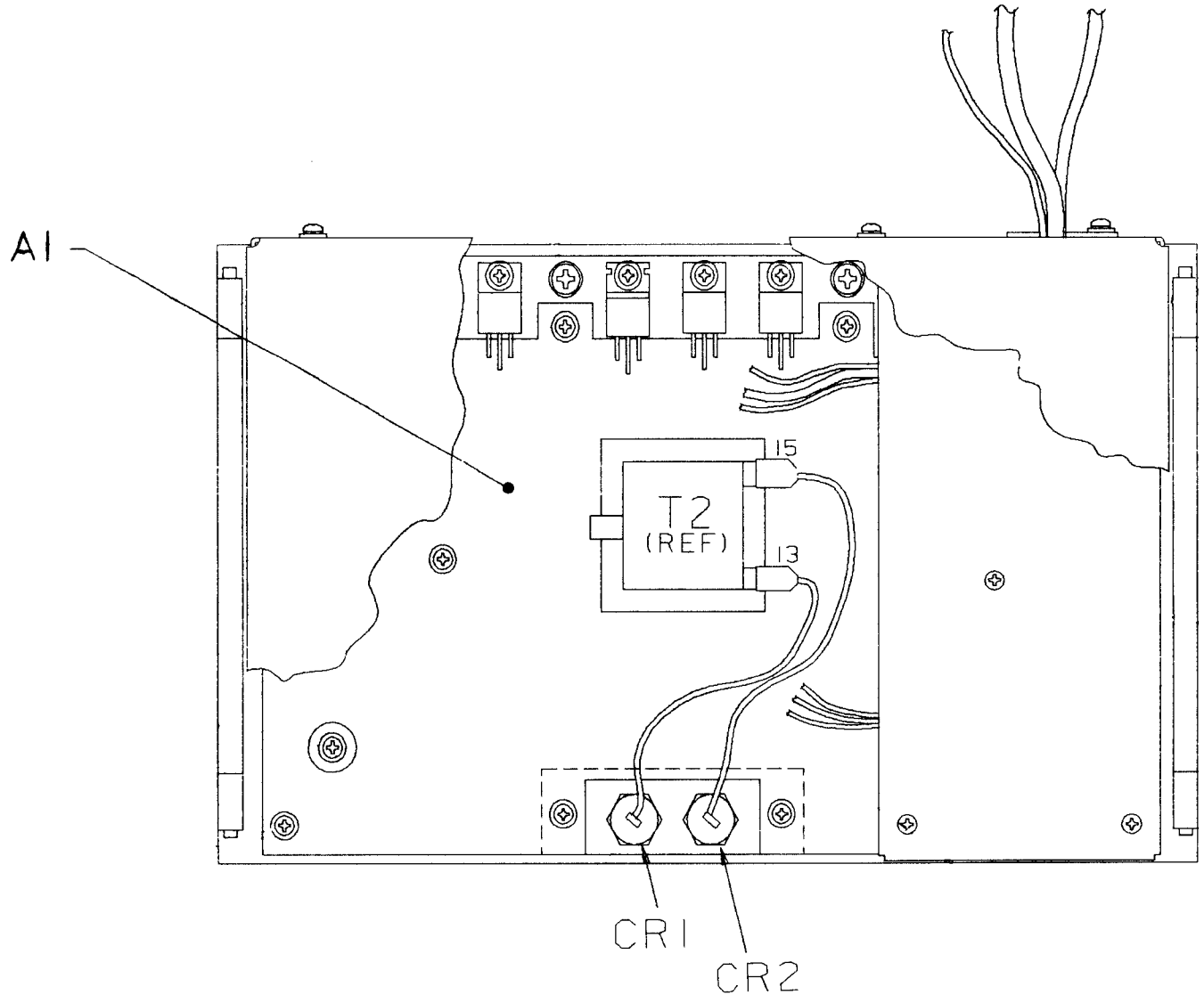


Figure 6-16. Power Supply Assembly Component Locations (10133-1200, Rev. D)

Table 6-10. Power Supply PWB Assembly A9A1 (10133-1220, Rev. N) Parts List

Ref. Desig.	Part Number	Description
	M39014/02-1310	CAP .1UF 10% 100V CER-R
	M10-0006-001	INSULATOR, TRANSISTOR
	M08-0001-051	INSULATOR, TRANSISTOR
	M10-0006-000	INSULATOR, TRANSISTOR
C1	C28-0250-221	CAP., 220UF, 250V
C2	C28-0250-221	CAP., 220UF, 250V
C3	C28-0250-221	CAP., 220UF, 250V
C4	C28-0250-221	CAP., 220UF, 250V
C5	C73-2050-221	CAP, 220 UF, 50V
C7	M39014/02-1320	CAP .47UF 10% 50V CER-R
C8	C73-0025-680	CAP, FXD, ELCTLT, 68 UF, 25 V
C9	C73-0025-680	CAP, FXD, ELCTLT, 68 UF, 25 V
C13	C26-0025-100	CAP, 10UF 20% 25V TANT
C14	M39014/02-1320	CAP .47UF 10% 50V CER-R
C15	C-0961	100V .0047MFD TUBE
C16	M39014/02-1307	CAP .068UF
C17	CK05BX222K	CAP 2200PF 10% 100V CER
C18	C26-0025-479	CAP 4.7UF 20% 25V TANT
C19	M39014/02-1307	CAP .068UF
C22	CK05BX102K	CAP 1000PF 10% 200V CER
C23	C-8040	CAP, 56UF
C24	C11-0034-152	CAP., .0015MF, 1KV
C25	C66-0250-105	CAP., 1MF
C26	C11-0034-152	CAP., .0015MF, 1KV
C27	C66-0250-105	CAP., 1MF
C28	CK06BX472K	CAP 4700PF 10% 200V CER
C29	C28-0035-392	CAP., 3900MF, 35V
C31	M39014/02-1320	CAP .47UF 10% 50V CER-R
C32	C73-0025-680	CAP, FXD, ELCTLT, 68 UF, 25 V
C33	C28-0035-392	CAP., 3900MF, 35V
C35	M39014/02-1320	CAP .47UF 10% 50V CER-R
C36	C73-0025-680	CAP, FXD, ELCTLT, 68 UF, 25 V
C37	M39014/02-1307	CAP .068UF
C38	M39014/02-1307	CAP .068UF
C39	C28-0010-153	CAP, 15000MF, 10V
C40	C73-2015-102	CAP, FXD, ELCTLT, 1000UF, 15V
C41	C66-0250-225	CAP., 2.2UF, 250V
C43	C73-0025-470	CAP, 47UF, 25V
C45	M39014/02-1320	CAP .47UF 10% 50V CER-R
C46	C26-0025-100	CAP, 10UF 20% 25V TANT
C47	M39014/02-1305	CAP
CR1	D22-5011-008	VARO BRIDGE, VJ847
CR2	D26-0001-000	BRIDGE, RECTIFIER
CR3	1N4454	DIODE, SS SILICON
CR4	1N4454	DIODE, SS SILICON
CR5	D50-0006-006	TRANSORB

Table 6-10. Power Supply PWB Assembly A9A1 (10133-1220, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
CR6	D50-0006-006	TRANSORB
CR7	D22-0007-006	RECTIFIER, MR 816
CR8	D22-0007-006	RECTIFIER, MR 816
CR9	D24-0003-001	RECT,F.W. COMMON COTH
CR10	D24-0003-002	RECT,F.W.,COMMON
CR11	1N4007	DIODE, RECT. 1000V 1A
CR12	1N4007	DIODE, RECT. 1000V 1A
CR15	D22-0007-002	DIODE, MR811
CR16	D22-0007-002	DIODE, MR811
CR17	1N5240B	DIODE 10V 5% 0.5W ZENER
CR18	1N5711	DIODE,HOT CARRIER
CR19	1N4454	DIODE, SS SILICON
CR20	1N4454	DIODE, SS SILICON
CR21	1N4454	DIODE, SS SILICON
L1	L13-0001-331	INDUCTOR,330UH
L2	L13-0001-331	INDUCTOR,330UH
L3	L13-0001-331	INDUCTOR,330UH
L4	MS90538-12	COIL, RF 100 UH 5%
L5	10085-1268	COIL,FXD,1 MH
L6	10085-1268	COIL,FXD,1 MH
L7	10133-1240	INDUCTOR, 50 UH, 17A
L8	10133-1241	INDUCTOR, 1UH, 17A
L9	W60-0009-003	WIRE,TFE,14AWG,ORN
Q1	2N2907A	XSTR SS/GP PNP TO-18
Q2	Q25-0019-004	TRANS., POWER FET
Q3	Q25-0019-004	TRANS., POWER FET
Q4	2N2222A	XSTR SS/GP NPN TO-18
Q5	D29-0003-102	SCR., 25A, 100V
R1	RCR42G473JM	RES,47K 5% 2W CAR COMP
R2	RCR42G473JM	RES,47K 5% 2W CAR COMP
R3	RN55D2430F	RES,243.0 1% 1/8W MET FLM
R4	RN55D2611F	RES,2610 1% 1/8W MET FLM
R5	RCR07G100JM	RES,FXD,COMP,10,5% 1/4W
R6	RN55D1501F	RES,1500 1% 1/8W MET FLM
R7	RN55D3481F	RES,3480 1% 1/8W MET FLM
R8	RCR07G470JM	RES,47 5% 1/4W CAR COMP
R9	RN55D6191F	RES,6190 1% 1/8W MET FLM
R10	RN55D2742F	RES,27.4K 1% 1/8W MET FLM
R11	RN55D3481F	RES,3480 1% 1/8W MET FLM
R12	RCR07G102JM	RES,1.0K 5% 1/4W CAR COMP
R13	RCR07G472JM	RES,4.7K 5% 1/4W CAR COMP
R14	RCR07G104JM	RES,100K 5% 1/4W CAR COMP
R15	RCR07G224JM	RES,220K 5% 1/4W CAR COMP
R16	RCR07G270JM	RES,27 5% 1/4W CAR COMP
R17	RCR07G102JM	RES,1.0K 5% 1/4W CAR COMP
R18	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R19	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R20	RN55D2551F	RES,METAL,FILM,1%,1/8W

Table 6-10. Power Supply PWB Assembly A9A1 (10133-1220, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R21	RN55D4640F	RES,464.0 1% 1/8W MET FLM
R22	RN55D1501F	RES,1500 1% 1/8W MET FLM
R23	RCR07G102JM	RES,1.0K 5% 1/4W CAR COMP
R24	RN60D44R2F	RES,MTL,FLM,44.2,1%,1/4W
R25	RN55D1001F	RES,1000 1% 1/8W MET FLM
R26	RN55D1001F	RES,1000 1% 1/8W MET FLM
R27	R-2225	RES,VAR,PCB 1K .5 20%
R28	RCR07G471JM	RES,470 5% 1/4W CAR COMP
R29	RCR07G471JM	RES,470 5% 1/4W CAR COMP
R30	RCR20G471JM	RES,470 5% 1/2W CAR COMP
R31	RCR20G471JM	RES,470 5% 1/2W CAR COMP
R32	RCR32G223JM	RES,22K 5% 1W CAR COMP
R33	RCR07G270JM	RES,27 5% 1/4W CAR COMP
R34	RCR07G220JM	RES,22 5% 1/4W CAR COMP
R35	RCR07G100JM	RES,FXD,COMP,10,5% 1/4W
R36	RCR07G100JM	RES,FXD,COMP,10,5% 1/4W
R37	RCR32G470JM	RES,47 5% 1W CAR COMP
R38	RCR07G101JM	RES,FXD,COMP,100,5%,1/4W
R39	RCR07G270JM	RES,27 5% 1/4W CAR COMP
R40	RCR07G102JM	RES,1.0K 5% 1/4W CAR COMP
R41	RCR07G471JM	RES,470 5% 1/4W CAR COMP
R42	RN55D4751F	RES,4750 1% 1/8W MET FLM
R43	RN55D3481F	RES,3480 1% 1/8W MET FLM
R44	RCR07G470JM	RES,47 5% 1/4W CAR COMP
R45	RCR07G474JM	RES,470K 5% 1/4W CAR COMP
R46	RCR07G101JM	RES,FXD,COMP,100,5%,1/4W
R47	RCR07G221JM	RES,220 5% 1/4W CAR COMP
R48	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R49	RCR07G102JM	RES,1.0K 5% 1/4W CAR COMP
R50	RN55D5110F	RES,511.0 1% 1/8W MET FLM
R51	RN55D1000F	RES,100.0 1% 1/8W MET FLM
R52	R-2222	RES,VAR,PCB 100 .5 20%
R53	RCR07G100JM	RES,FXD,COMP,10,5% 1/4W
R54	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
RT1	D40-0013-010	THERMISTOR 10,3A
S1	S10-0012-111	SWITCH, DPDT
T1	10133-1245	TRANSFORMER, DRIVER
T2	10133-1246	TRANSFORMEWR, POWER
T3	L61-0001-005	XFMR,PULSE,100T CT
T4	10133-1247	TRANS., POWER
U1	I62-0005-001	REGULATOR,SG1525A
U2	I20-0008-000	IC LM239 COMPARATOR
U3	I35-0004-001	TIMER
U4	IC-0358	IC VR 317 ADJ V 1.5A
U5	I10-0007-015	POSITIVE 15V,REG.
U6	I10-0006-015	NEGATIVE,15V,REG
U7	I14-0004-001	OVER,VOLTAGE,PROTECTION

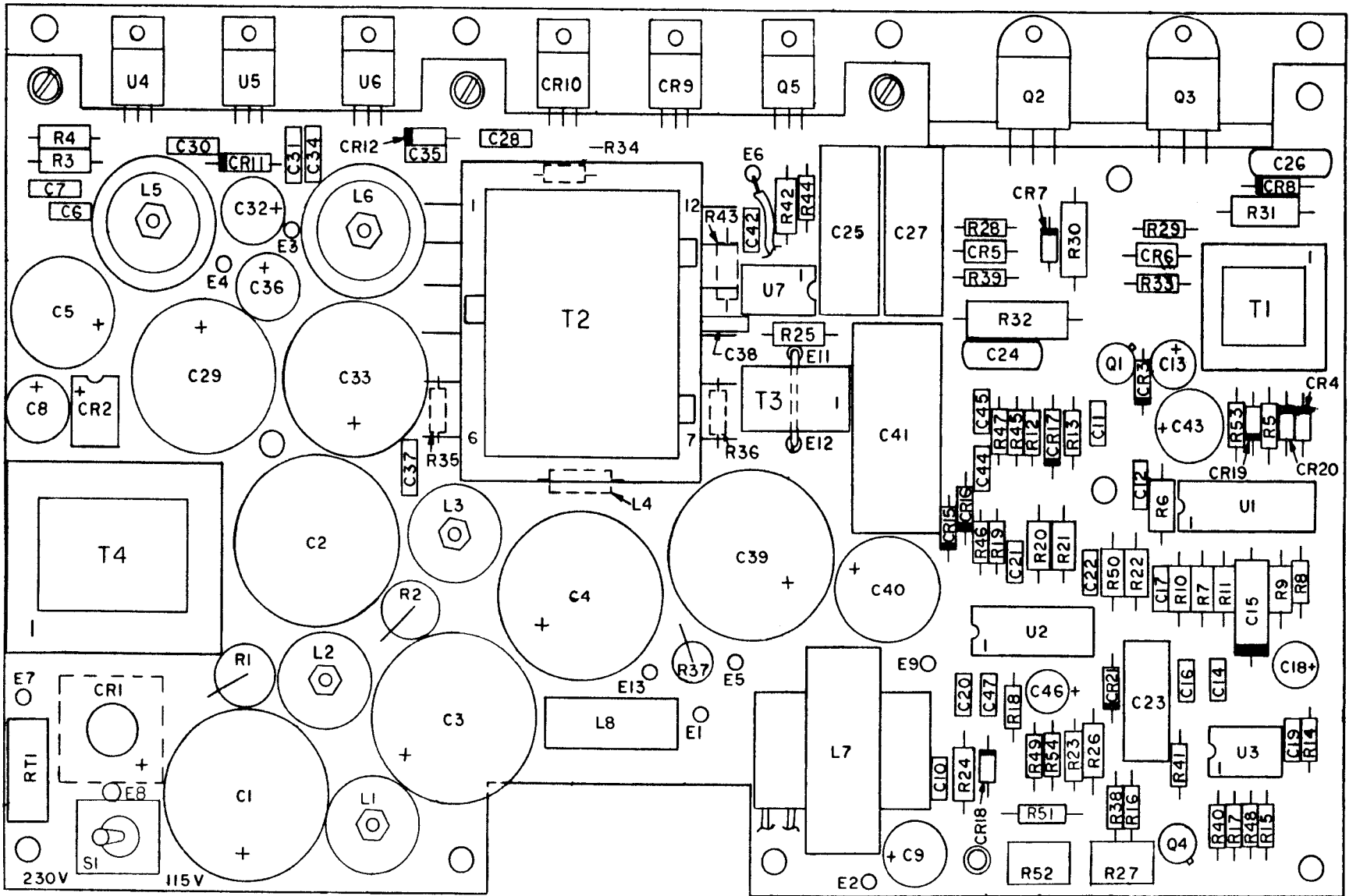


Figure 6-17. Power Supply PWB Assembly A9A1 Component Locations (10133-1220, Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

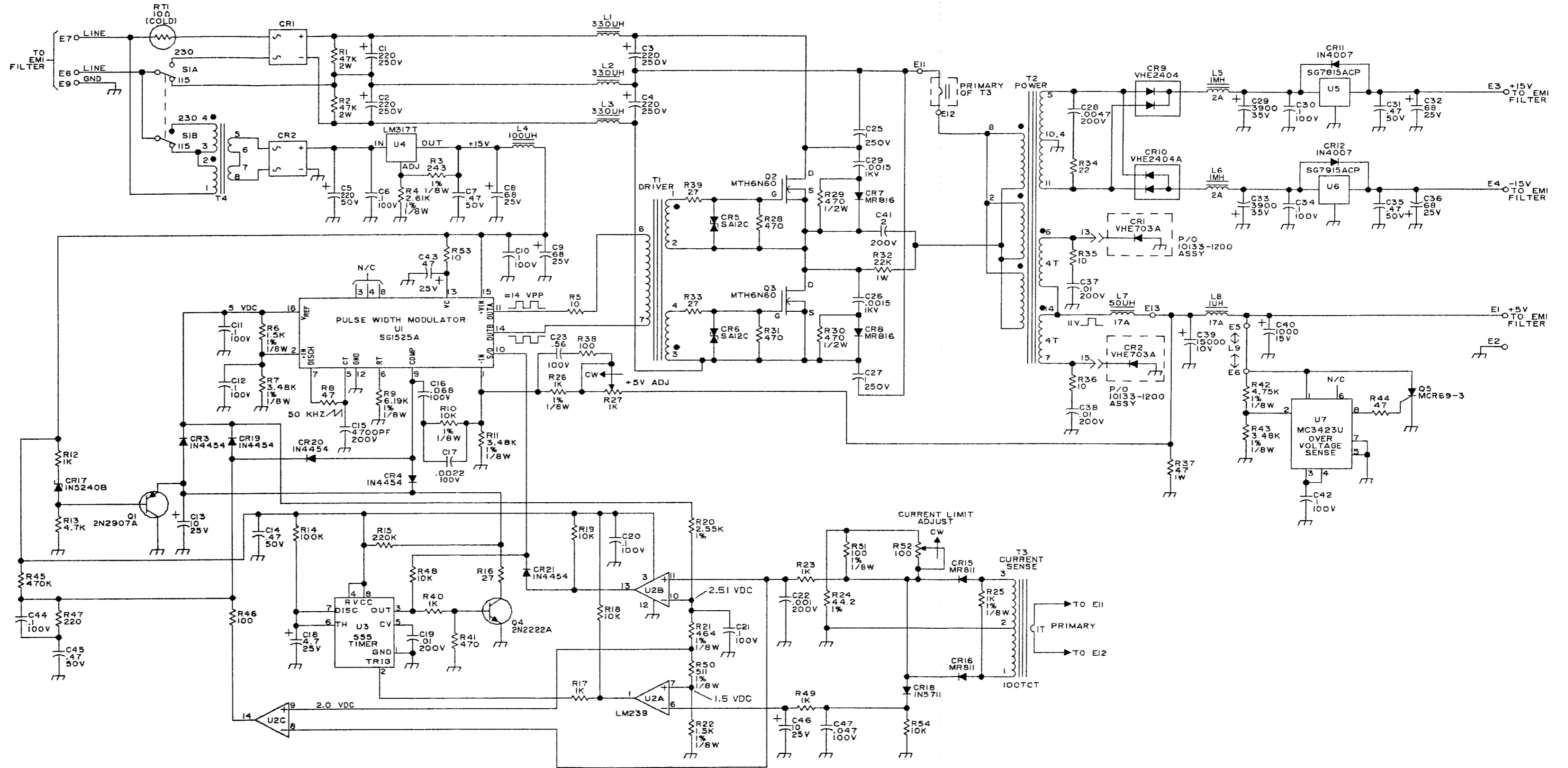
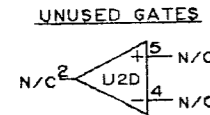


Figure 6-18. Power Supply PWB Assembly A9A1 Schematic Diagram (10133-1221, Rev. C)

Table 6-11. EMI Filter PWB Assembly A9A2A1 (10133-1300-01/-02, Rev. G) Parts List

Ref. Desig.	Part Number	Description
C1	C11-0033-103	CAP., CER., .01UF, 500V
C2	C11-0033-104	CAP., .1UF, 500V
C3	C11-0033-503	CAP., CER., .05UF, 500V
C4	C11-0033-503	CAP., CER., .05UF, 500V
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1298	CAP., .01UF, 10%200V, CER-R
C7	M39014/02-1320	CAP .47UF 10% 50V CER-R
C8	C73-1012-471	CAP, ELECTROL., 470UF, 12V
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1298	CAP., .01UF, 10%200V, CER-R
C11	M39014/02-1320	CAP .47UF 10% 50V CER-R
C12	C73-0025-680	CAP, FXD, ELCTLT, 68 UF, 25 V
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1298	CAP., .01UF, 10%200V, CER-R
C15	M39014/02-1320	CAP .47UF 10% 50V CER-R
C16	C73-0025-680	CAP, FXD, ELCTLT, 68 UF, 25 V
C17	C11-0033-104	CAP., .1UF, 500V
C18	C11-0033-104	CAP., .1UF, 500V
C19	C11-0033-104	CAP., .1UF, 500V
C20	C11-0033-104	CAP., .1UF, 500V
C21	C11-0033-104	CAP., .1UF, 500V
L1	10133-1312	INDUCTOR, COMMON-MODE, 10
L2	10133-1312	INDUCTOR, COMMON-MODE, 10
L3	10133-1310	INDUCTOR, PWR, 12UH
L4	10133-1311	INDUCTOR, PWR, 100UH
L5	10133-1311	INDUCTOR, PWR, 100UH
P1	J20-0014-004	PLUG-4-PIN
P2	J21-0001-010	CONNECTOR SHELL, 10 PIN
P3	J40-0023-003	CONNECTOR, 3 PIN
R1	RCR07G225JM	RES, 2.2M 5% 1/4W CAR COMP
R2	R65-0003-152	RES, 1.5K 5% 1/4W CAR FILM

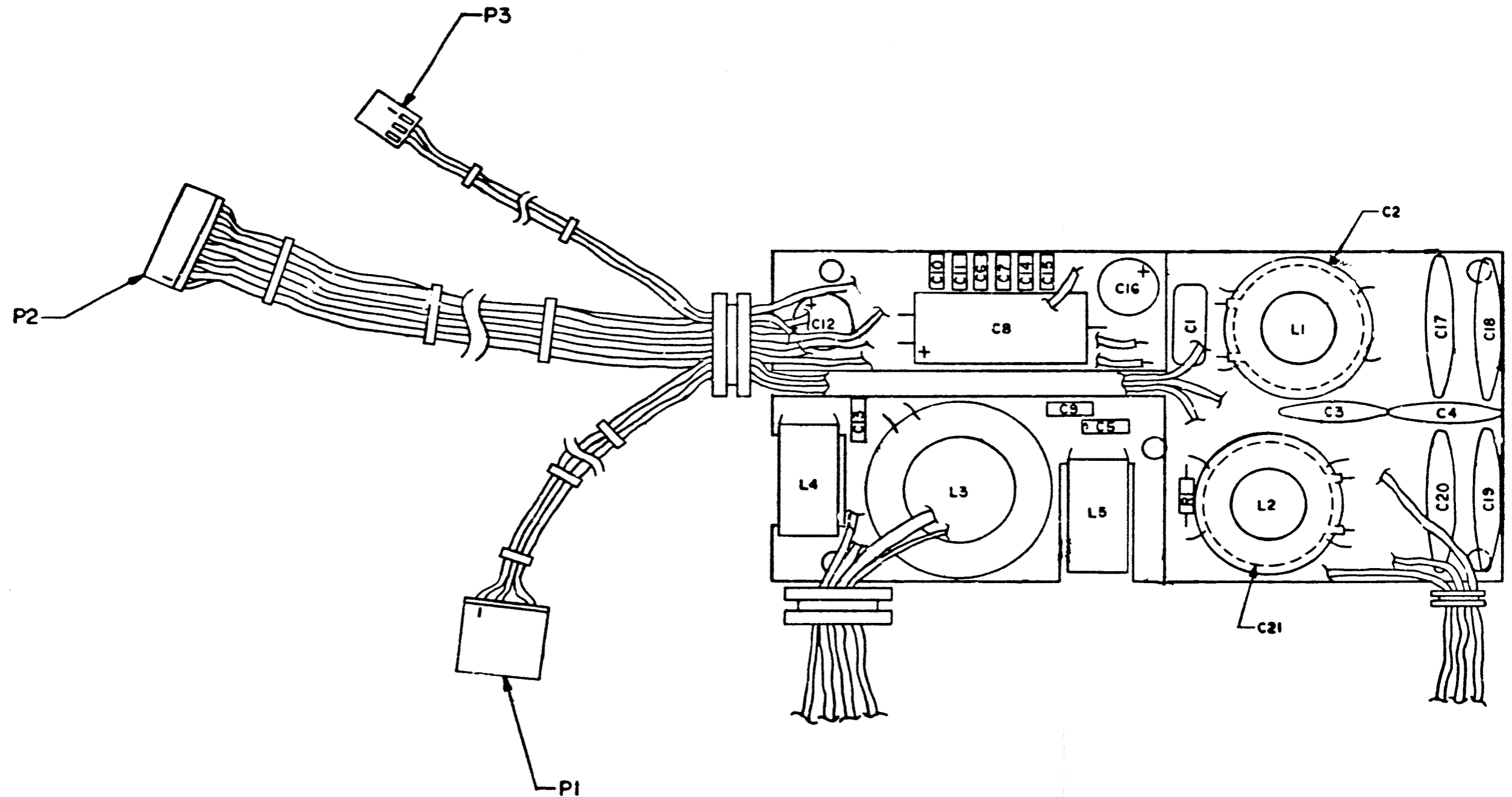


Figure 6-19. EMI Filter PWB Assembly A9A2A1  
Component Locations  
(10133-1300-01/-02, Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

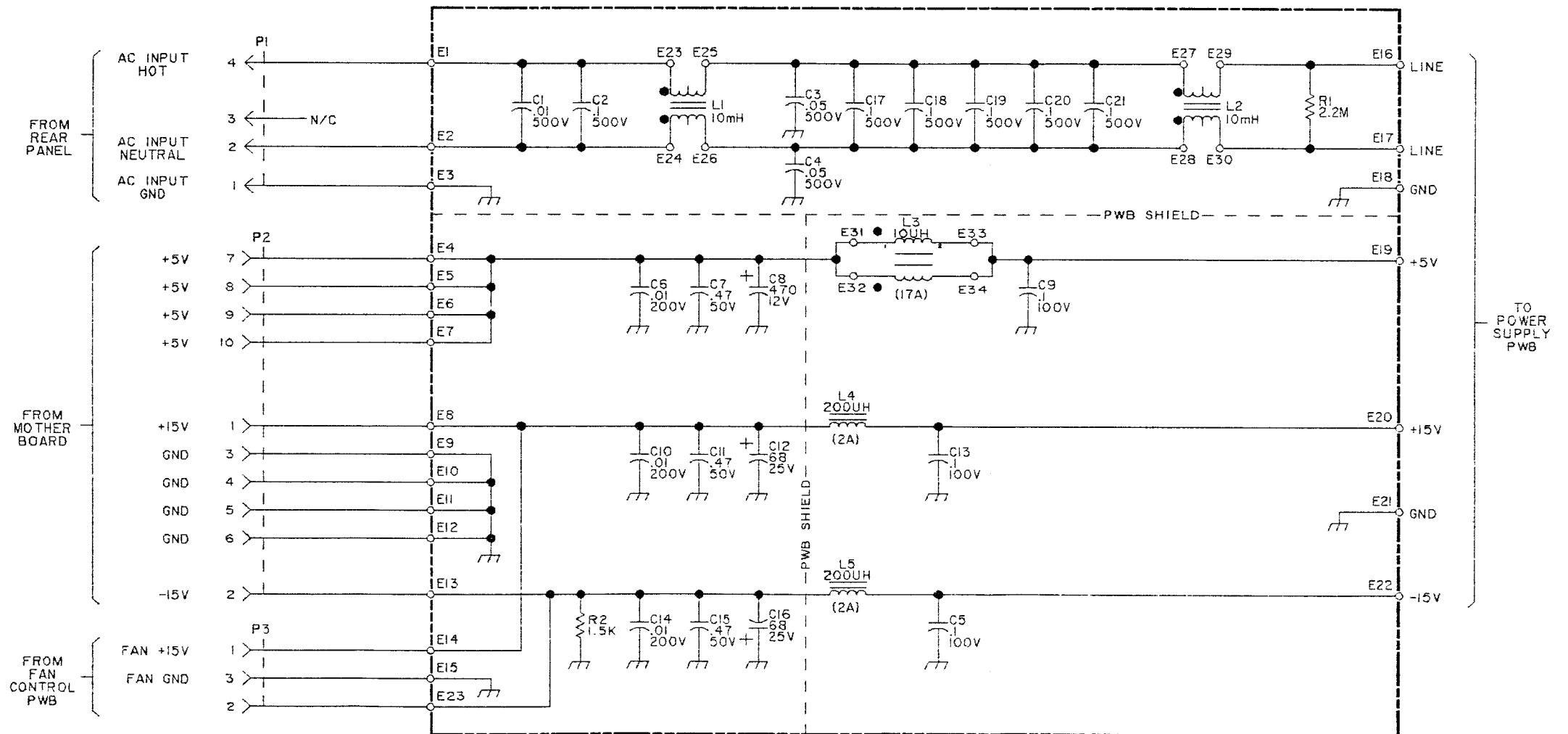


Figure 6-20. EMI Filter PWB Assembly A9A2A1 Schematic Diagram (10133-1301, Rev. C)

Table 6-12. Interconnect PWB Assembly A10 (10133-2900-01, Rev. D) Parts List

Ref. Desig.	Part Number	Description
J1	J71-9602-196	CONN.,96PIN,FEMALE
J2	J71-9602-196	CONN.,96PIN,FEMALE
J3	J71-9602-196	CONN.,96PIN,FEMALE
J4	J71-9602-196	CONN.,96PIN,FEMALE
J5	J71-9602-196	CONN.,96PIN,FEMALE
J6	J71-9602-196	CONN.,96PIN,FEMALE
J7	J71-9602-196	CONN.,96PIN,FEMALE
J8	J71-9602-196	CONN.,96PIN,FEMALE
J9	J71-9602-196	CONN.,96PIN,FEMALE
J10	J71-9602-196	CONN.,96PIN,FEMALE
J11	J71-9602-196	CONN.,96PIN,FEMALE
J12	J71-9602-196	CONN.,96PIN,FEMALE
J13	J71-9602-196	CONN.,96PIN,FEMALE
J14	J71-9602-196	CONN.,96PIN,FEMALE
J15	J71-9602-196	CONN.,96PIN,FEMALE
J16	J71-9602-196	CONN.,96PIN,FEMALE
J17	J42-0003-007	CONNECTOR, 10 PIN
J18	J42-0003-001	CONNECTOR, LOCKING, 4 PIN
P1	10133-4012	P1 RIBBON CBL ASSY,14 PIN
P2	10133-4013	P2 RIBBON CBL ASSY,40 PIN

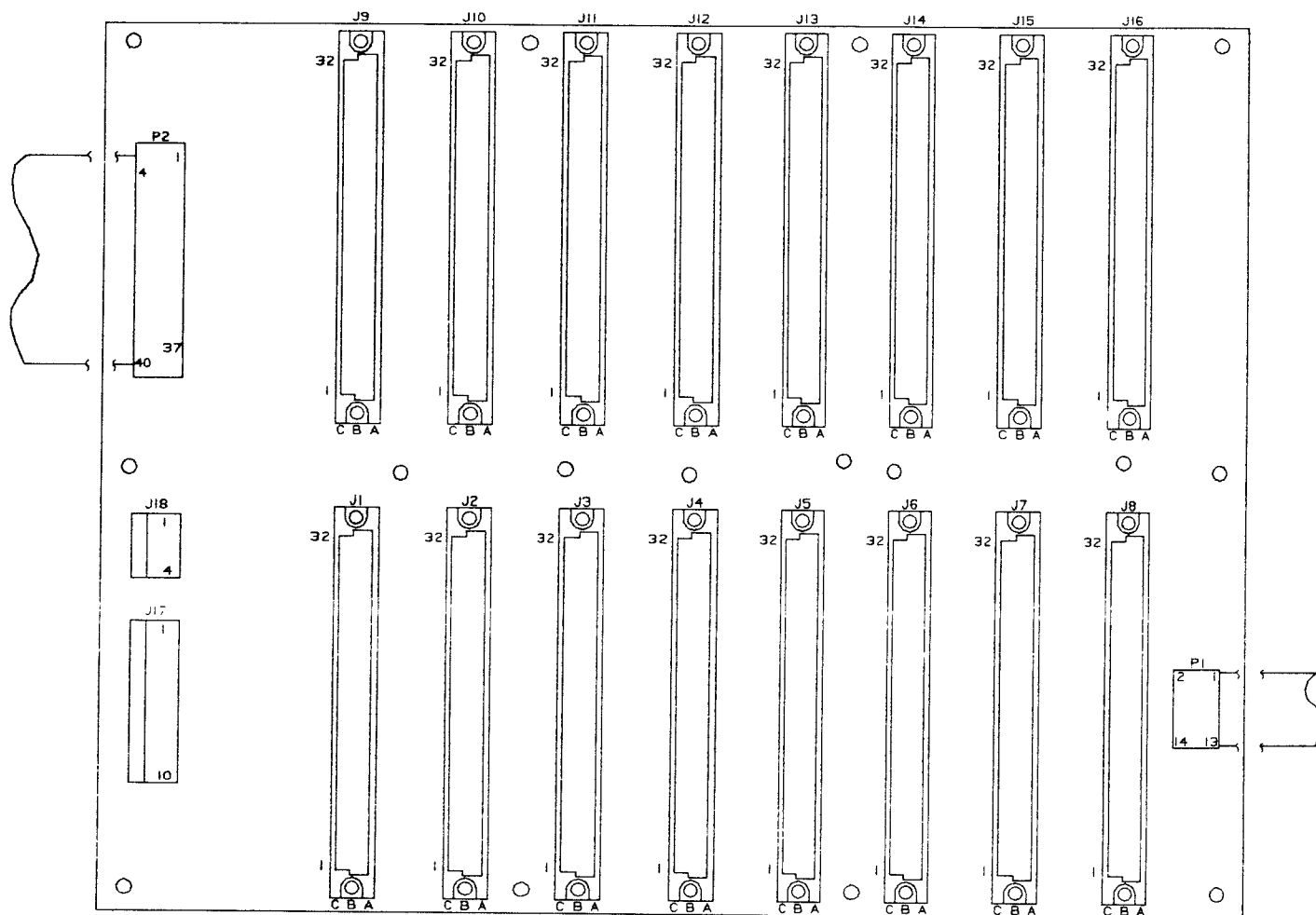


Figure 6-21. Interconnect PWB Assembly A10 Component Locations (10133-2900, Rev. C)

NOTE:  
UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

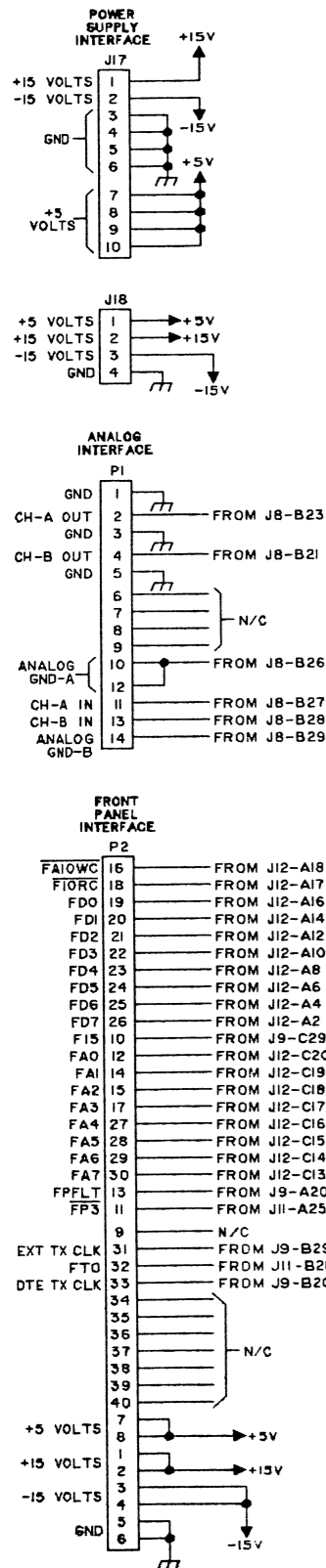


Figure 6-22. Interconnect PWB Assembly A10 Schematic Diagram (10133-2901, Rev. D) (Sheet 1 of 2)

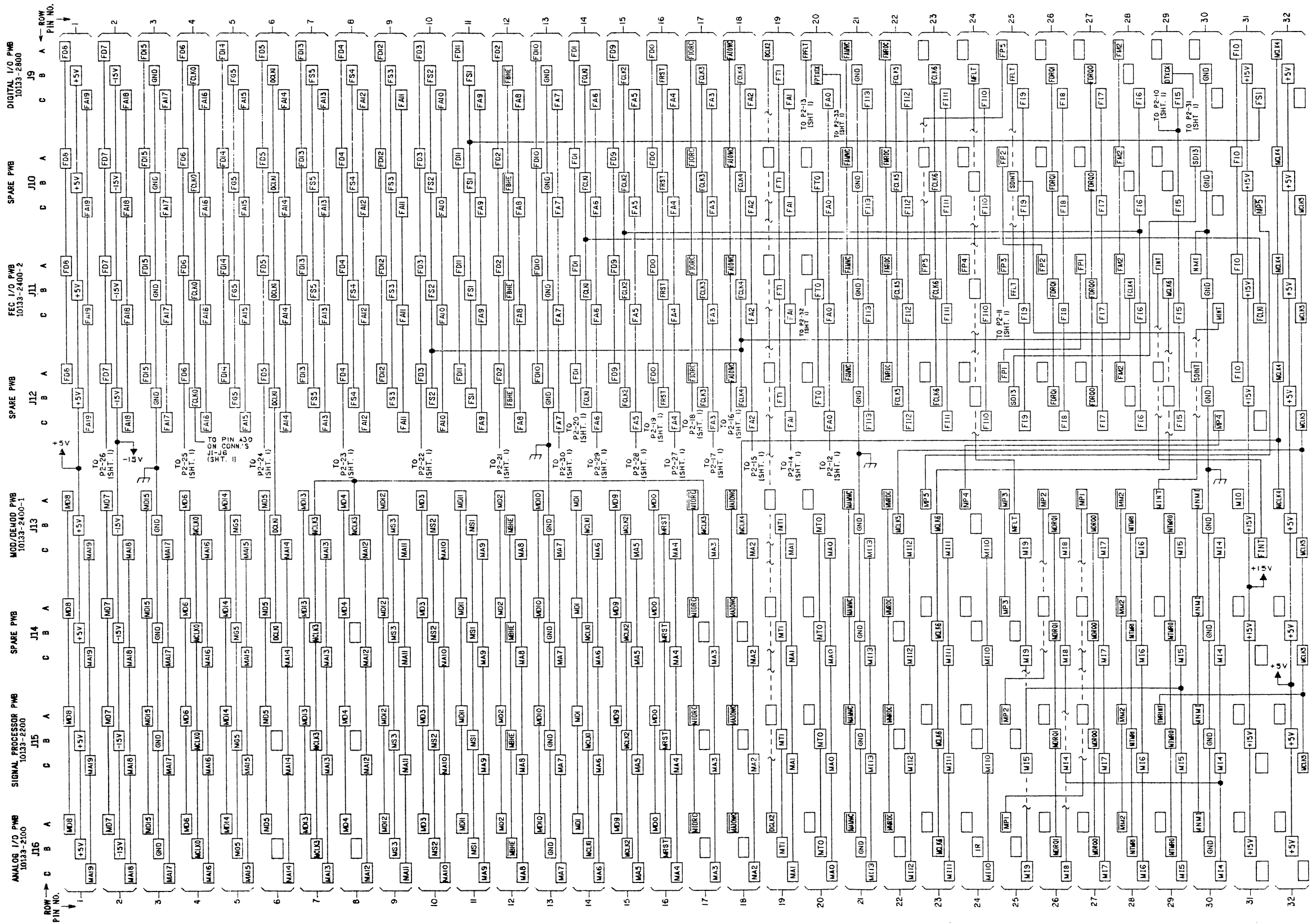


Figure 6-22. Interconnect PWB Assembly A10  
Schematic Diagram (10133-2901,  
Rev. D) (Sheet 2 of 2)

**Table 6-13. Front Panel Assembly A11 (10133-1800, Rev. B) Parts List**

Ref. Desig.	Part Number	Description
	10133-1805	FRONT PANEL
	10133-1016	FILTER FOAM
	Z03-0001-004	HANDLE(10350-A-1032-
	Z03-0004-002	FERRULE, ALUM, BLK
	MS91528-1P1B	KNOB
A1	10133-1850	LOGIC/CLK ASSY
A2	10133-1840	SWITCH ASSY
A3	10133-1804	DISPLAY ASSY
S1	S12-0004-012	SWITCH,PWR
W11	10133-4022	CABBLE ASSY
W12	10133-4023	CABLE ASSY (DISPLAY PWR)

**Table 6-14. Front Panel Logic/Clock PWB Assembly A11A1 (10133-1850, Rev. B) Parts List**

Ref. Desig.	Part Number	Description
C1	M39014/02-1298	CAP, .01UF
C2	C10-0003-012	CAP, .1UF
C3	C10-0003-012	CAP, .1UF
C4	C10-0003-012	CAP, .1UF
C5	C10-0003-012	CAP, .1UF
C6	C10-0003-012	CAP, .1UF
C7	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C10-0003-012	CAP, .1UF
C12	C26-0035-220	CAP, 22UF TANT 35V
C13	C26-0035-220	CAP, 22UF TANT 35V
C14	C26-0035-220	CAP, 22UF TANT 35V
C15	C10-0003-012	CAP, .1UF
C16	C26-0035-220	CAP, 22UF TANT 35V
C17	C26-0035-220	CAP, 22UF TANT 35V
C18	C26-0035-220	CAP, 22UF TANT 35V
C19	C25-0003-007	CAP, 1UF TANT 50V
C20	C26-0035-220	CAP, 22UF 20% 35V TANT
C21	C26-0035-220	CAP, 22UF 20% 35V TANT
C22	C10-0003-012	CAP, .1UF
C23	C10-0003-012	CAP, .1UF
C24	C10-0003-012	CAP, .1UF
C25	C10-0003-012	CAP, .1UF
C26	C10-0003-012	CAP, .1UF
C27	C10-0003-012	CAP, .1UF
C28	C10-0003-012	CAP, .1UF
C29	C10-0003-012	CAP, .1UF
C30	C10-0003-012	CAP, .1UF
C31	C10-0003-012	CAP, .1UF
C32	C10-0003-012	CAP, .1UF
C33	C10-0003-012	CAP, .1UF

Table 6-14. Front Panel Logic/Clock PWB Assembly A11A1 (10133-1850, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
C34	C10-0003-012	CAP, .1UF
C35	C10-0003-012	CAP, .1UF
C36	C10-0003-012	CAP, .1UF
C37	C10-0003-012	CAP, .1UF
C38	C25-0003-007	CAP, 1UF TANT
C39	C10-0003-012	CAP, .1UF
C40	C10-0003-012	CAP, .1UF
C41	C10-0003-012	CAP, .1UF
C42	CK05BX470K	CAP, 47PF
C43	C10-0003-012	CAP, .1UF
C44	C10-0003-012	CAP, .1UF
C45	CK05BX681K	CAP, 680PF
C46	C26-0035-220	CAP, 22UF TANT 35V
CR1	1N914	DIODE
CR2	1N4454	DIODE
CR3	1N4454	DIODE
J1	J46-0044-003	CONNECTOR, 3 POS
J3	J46-0054-026	CONNECTOR, 26 POS
J4	J46-0044-002	CONNECTOR, 2 POS
J5	J46-0054-034	CONNECTOR, 34 POS
J6	J42-0003-001	CONNECTOR, 4 POS
J7	J42-0003-001	CONNECTOR, 4 POS
J8	J-0031	CONNECTOR, COAX
J9	J-0031	CONNECTOR, COAX
J10	J46-0013-040	CONNECTOR, 40 POS
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-101	RES,100 OHM 5% 1/4W
R2	R65-0003-103	RES,10K 5% 1/4W
R3	R65-0003-104	RES,100K 5% 1/4W
R4	R65-0003-223	RES,22K 5% 1/4W
R5	R65-0003-103	RES,10K 5% 1/4W
R6	R65-0003-510	RES,51K 5% 1/4W
R7	R65-0003-510	RES,51K 5% 1/4W
R8	R65-0003-102	RES, 1K 5% 1/4W
R9	RN55D1212F	RES,12.1K 1% 1/8W
R10	RN55D1212F	RES,12.1K 1% 1/8W
R11	RN55D1212F	RES,12.1K 1% 1/8W
R12	RN55D1212F	RES,12.1K 1% 1/8W
R13	RN55D2002F	RES,20.0K 1% 1/8W
R14	RN55D2002F	RES,20.0K 1% 1/8W
R15	RCR20G271JM	RES,270K 5% 1/2W
R16	RN55D1628F	RES,162K 1% 1/8W
R17	RN55D5111F	RES,5.11K 1% 1/8W
R18	R30-0000-102	POT, 1K
R19	RN55D5111F	RES,5.11K 1% 1/8W
R20	RN55D1623F	RES,162K 1% 1/8W
R21	RN55D1623F	RES,162K 1% 1/8W
R22	RN55D1002F	RES,10K 1% 1/8W
R23	RN55D1002F	RES,10K 1% 1/8W
R24	RN55D1002F	RES,10K 1% 1/8W

Table 6-14. Front Panel Logic/Clock PWB Assembly A11A1 (10133-1850, Rev. B) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R25	R65-0003-473	RES,47K 5% 1/4W
R26	R65-0003-123	RES,12K 5% 1/4W
R27	RN55D6040F	RES,604 1% 1/8W
R28	R65-0003-123	RES,12K 5% 1/4W
TP1	J65-0009-002	TEST POINT
TP2	J65-0009-002	TEST POINT
TP3	J65-0009-002	TEST POINT
TP4	J65-0009-002	TEST POINT
U1	I27-0005-001	IC 8071 UP
U2	I35-0004-001	IC 555 TIMER
U4	I15-1000-373	IC 74HCT373
U5	I15-0000-000	IC 74HCT00
U6	10133-8063	IC PROGRAMMED A11A1U6
U7	I15-1000-259	IC 74HCT259
U8	I15-1000-259	IC 74HCT259
U9	I17-0011-001	IC RS232 DRIVER/RECEIVER
U10	I15-1000-157	IC 74HCT157
U11	I20-0012-001	IC LM361
U12	I15-1000-157	IC 74HCT157
U13	I70-0006-001	IC 145145 PLL
U14	I30-0010-001	IC LM336
U15	I15-1000-138	IC 74HCT138
U16	I15-1000-032	IC 74HCT32
U18	I15-1000-006	IC 74HCT86
U19	I15-1000-157	IC 74HCT157
U20	I15-1000-374	IC 74HCT374
U21	I15-1000-294	IC 74HCT294
U22	I30-0035-000	IC TL072
U23	I05-0000-628	IC 74LS628
VR1	IN4735	ZENER, 6.2V
XU1	J77-0008-007	SOCKET, 40 PIN
XU3	J77-0008-006	SOCKET, 28 PIN
XU6	J77-0008-006	SOCKET, 28 PIN
Y1	Y01-0009-001	XTAL, 11.0592 MHZ
Y2	10133-1750	VCXO, 9600 HZ

Table 6-15. Front Panel Switch Assembly (10133-1840, Rev. B) Parts List

Ref. Desig.	Part Number	Description
DS1	N21-0017-105	LED, GREEN
DS2	N21-0017-105	LED, GREEN
DS3	N21-0017-105	LED, GREEN
DS4	N21-0017-105	LED, GREEN
DS5	N21-0017-102	LED, RED
DS6	N21-0017-105	LED, GREEN
DS7	N21-0017-105	LED, GREEN
DS8	N21-0017-105	LED, GREEN
DS14	N21-0017-105	LED, GREEN
J2	J46-0044-004	CONNECTOR, 4 POS
R1	R50-0010-820	RES, SIP, 20 POS, 820 OHMS
R2	R50-0010-820	RES, SIP, 20 POS, 820 OHMS
S1	10122-2076	SWITCH DPST
S2	S05-0004-001	SWITCH DPST
S3	S05-0004-001	SWITCH DPST
S4	S05-0004-001	SWITCH DPST
S5	S05-0004-001	SWITCH DPST
S6	S05-0004-001	SWITCH DPST
S7	S05-0004-001	SWITCH DPST
S8	10122-2076	SWITCH DPST
S10	S05-0004-002	SWITCH SPST
S12	10122-2076	SWITCH DPST
S13	10122-2076	SWITCH DPST
S14	10122-2076	SWITCH DPST
S15	10122-2076	SWITCH DPST
S16	10122-2076	SWITCH DPST
S17	10122-2076	SWITCH DPST
S18	10122-2076	SWITCH DPST
S19	10122-2076	SWITCH DPST
S20	10122-2076	SWITCH DPST
S21	10122-2076	SWITCH DPST
S22	10122-2076	SWITCH DPST
S23	10122-2076	SWITCH DPST
S24	10122-2076	SWITCH DPST
S25	10122-2076	SWITCH DPST
S26	10122-2076	SWITCH DPST
S27	10122-2076	SWITCH DPST
W1	10133-4021	CABLE ASSY W10
Z1	10133-1824	FIXTURE, SWITCH

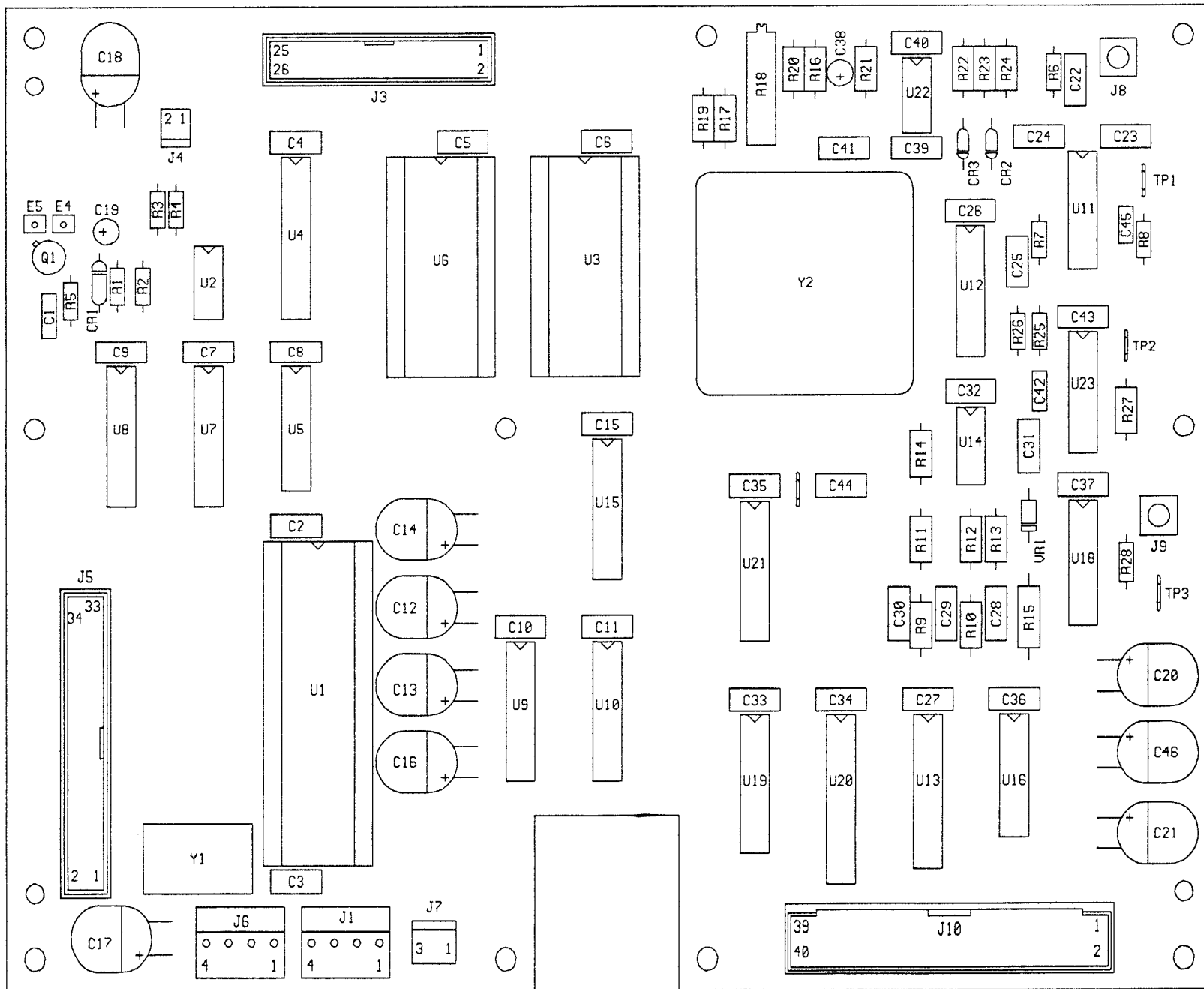


Figure 6-23. Logic/Clock PWB Assembly A11A1 Component Locations (10133-1850, Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, +/-5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

D[0:7]

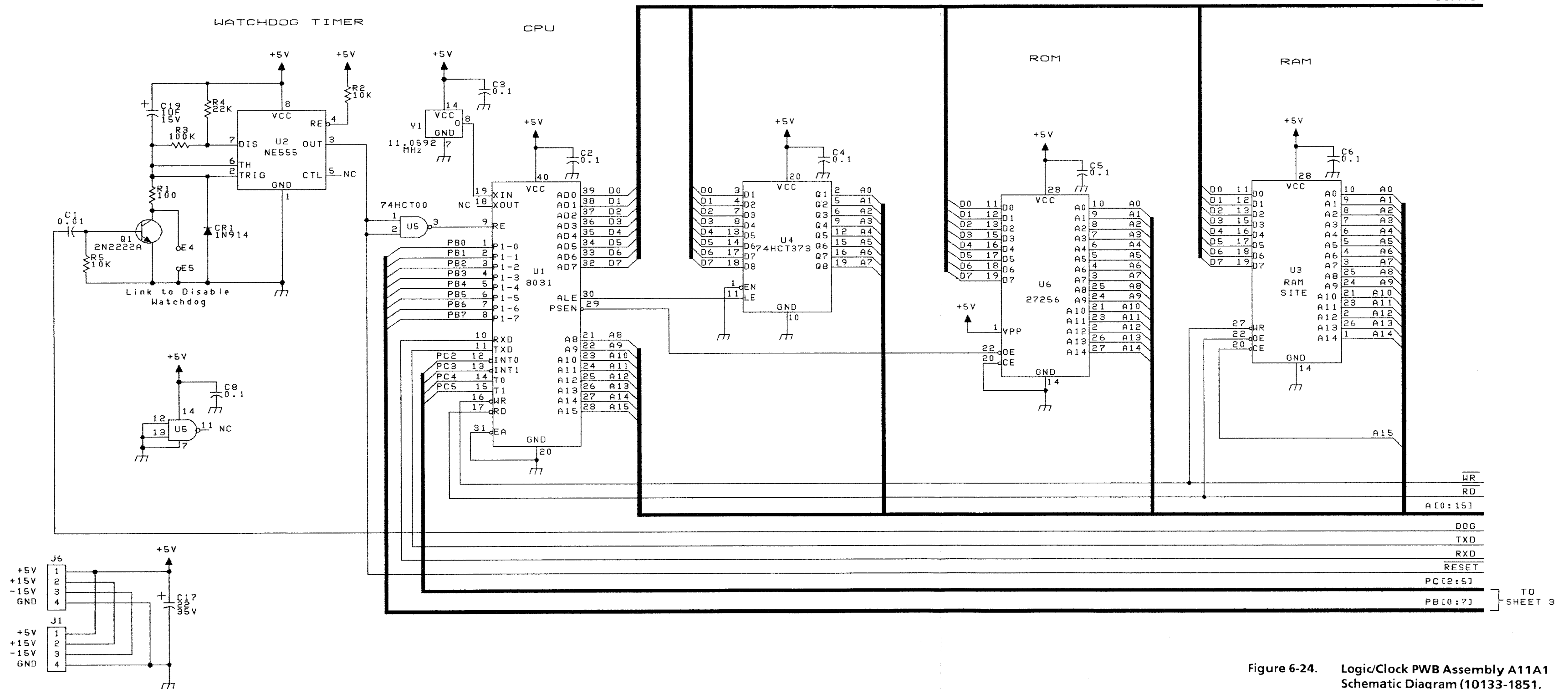


Figure 6-24. Logic/Clock PWB Assembly A11A1 Schematic Diagram (10133-1851, Rev. B) (Sheet 1 of 4)

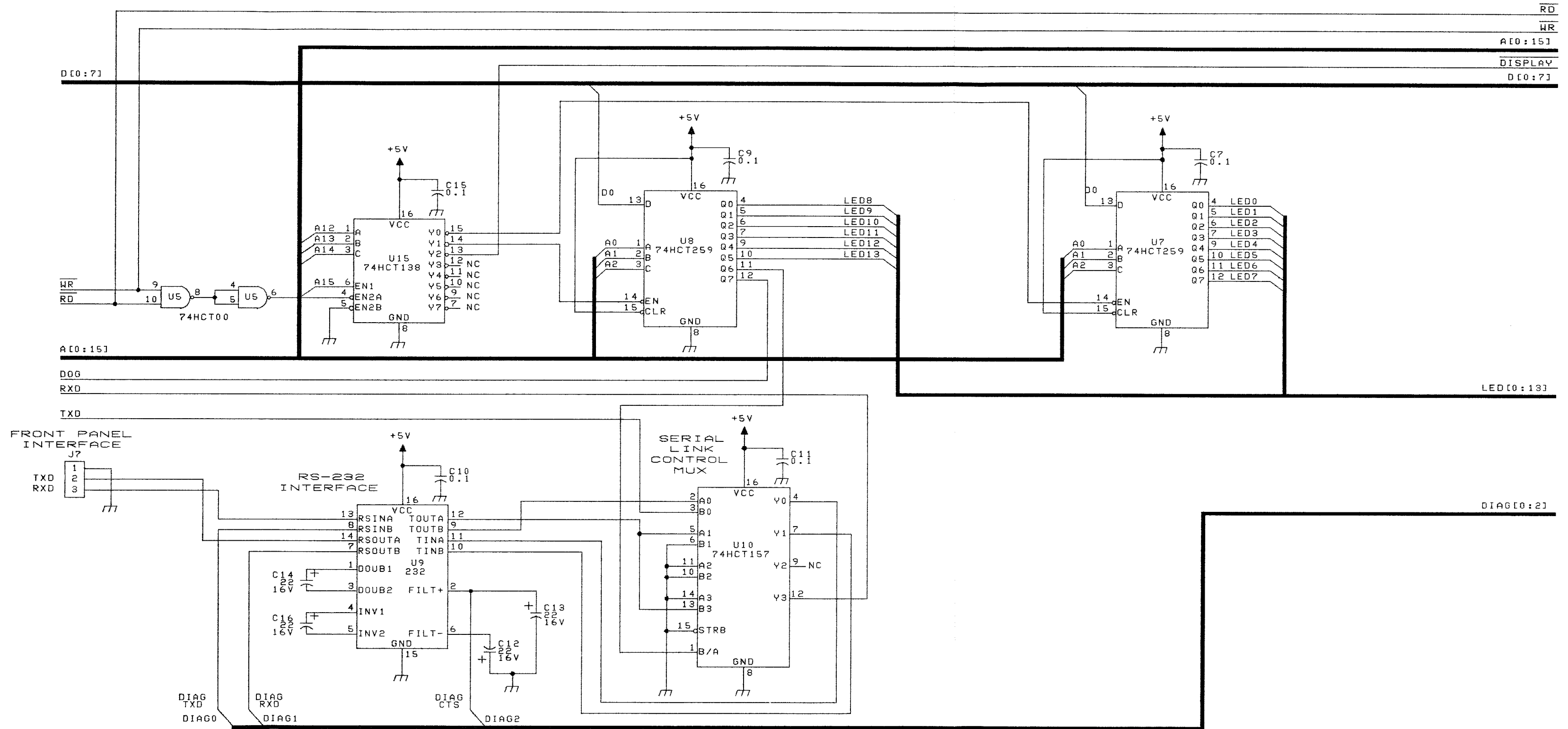


Figure 6-24. Logic/Clock PWB Assembly A11A1 Schematic Diagram (10133-1851, Rev. B) (Sheet 2 of 4)

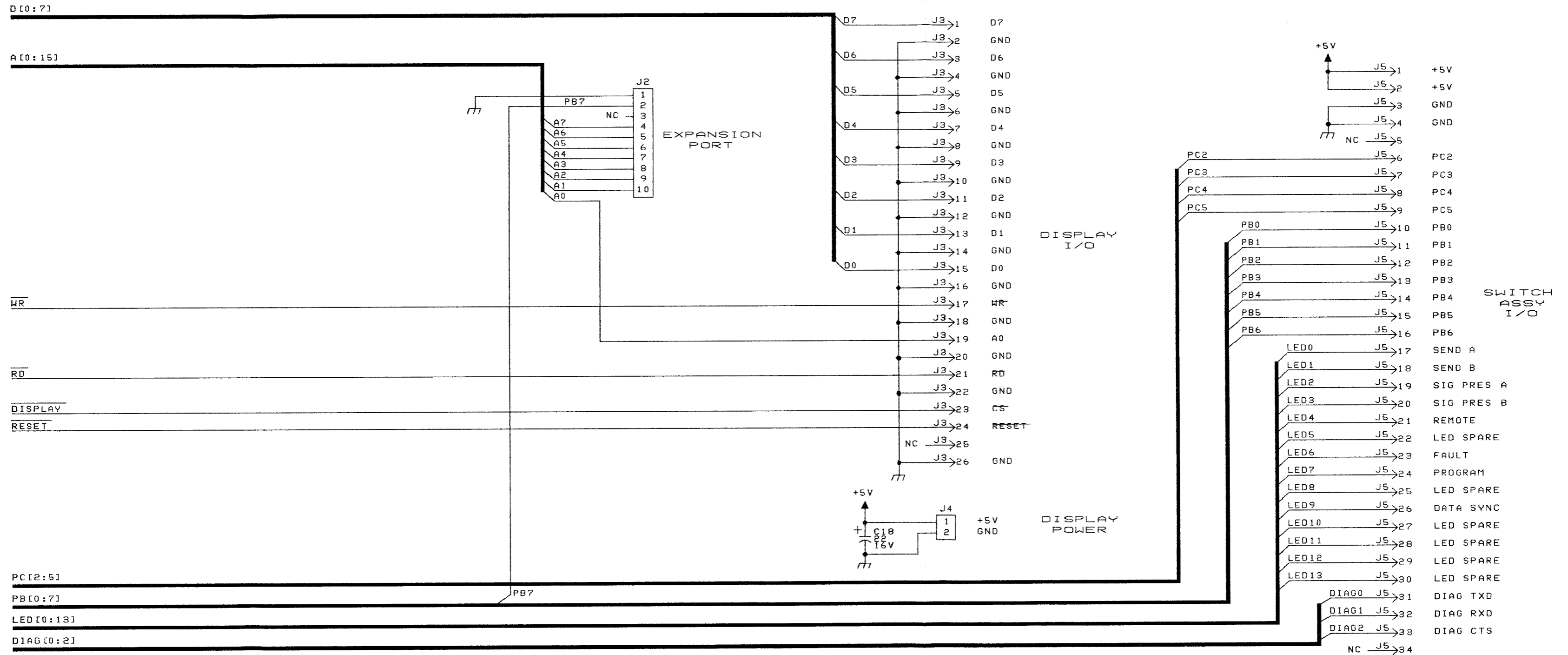


Figure 6-24. Logic/Clock PWB Assembly A11A1 Schematic Diagram (10133-1851, Rev. B) (Sheet 3 of 4)

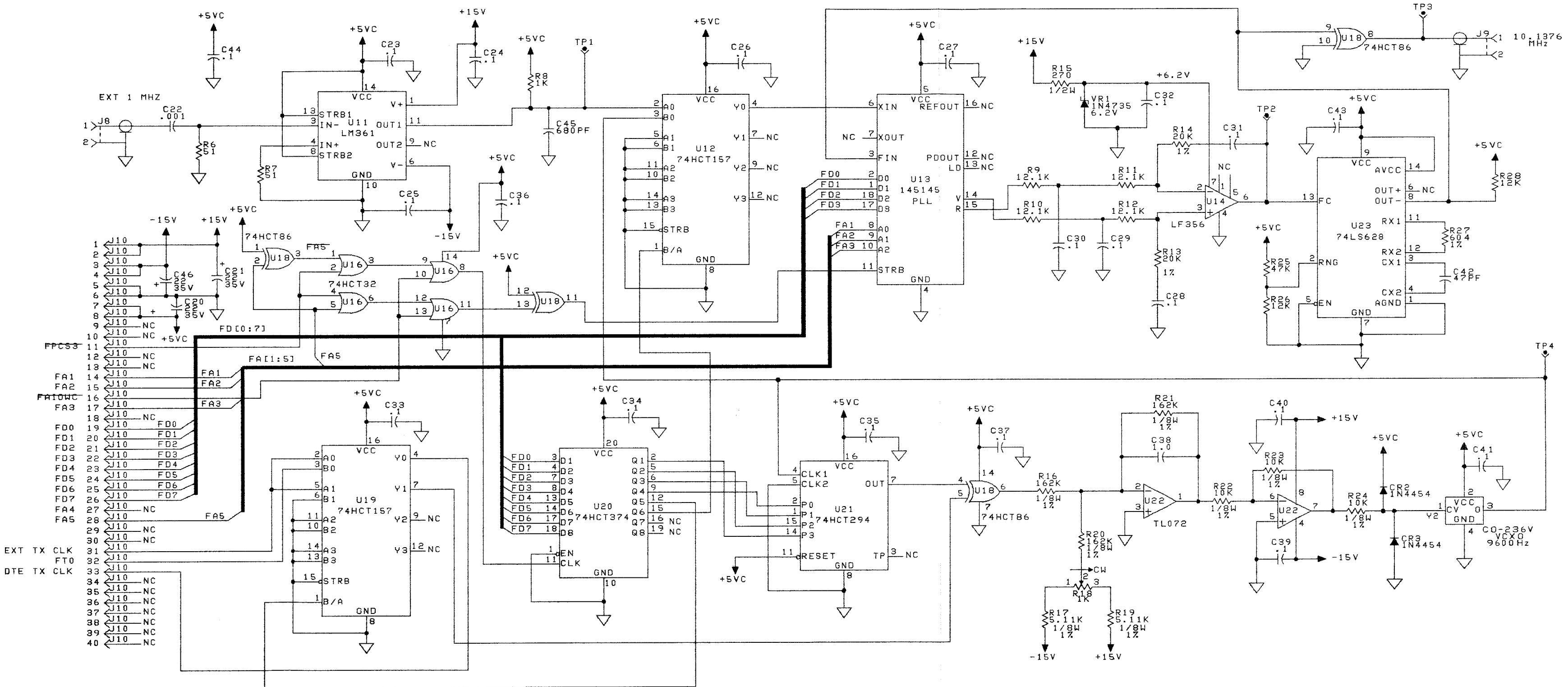


Figure 6-24. Logic/Clock PWB Assembly A11A1 Schematic Diagram (10133-1851, Rev. B) (Sheet 4 of 4)

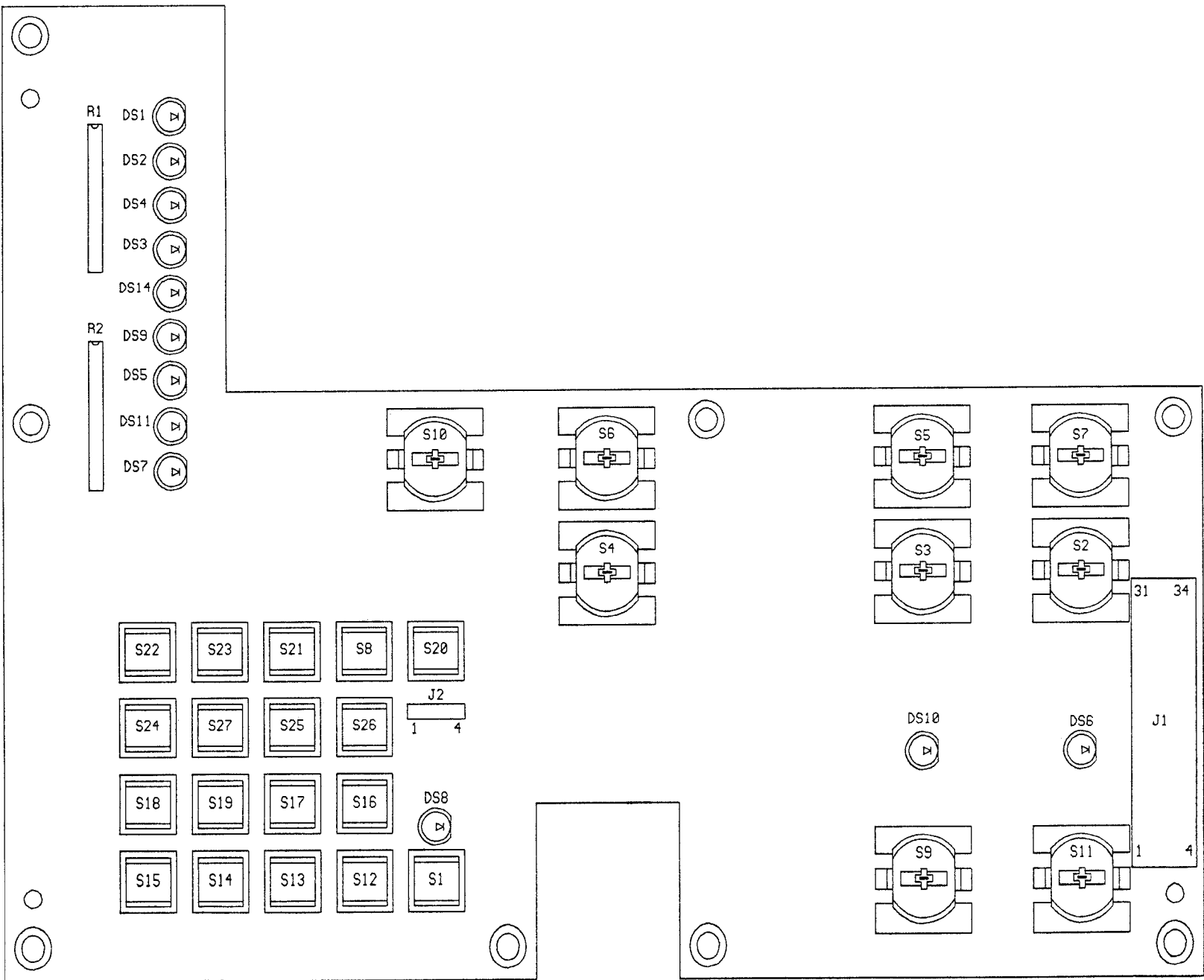


Figure 6-25. Front Panel Switch PWB Assembly, A11A2 (10133-1840, Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, +/-5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

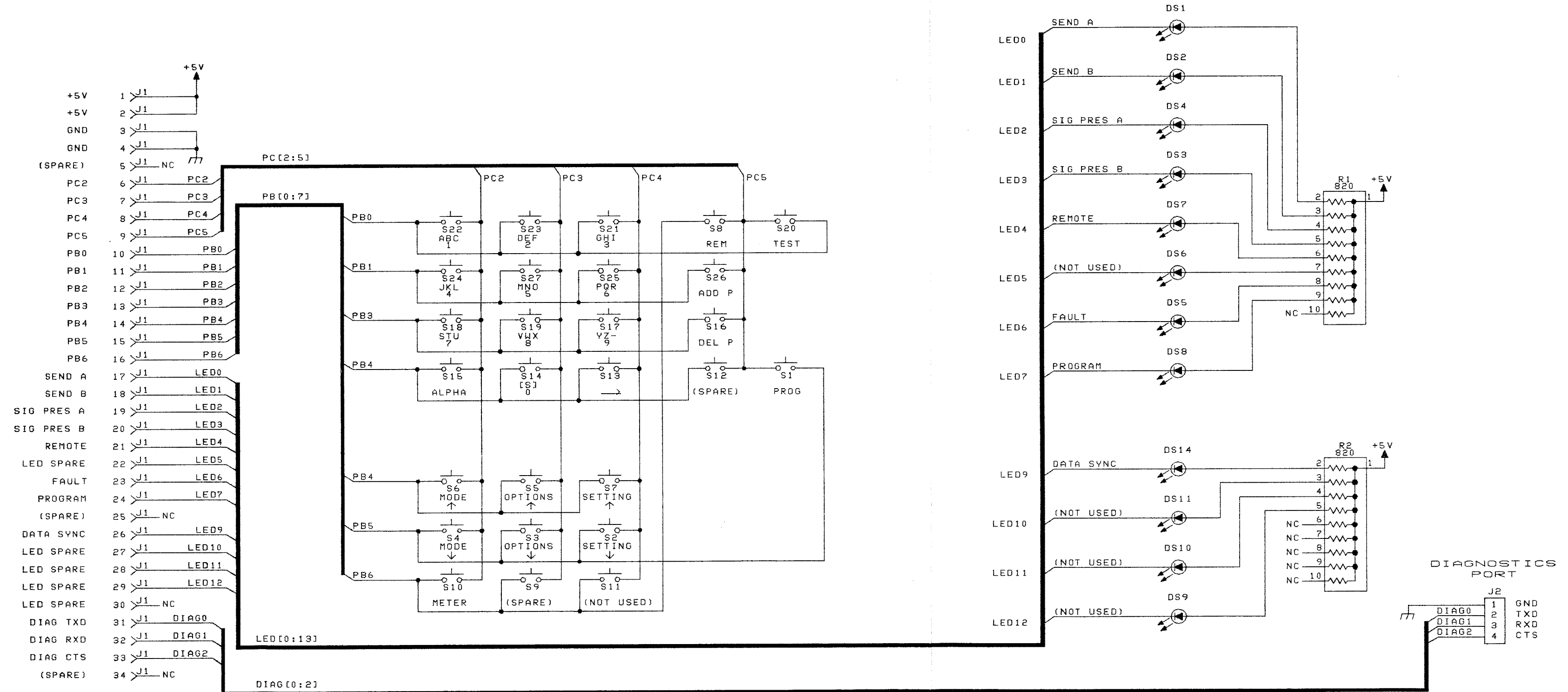


Figure 6-26. Front Panel Switch PWB Assembly, A11A2 Schematic Diagram (10133-1841, Rev. B)

**Table 6-16. Rear Panel Assembly A12 (10133-1009, Rev. F) Parts List**

Ref. Desig.	Part Number	Description
A1	10133-1150	FILTER ASSY
A2	10133-1090	PWB ASSY,FAN SPEED
F1	F-0013	FUSE 3.0A QA 250V 3AG
F2	F-0022	FUSE 10A QA 32V 3AG
FL2	G01-0005-000	FILTER, AC LINE
J5	MS3102A-16-9P	BOX RECEPTACLE
P1	J20-0015-004	CONN., 4 PIN,FEMALE
P2	J20-0014-004	PLUG-4-PIN
XF1	F01-0002-102	FUSE HOLDER

**Table 6-17. Rear Panel Assembly A12A1 (10133-1150, Rev. B) Parts List**

Ref. Desig.	Part Number	Description
A1	10133-1080	PWB ASSY,FILTER BD #1
A2	10133-1070	PWB ASSY,FILTER BD #2
A3	10133-1160	PWB ASSY,FILTER BD #3

Table 6-18. Rear Panel Filter PWB Assembly No. 1 A12A1A1 (10133-1080, Rev. N) Parts List

Ref. Desig.	Part Number	Description
	J46-0047-003	HEADER, 3 POS
C1	C25-0003-107	CAP 1.0UF 10% 35V TANT
C2	C25-0003-107	CAP 1.0UF 10% 35V TANT
C3	C10-0003-012	CAP, .1UF
C4	C10-0003-012	CAP, .1UF
C5	C10-0003-012	CAP, .1UF
C6	C10-0003-012	CAP, .1UF
C8	C10-0003-012	CAP, .1UF
C9	C10-0003-012	CAP, .1UF
C10	C10-0003-012	CAP, .1UF
C11	C26-0035-220	CAP 22UF 20% 35V TANT
C12	C26-0035-220	CAP 22UF 20% 35V TANT
C13	C26-0035-220	CAP 22UF 20% 35V TANT
C14	C25-0001-301	CAP 1.0UF 20% 20V TANT
C15	C25-0001-301	CAP 1.0UF 20% 20V TANT
C16	C10-0003-012	CAP, .1UF
C17	C10-0003-012	CAP, .1UF
CR1	1N4148	DIODE,SILICON
CR2	1N4148	DIODE,SILICON
CR3	1N4148	DIODE,SILICON
CR4	1N4148	DIODE,SILICON
CR5	1N4148	DIODE,SILICON
CR6	1N4148	DIODE,SILICON
D1	D50-0006-002	TRANZORB,SA-8.0
D2	D50-0006-002	TRANZORB,SA-8.0
D3	D50-0006-002	TRANZORB,SA-8.0
D4	D50-0006-002	TRANZORB,SA-8.0
H1	Z60-0020-001	HEATSINK,TO-5
H2	Z60-0020-001	HEATSINK,TO-5
J1	J46-0013-026	HEADER ASSY, 26 PIN
J2	J42-0003-001	CONNECTOR, LOCKING, 4 PIN
J3	J46-0013-014	CONNECTOR,14 PIN
P1	J46-0029-048	CONNECTOR, 48 PIN
P2	J46-0029-048	CONNECTOR, 48 PIN
Q1	2N2907	XSTR SS/GP PNP TO-18
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	2N6515	XSTR
Q4	2N6515	XSTR
R1	RCR07G332JM	RES,3.3K 5% 1/4W CAR COMP
R2	RCR07G332JM	RES,3.3K 5% 1/4W CAR COMP
R3	RCR07G301JM	RES,300 5% 1/4W CAR COMP
R4	RCR07G301JM	RES,300 5% 1/4W CAR COMP
R5	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R6	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R7	RN55D2210F	RES,221.0 1% 1/8W MET FLM
R8	RN55D1101F	1100 OHM RESISTOR

Table 6-18. Rear Panel Filter PWB Assembly No. 1 A12A1A1 (10133-1080, Rev. N) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R9	RN55D6040F	RES,604.0 1% 1/8W MET FLM
R10	RN55D1210F	RES,121.0 1% 1/8W MET FLM
R11	RCR07G102JM	RES,1.0K 5% 1/4W CAR COMP
R12	RCR07G102JM	RES,1.0K 5% 1/4W CAR COMP
R13	R50-0006-123	RES,SIP,12K, 6PIN
R14	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R15	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R16	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
S1	S30-0002-405	SW,4PDT,.3A, ,MNTAB,PCTRM
S2	S10-0026-001	SW,SP,ON-NONE-OFF,TOG,PCM
T1	T30-0001-005	TRANSFORMER,AUDIO,600 OH
T2	T30-0001-005	TRANSFORMER,AUDIO,600 OH
T3	T30-0001-005	TRANSFORMER,AUDIO,600 OH
T4	T30-0001-005	TRANSFORMER,AUDIO,600 OH
TP1	J65-0009-002	TEST POINT
TP2	J65-0009-002	TEST POINT
TP3	J65-0009-002	TEST POINT
TP4	J65-0009-002	TEST POINT
TP5	J65-0009-002	TEST POINT
TP6	J65-0009-002	TEST POINT
U1	I11-0015-006	IC,REG ADJ,TO-39,LM317
U2	I11-0012-002	VOLT,REGULATOR,NEG.
U3	I16-0008-002	IC, RS-422 DRIVER
U4	I17-0003-000	IC 26LS33 PLASTIC TTL
U5	I15-0000-086	IC 74HC86 PLASTIC CMOS
U6	I15-0000-086	IC 74HC86 PLASTIC CMOS
U7	I17-0007-001	TRIPLE RS232 DRIVER-RCVR
U8	I16-0001-000	IC 1488 CERAMIC DTL
U9	I16-0001-000	IC 1488 CERAMIC DTL
U10	I17-0001-000	IC 1489 CERAMIC DTL

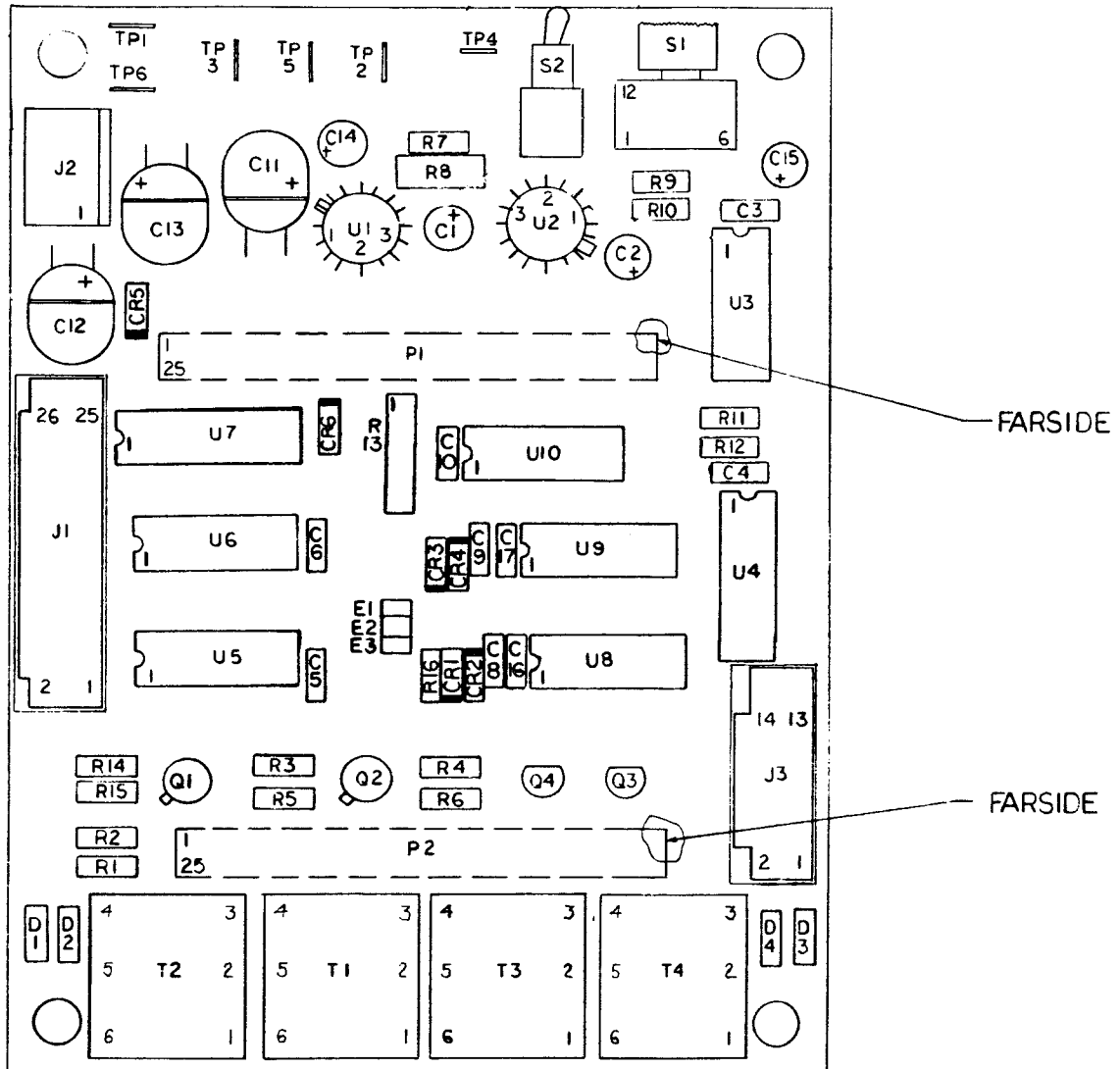


Figure 6-27. Rear Panel Filter PWB Assembly No. 1, A12A1A1, Component Locations (10133-1080, Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. E2 IS NORMALLY JUMPED TO E3. WHEN THE RF-3466 IS CONFIGURED FOR THE MIL POS INTERFACE, THE DATA CLOCKS CAN BE INVERTED BY JUMPING E1 TO E2. THIS MAY BE REQUIRED WITH SOME DATA TERMINAL EQUIPMENT.

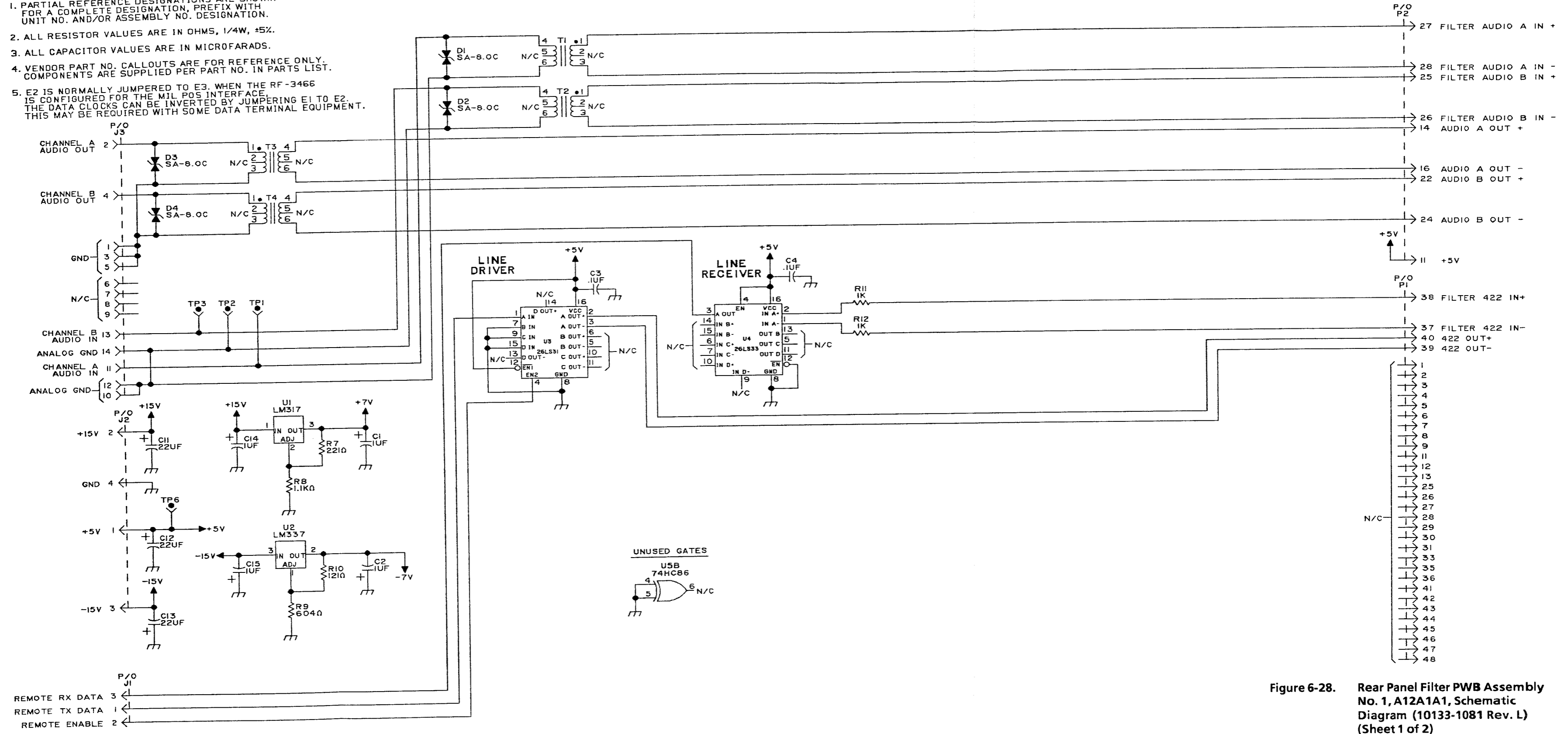
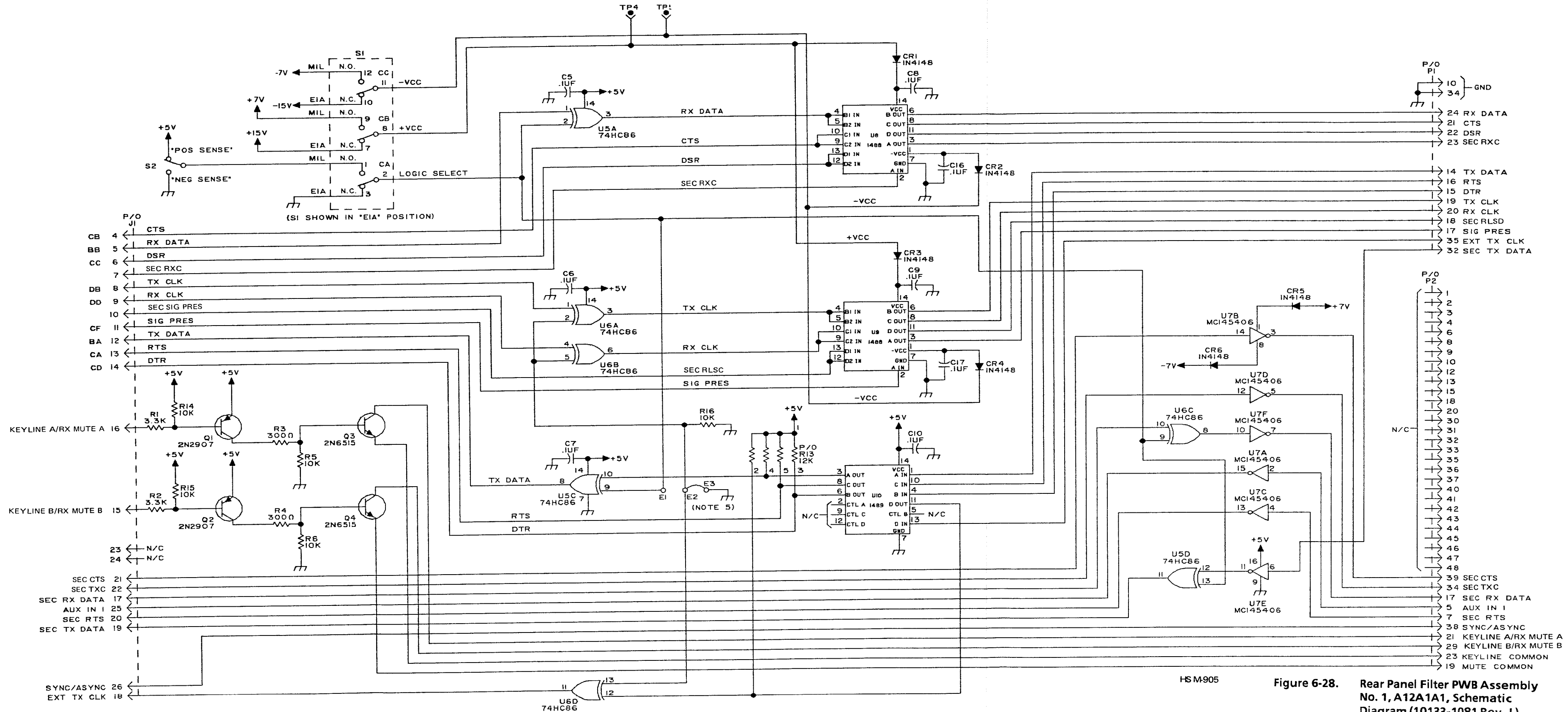


Figure 6-28. Rear Panel Filter PWB Assembly No. 1, A12A1A1, Schematic Diagram (10133-1081 Rev. L) (Sheet 1 of 2)



HSM-905  
Figure 6-28. Rear Panel Filter PWB Assembly No. 1, A12A1A1, Schematic Diagram (10133-1081 Rev. L) (Sheet 2 of 2)

Table 6-19. Rear Panel Filter PWB Assembly No. 2 A12A1A2 (10133-1070, Rev. G) Parts List

Ref. Desig.	Part Number	Description
C1	CKO6BX472K	CAP 4700PF 10% 200V CER
C2	CKO6BX472K	CAP 4700PF 10% 200V CER
C3	CKO6BX472K	CAP 4700PF 10% 200V CER
C4	CKO6BX472K	CAP 4700PF 10% 200V CER
C5	CKO6BX472K	CAP 4700PF 10% 200V CER
C6	CKO6BX472K	CAP 4700PF 10% 200V CER
C7	CKO6BX472K	CAP 4700PF 10% 200V CER
C8	CKO6BX472K	CAP 4700PF 10% 200V CER
C9	CKO6BX472K	CAP 4700PF 10% 200V CER
C10	CKO6BX472K	CAP 4700PF 10% 200V CER
C11	CKO6BX472K	CAP 4700PF 10% 200V CER
C12	CKO6BX472K	CAP 4700PF 10% 200V CER
C13	CKO6BX472K	CAP 4700PF 10% 200V CER
C14	CKO6BX472K	CAP 4700PF 10% 200V CER
C15	CKO6BX472K	CAP 4700PF 10% 200V CER
C16	CKO6BX472K	CAP 4700PF 10% 200V CER
C17	CKO5BX102K	CAP 1000PF 10% 200V CER
C18	CKO5BX102K	CAP 1000PF 10% 200V CER
C19	CKO5BX102K	CAP 1000PF 10% 200V CER
C20	CKO5BX102K	CAP 1000PF 10% 200V CER
C21	CKO5BX102K	CAP 1000PF 10% 200V CER
C22	CKO5BX102K	CAP 1000PF 10% 200V CER
C23	CKO5BX102K	CAP 1000PF 10% 200V CER
C24	CKO5BX102K	CAP 1000PF 10% 200V CER
C25	CKO5BX102K	CAP 1000PF 10% 200V CER
C26	CKO5BX102K	CAP 1000PF 10% 200V CER
C27	CKO5BX102K	CAP 1000PF 10% 200V CER
C28	CKO6BX472K	CAP 4700PF 10% 200V CER
C29	CKO6BX472K	CAP 4700PF 10% 200V CER
C30	CKO6BX472K	CAP 4700PF 10% 200V CER
C31	CKO6BX472K	CAP 4700PF 10% 200V CER
C32	CKO5BX102K	CAP 1000PF 10% 200V CER
C33	CKO5BX102K	CAP 1000PF 10% 200V CER
C34	CKO5BX102K	CAP 1000PF 10% 200V CER
C35	CKO5BX102K	CAP 1000PF 10% 200V CER
C36	CKO5BX102K	CAP 1000PF 10% 200V CER
C37	CKO5BX102K	CAP 1000PF 10% 200V CER
C38	CKO5BX102K	CAP 1000PF 10% 200V CER
C39	CKO5BX102K	CAP 1000PF 10% 200V CER
L1	MS90539-7	COIL, RF 470 UH 5%
L2	MS90539-7	COIL, RF 470 UH 5%
L3	MS90539-7	COIL, RF 470 UH 5%
L4	MS90539-7	COIL, RF 470 UH 5%
L9	MS90539-7	COIL, RF 470 UH 5%
L10	MS90539-7	COIL, RF 470 UH 5%
L11	MS90539-7	COIL, RF 470 UH 5%

Table 6-19. Rear Panel Filter PWB Assembly No. 2 A12A1A2 (10133-1070, Rev. G) Parts List (Cont.)

Ref. Desig.	Part Number	Description
L12	MS90539-7	COIL, RF 470 UH 5%
P1	J46-0043-048	CONNECTOR, 48 PIN
P2	J46-0043-048	CONNECTOR, 48 PIN
R1	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R2	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R3	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R4	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R5	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R6	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R7	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R8	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R9	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R10	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R11	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R12	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R13	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R14	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R15	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R16	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R17	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R18	RCR07G330JM	RES,33 5% 1/4W CAR COMP
R19	RCR07G330JM	RES,33 5% 1/4W CAR COMP
TP7	J65-0009-002	TEST POINT

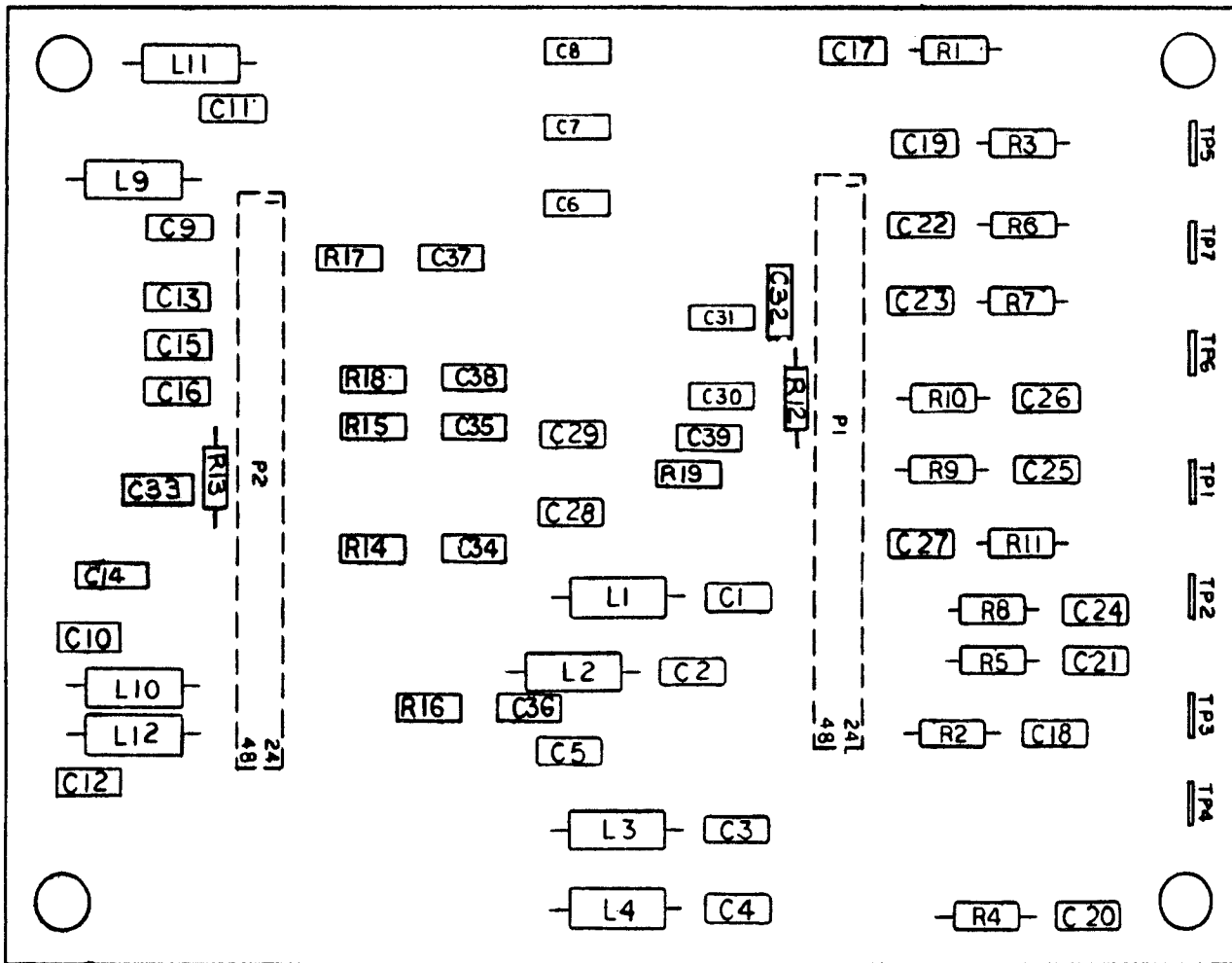




Figure 6-29. Rear Panel Filter PWB Assembly No. 2, A12A1A2, Component Locations (10133-1070, Rev. H)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN PICOFARADS (PF).
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES (UH).
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
6.  IS A SIGNAL GROUND AND IS NOT CONNECTED TO PWB GROUND PLANE.
7.  IS A CHASSIS GROUND AND IS CONNECTED TO ASSY CHASSIS AND PWB GROUND PLANE ONLY.

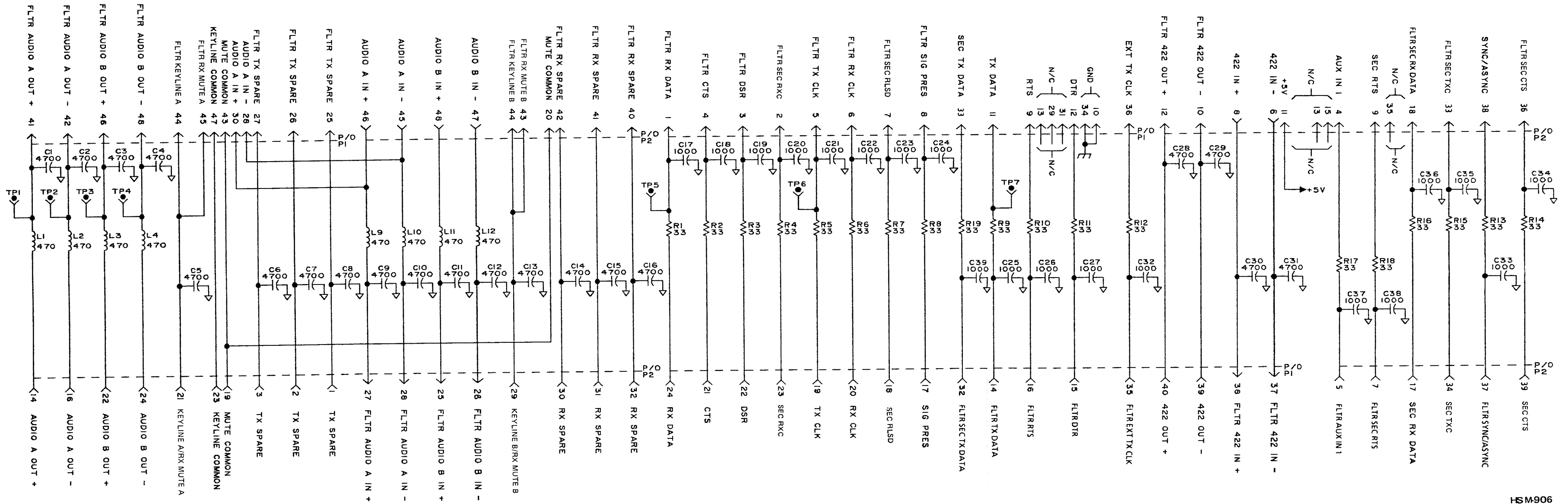


Figure 6-30. Rear Panel Filter PWB Assembly No. 2, A12A1A2, Schematic Diagram (10133-1071, Rev. H)

HSM906

Table 6-20. Rear Panel Filter PWB Assembly No. 3 A12A1A3 (10133-1160, Rev. B) Parts List

Ref. Desig.	Part Number	Description
J1	J22-0035-001	CONNECTOR, 25 PIN
J3	J22-0053-001	15PIN, DB CONN, FEMALE
J4	J22-0053-002	15 PIN, DB, CONN., MALE
J5	J22-0034-001	CONN, 9 POS, FEMALE
P1	J46-0040-048	CONN, 48 PIN
P2	J46-0040-048	CONN, 48 PIN
TP1	J65-0009-002	TEST POINT
TP2	J65-0009-002	TEST POINT
TP3	J65-0009-002	TEST POINT
TP4	J65-0009-002	TEST POINT
TP5	J65-0009-002	TEST POINT
TP6	J65-0009-002	TEST POINT
TP7	J65-0009-002	TEST POINT

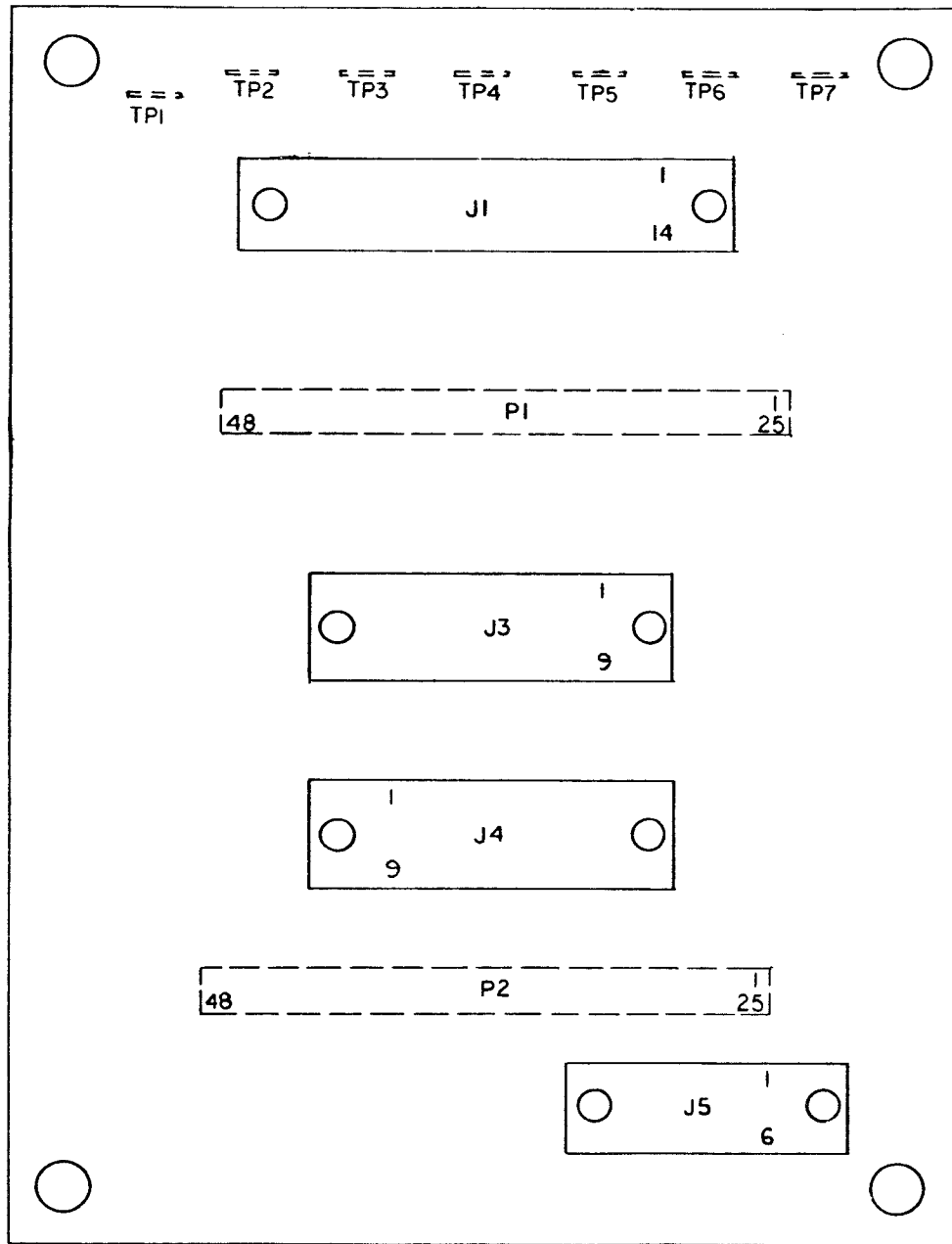




Figure 6-31. Rear Panel Filter PWB Assembly No. 3, A12A1A3, Component Locations (10133-1160, Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
3.  IS A SIGNAL GROUND AND IS NOT CONNECTED TO PWB GND PLANE.
4.  IS A CHASSIS GROUND AND IS CONNECTED TO ASSY CHASSIS AND PWB GROUND PLANE ONLY.

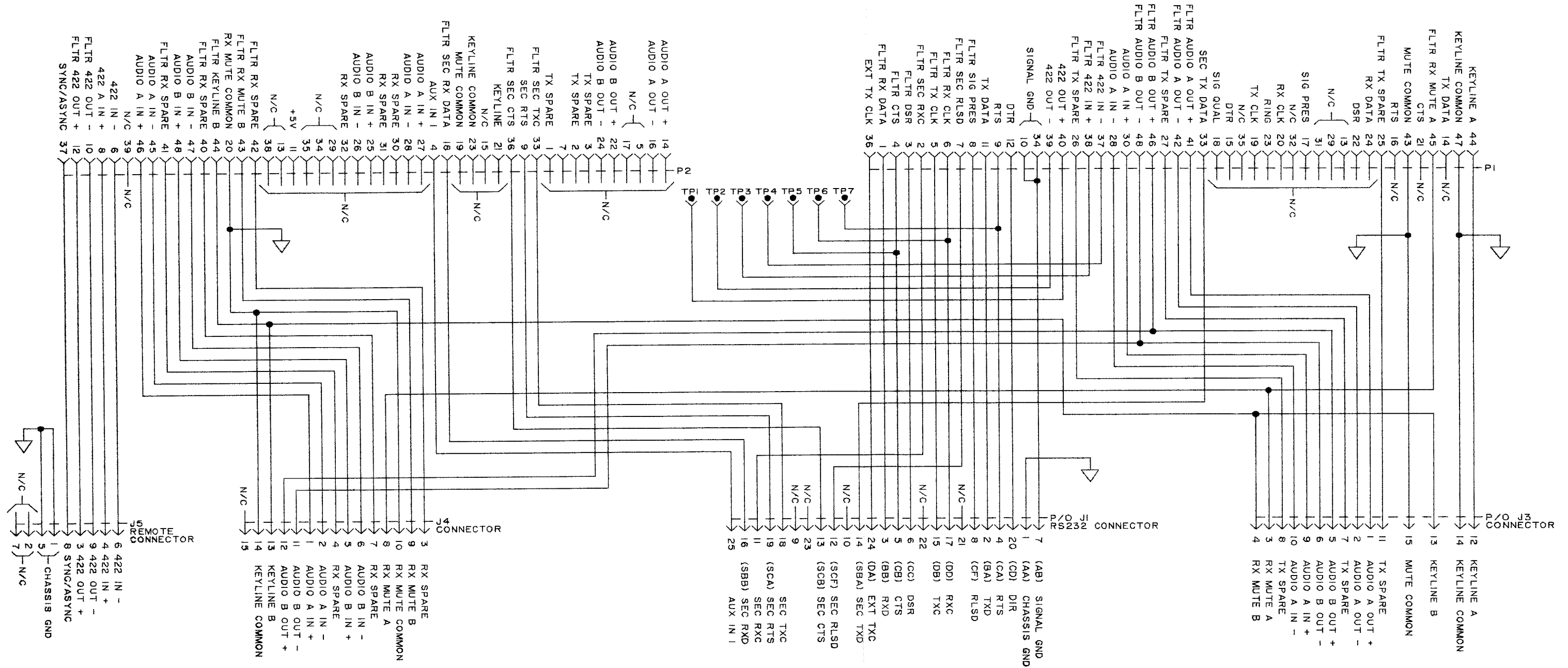


Figure 6-32. Rear Panel Filter PWB Assembly No. 3, A12A1A3, Schematic Diagram (10133-1161, Rev. B)

Table 6-21. Fan Speed Control PWB Assembly A12A2 (10133-1090, Rev.E) Parts List

Ref. Desig.	Part Number	Description
C1	C73-0025-680	CAP,FXD,ELCTLT,68 UF,25 V
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	C26-0025-220	CAP 22UF 20% 25V TANT
C4	C26-0025-220	CAP 22UF 20% 25V TANT
C5	C28-0025-222	CAP, 2200UF, 25V
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
CR1	1N4454	DIODE, SS SILICON
CR2	1N4454	DIODE, SS SILICON
CR3	1N4454	DIODE, SS SILICON
J1	J46-0044-003	FRICITION LOCK WAFER,3 PIN
J2	J46-0044-002	CONNECTOR, 2-PIN
Q1	2N4920	TRANS., PNP
R1	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R2	RN55D1372F	RES,13.7K 1% 1/8W MET FLM
R3	R-2224	RES,VAR,PCB 500 .5 20%
R4	RN55D3481F	RES,3480 1% 1/8W MET FLM
R5	RCR07G104JM	RES,100K 5% 1/4W CAR COMP
R6	RCR07G153JM	RES,15K 5% 1/4W CAR COMP
R8	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R9	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R10	RCR07G103JM	RES,10K 5% 1/4W CAR COMP
R11	RCR07G222JM	RES,2.2K 5% 1/4W CAR COMP
R12	RCR07G331JM	RES,330 5% 1/4W CAR COMP
TP1	J60-0001-002	TEST POINT, RED
U1	I23-0001-002	TEMPERATURE SENSOR
U2	I30-0020-004	IC 258 OP AMP TO-5

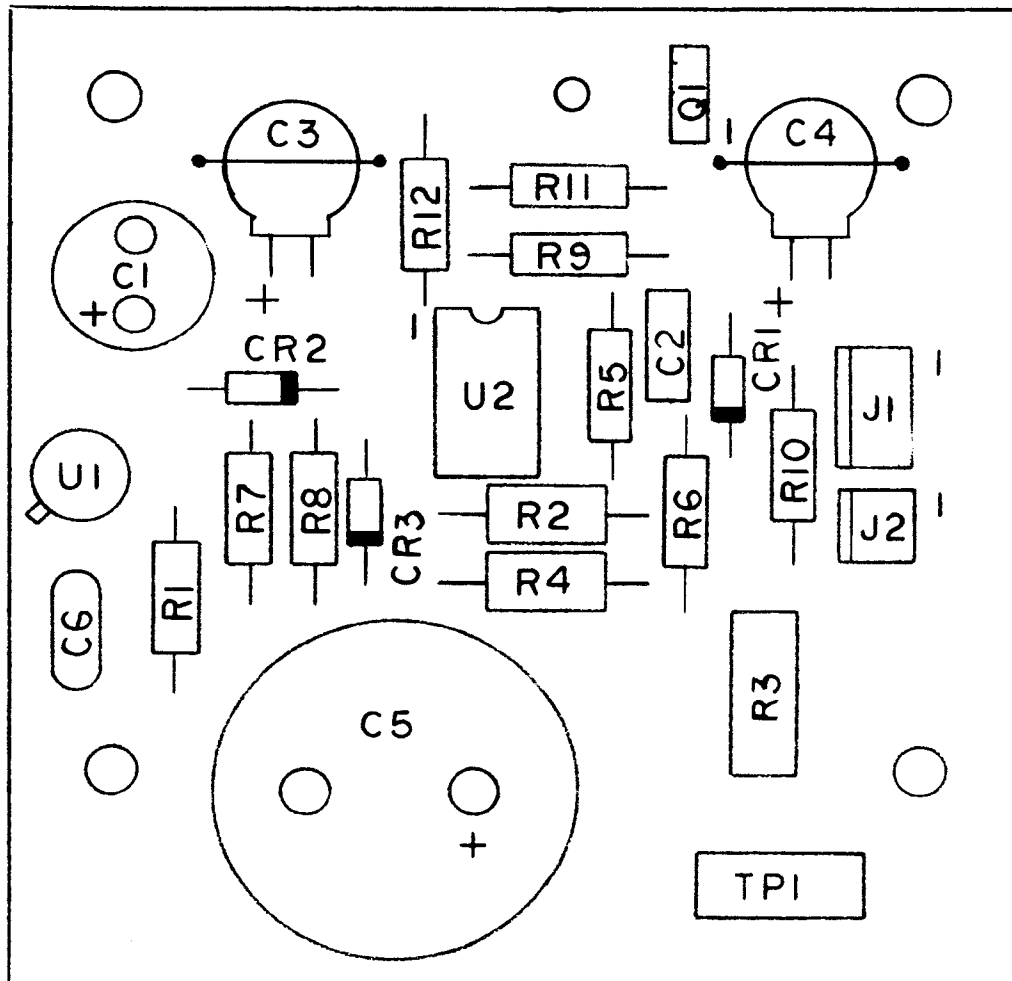
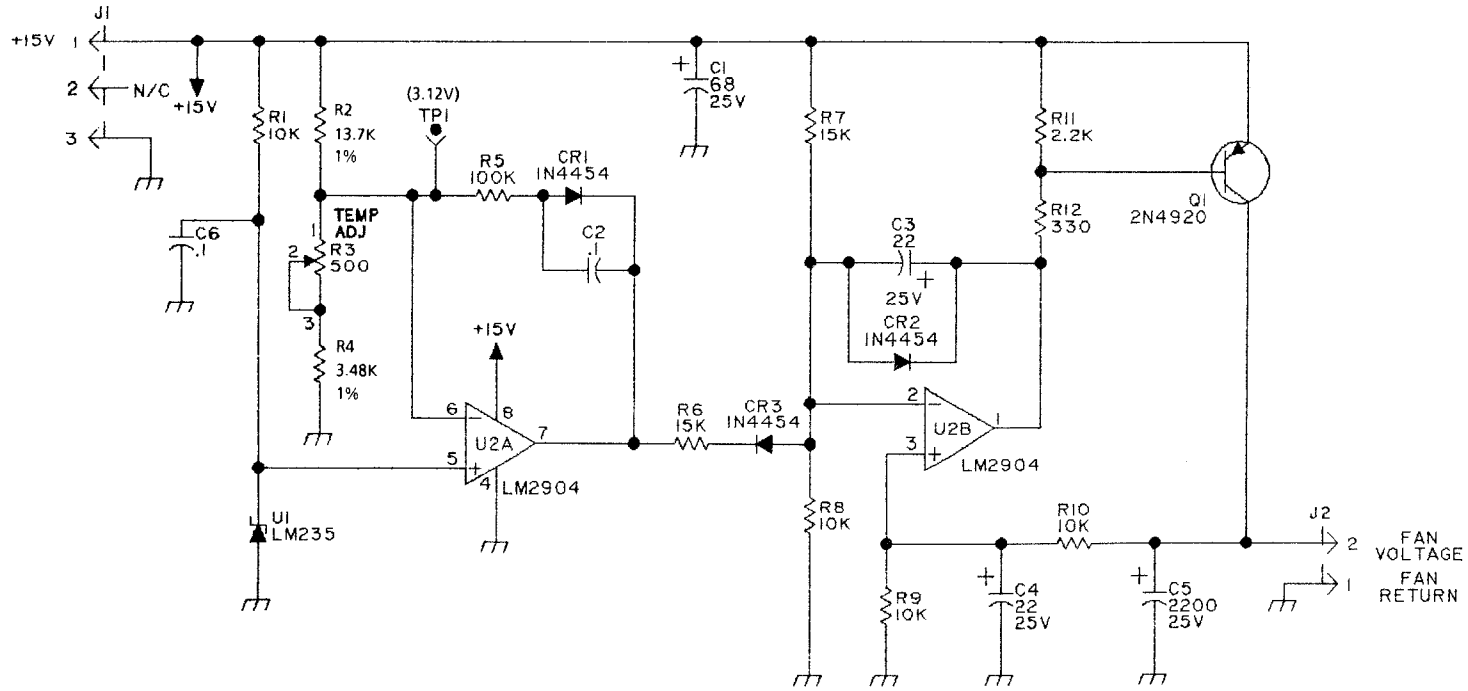


Figure 6-33. Fan Speed Control PWB Assembly A12A2 Component Locations (10133-1090, Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.



HSM-908

Figure 6-34. Fan Speed Control PWB Assembly A12A2 Schematic Diagram (10133-1091, Rev. C)

# **ROBUST SERIAL TONE OPTION**

**THIS SECTION IS SUPPLIED WITH  
THE ROBUST SERIAL TONE OPTION  
AS SUPPLEMENT NUMBER SU-10133-0045.**

**GLOSSARY**

Term or Abbreviation	Description
AC	Alternating Current
AM	Amplitude Modulation
ALC	Automatic Level Control
AME	Amplitude Modulation Equivalent
APC	Average Power Control
ARQ	Automatic Repeat on Request
A-to-D	Analog-to-Digital Conversion
BAUD	Data bits per second
bps	Bits per second
BIT	Built-In Test
BITE	Built-In Test Equipment
CCIR	International Radio Consultative Committee
CFE	Customer Furnished Equipment
CLK	Clock
COAX	Coaxial (i.e., coaxial cable)
CPU	Central Processing Unit
CTS	Clear to Send
CW	Continuous Wave; Morse Code Communication
dB	Decibel, logarithmic power ratio
DC	Direct Current
DIAG	Diagnostic
DIP	Dual In-Line Package
DSR	Data Set Ready
DTE	Data Terminal Equipment
D-to-A	Digital-to-Analog Conversion
EIA	Electronic Industries Association
EMI	Electro-Magnetic Interference
FEC	Forward Error Corrections
FFT	Fast Fourier Transform
FIFO	First In First Out
FM	Frequency Modulation
FSK	Frequency Shift Keying
GND	Ground
HF	High Frequency (3-30 MHz)
Hz	Hertz, 1 cycle per second

GLOSSARY (Cont.)

Term or Abbreviation	Description
IC	Integrated Circuit
IFFT	Inverse Fast Fourier Transform
I/O	Input/Output
ISB	Independent Sideband, usually 2-ISB or 4-ISB
kHz	Kilohertz, 1000 Hertz
kW	Kilowatt, 1000 watts
LED	Light Emitting Diode
LPF	Low Pass Filter
LSB	Lower Sideband
LV	Low Voltage
MF	Medium Frequency (300 kHz - 3 MHz)
MHz	Megahertz, 1 Million Hertz
MIC	Microphone
MIL	Military; usually MIL SPEC, Military Specification
MUTE	Controlled no-output condition
PA	Power Amplifier
PCB	Printed Circuit Board
PEP	Peak Envelope Power
PLL	Phase Lock Loop
P/N	Part Number
PPC	Peak Power Control
PS	Power Supply
PSK	Phase Shift Keying
PTT	Push-to-Talk
PWM	Pulse Width Modulated
RATT	Radioteletype
RCV	Receive
RCVR	Receiver
RF	Radio Frequency
RMS	Root Mean Square
RTS	Ready to Send
RTTY	Radioteletype
RS	Receive/Send
RX	Receive (or Receiver)
SNR	Signal to Noise Ratio

**GLOSSARY (Cont.)**

Term or Abbreviation	Description
SSB	Single Sideband
STD	Standard
SWITCHER	Switching Power Supply
Symbol	4 Bits
TDQPSK	Time Differential Quaternary Phase Shift Keying
TGC	Transmitter Gain Control
TTY	Radioteletype
T/R	Transmit/Receive
TX	Transmit (or Transmitter)
UHF	Ultra High Frequency
USART	Universal Synchronous Asynchronous Receiver Transmitter
USB	Upper Sideband
VCA	Voltage Controlled Attenuator
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio
XMIT	Transmit
XMTR	Transmitter