This is a scan of a copy of a reprint. The quality is not very good. This copy contains only the T-827/URT sections of the 94840(A) manual.

To help with difficult-to-read images, use the T-827B/URT manual NAVSHIPS 0967-LP-427-5010 at https://www.navy-radio.com/manuals/wrc1b-cu937-man-7209.pdf

The T-827B differs mainly in having 100Hz increments instead of 500Hz increments.

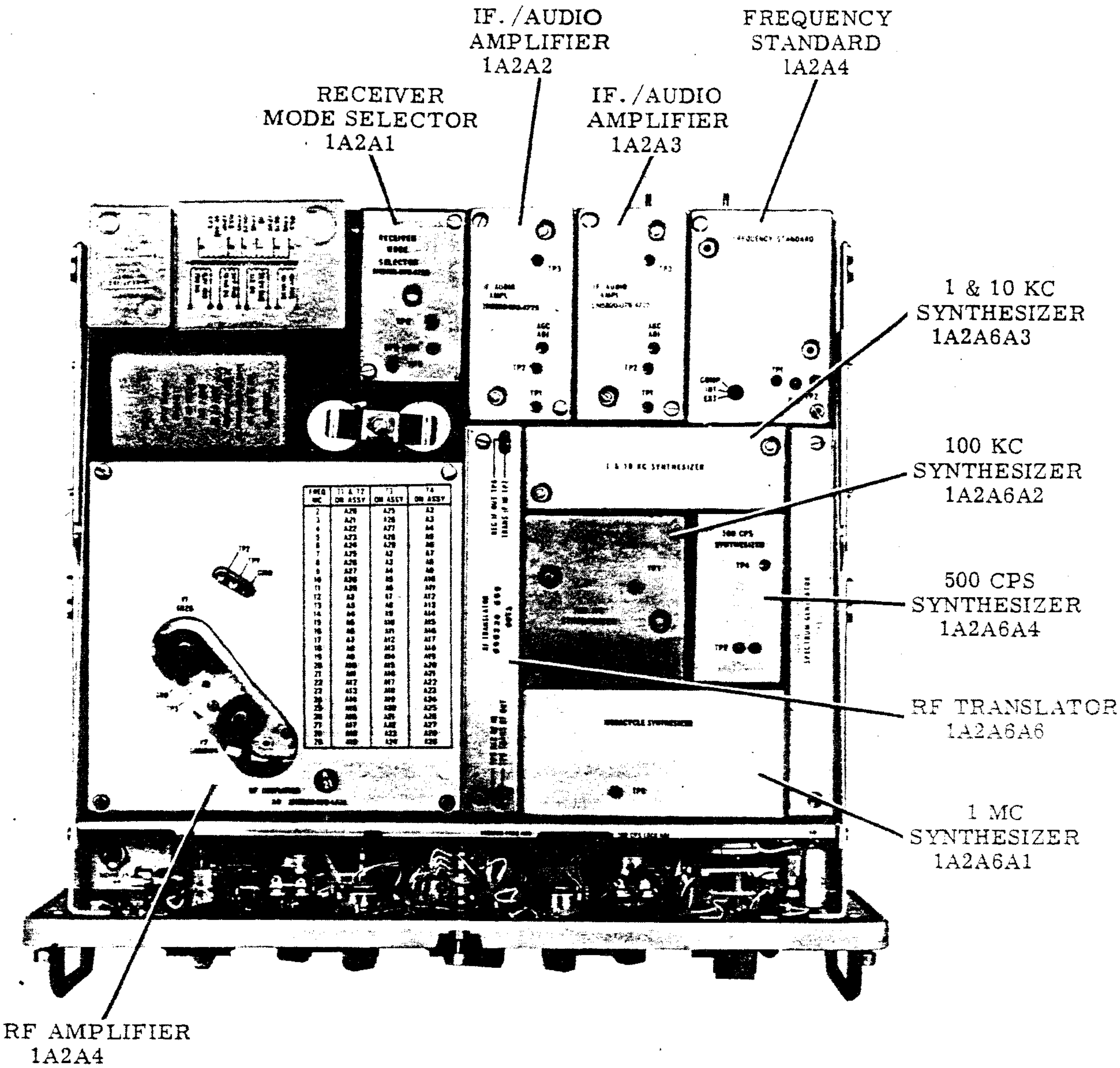


Figure 1-2. Radio Receiver R-1051/URR, Top View, Case Removed

1-14. DESCRIPTION OF RADIO TRANSMITTER T-827/URT.

1-15. FUNCTION. The function of the T-827/URT is to provide a USB, ISB, LSB, CW, FSK, or compatible AM rf signal of sufficient power to drive the AM-3007/URT. The operating frequency range of the T-827/URT is from 2.0 to 29.9995 megacycles.

1-16. PHYSICAL CHARACTERISTICS. The physical characteristics of the T-827/URT are the same as those for the R-1051/URT (see paragraph 1-12). The T-827/URT is illustrated in figures 1-4 and 1-5.

1-17. ELECTRICAL CHARACTERISTICS. The T-827/URT is a low level transmitter, which produces a nominal 0.1 watt rf output, making

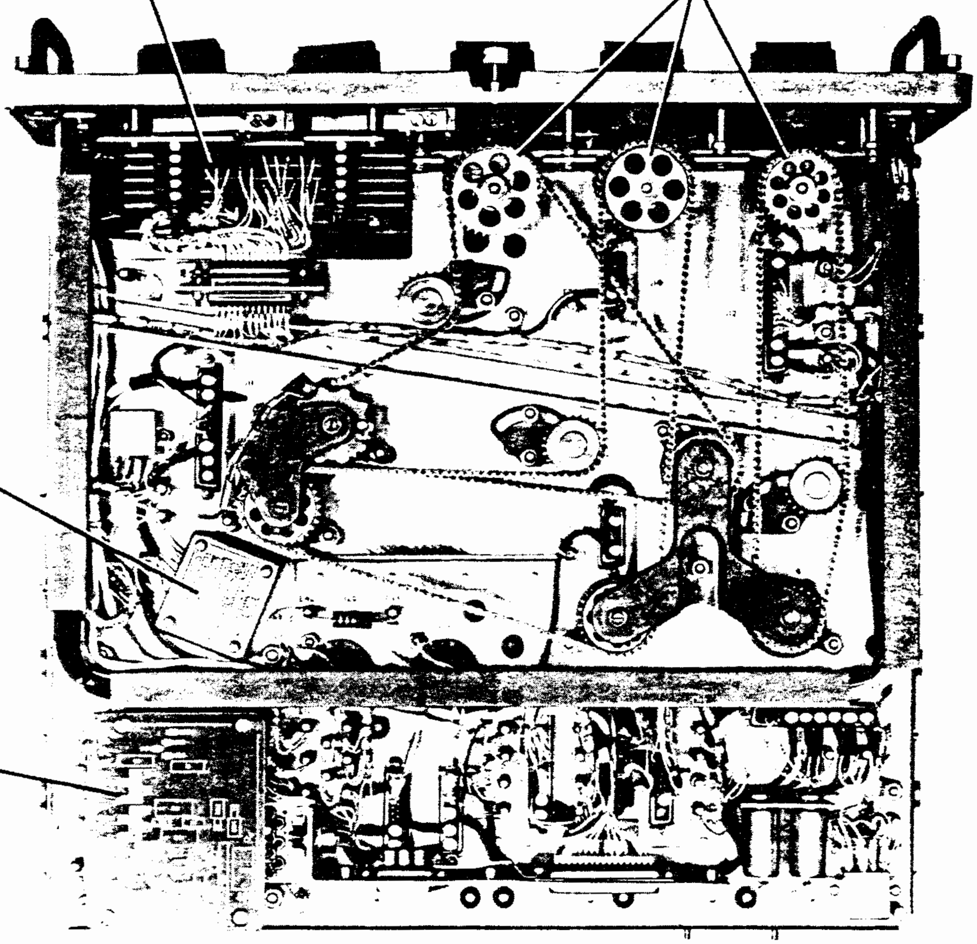


Figure 1-3. Radio Receiver R-1051/URR, Bottom View, Case Removed

it capable of driving the AM-3007/URT. Like the R-1051/URR, the T-827/URT employs a digital tuning scheme for automatically tuning to any one of 56,000 channels in 500 cps steps in the 2.0 to 29.9995-megacycle frequency range. All circuits of the T-827/URT (except two rf amplifier stages) utilize solid-state devices. These circuits are assembled into plug-in electronic assemblies, some of which are interchangeable between the R-1051/URR and the T-827/URT (see paragraph 5-46). The frequency generation circuits, which are referenced to an ultra-stable master frequency standard with a stability better than 1 part in 10^8 per day provide an extremely stable transmitter output.

1-18. DESCRIPTION OF RF AMPLIFIER AM-3007/URT.

1-19. FUNCTION. The function of the AM-3007/URT is to provide linear amplification of the

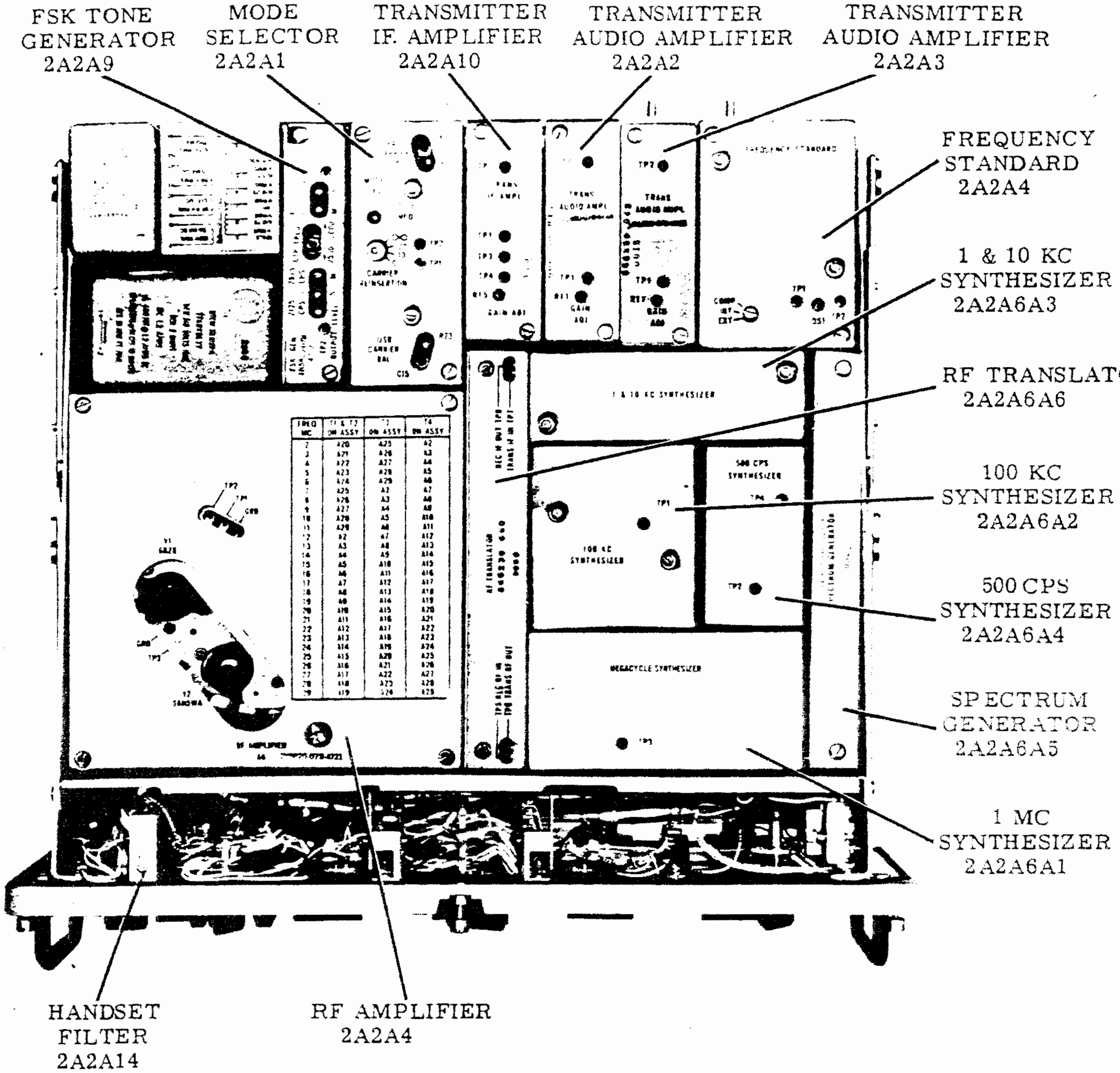


Figure 1-4. Radio Transmitter T-827/URT, Top View, Case Removed

level rf output from the T-827/URT for
ication to a 50-ohm antenna system or
ugh the CU-937/UR to a whip antenna for
agation.

ı. PHYSICAL CHARACTERISTICS. Like
T-827/URT and the R-1051/URR, the
3007/URT (figures 1-6 and 1-7) is housed
metal case with the chassis mounted on
er-type slides. All operating controls and
cators for the AM-3007/URT and the CU-937/UR are mounted on the front panel of the AM-3007/URT. The two amplifier tubes in the AM-3007/URT, used to amplify the low level output from the T-827/URT to a nominal 100 watts peak envelope power (PEP), are mounted on a heat sink that is part of the front panel. This heat sink conducts the heat propagated by these tubes to the fins on the front panel of the AM-3007/URT. All control and power supply circuits of the AM-3007/URT are composed of solid-state devices.

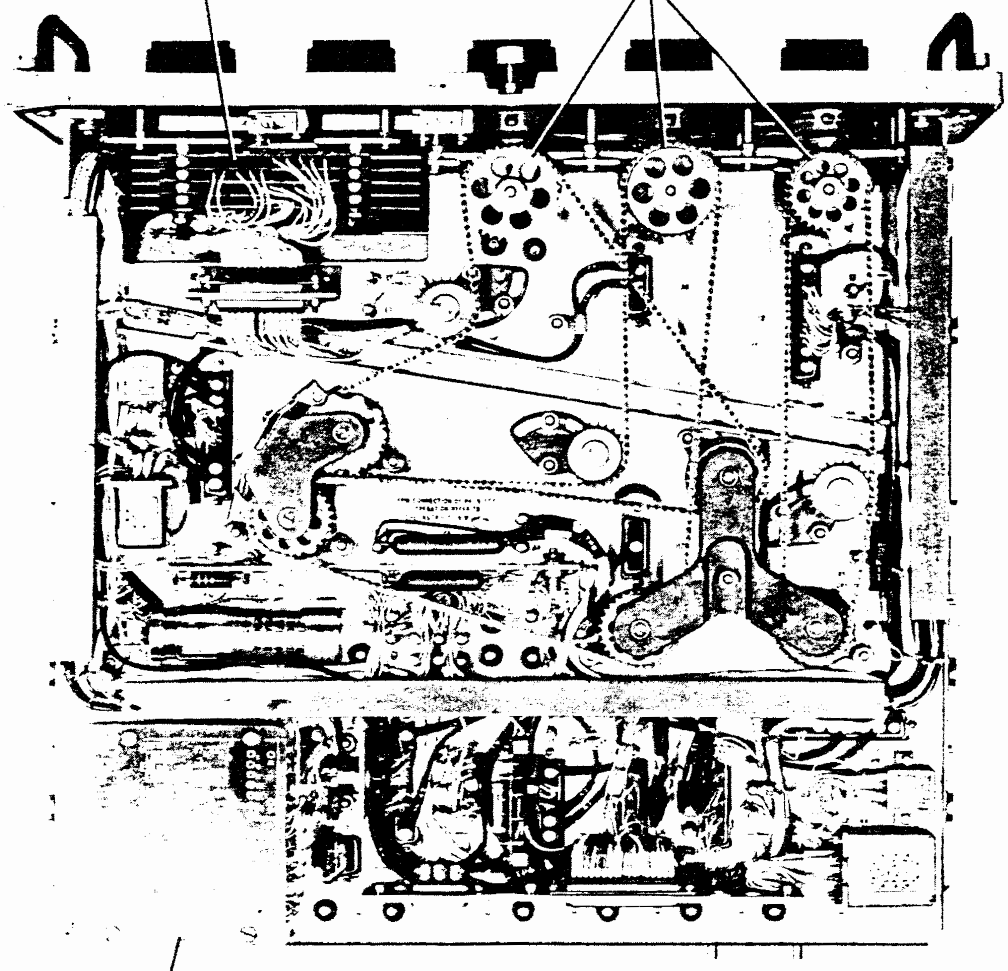


Figure 1-5. Radio Transmitter T-827/URT, Bottom View, Case Removed

1-21. ELECTRICAL CHARACTERISTICS. The AM-3007/URT is a two-stage power amplifier. With an rf input of 0. 1 to 0. 25 watt, it will produce an output of 100 watts PEP SSB, 25 watts AM carrier, or 50 watts average CW or FSK into a 50-ohm load. In the AM and SSB modes, the AM-3007/URT is a linear amplifier. In the CW and FSK modes, the AM-3007/URT operates more nearly class C to increase efficiency. The AM-3007/URT is automatically tuned by a five-wire code from the T-827/URT. This code controls a motor that positions a turret containing broadband coils. These broadband coils act as tuned interstage and output circuits for the two amplifier stages. Another code is generated in the AM-3007/URT to coarse tune the CU-937/UR. An inverse feedback loop is used in the AM-3007/URT to improve linearity and decrease intermodulation distortion.

TABLE 1-2. RADIO TRANSMITTER T-827/URT, CRYSTAL COMPLEMENT

REF. DESIG.	TYPE OF CUT	CRYSTAL OSC. FREQ. (MC)	OPERATING TEMP. RANGE	TOLERANCE (PERCENT)
2A2A5A3Y1	AT	5.000000	84.5°C to 85.5°C	0.001
2A2A6A1Y1	AT	2.498850	0°C to 75°C	0.003
2A2A6A1Y2	AT	3.499720	0°C to 75°C	0.003
2A2A6A1Y3	AT	4.499640	0°C to 75°C	0.003
2A2A6A1Y4	AT	5.499640	0°C to 75°C	0.003
2A2A6A1Y5	AT	7.499400	0°C to 75°C	0.003
2A2A6A1Y6	AT	8.499320	0°C to 75°C	0.003
2A2A6A1Y7	AT	9.499160	0°C to 75°C	0.003
2A2A6A1Y8	AT	10.499160	0°C to 75°C	0.003
2A2A6A1Y9	AT	11.499080	0°C to 75°C	0.003
2A2A6A1Y10	AT	12.499000	0°C to 75°C	0.003
2A2A6A1Y11	AT	14.498840	0°C to 75°C	0.003
2A2A6A1Y12	AT	15.498760	0°C to 75°C	0.003
2A2A6A1Y13	AT	16.498690	0°C to 75°C	0.003
2A2A6A1Y14	AT	17.498600	0°C to 75°C	0.003
2A2A6A1Y15	AT	18.498440	0°C to 75°C	0.003
2A2A6A1Y16	AT	20.498360	0°C to 75°C	0.003
2A2A6A1Y17	AT	23.498120	0°C to 75°C	0.003
2A2A6A2Y1	AT	4.553	0°C to 75°C	0.003
2A2A6A2Y2	AT	4.653	0°C to 75°C	0.003
2A2A6A2Y3	AT	4.753	0°C to 75°C	0.003
2A2A6A2Y4	AT	4.853	0°C to 75°C	0.003
2A2A6A2Y5	AT	4.953	0°C to 75°C	0.003
2A2A6A2Y6	AT	5.053	0°C to 75°C	0.003
2A2A6A2Y7	AT	5.153	0°C to 75°C	0.003
2A2A6A2Y8	AT	5.253	0°C to 75°C	0.003

TABLE 1-2. RADIO TRANSMITTER T-827/URT, CRYSTAL COMPLEMENT (Continued)

REF. DESIG.	TYPE OF CUT	CRYSTAL OSC. FREQ. (MC)	OPERATING TEMP. RANGE	TOLERANCE (PERCENT)
2A2A6A2Y9	AT	5.353	0°C to 75°C	0.003
2A2A6A2Y10	AT	5.453	0°C to 75°C	0.003
2A2A6A3Y1	AT	5.25	0°C to 75°C	0.003
2A2A6A3Y2	AT	5.24	0°C to 75°C	0.003
2A2A6A3Y3	AT	5.23	0°C to 75°C	0.003
2A2A6A3Y4	AT	5.22	0°C to 75°C	0.003
2A2A6A3Y5	AT	5.21	0°C to 75°C	0.003
2A2A6A3Y6	AT	5.20	0°C to 75°C	0.003
2A2A6A3Y7	AT	5.19	0°C to 75°C	0.003
2A2A6A3Y8	AT	5.18	0°C to 75°C	0.003
2A2A6A3Y9	AT	5.17	0°C to 75°C	0.003
2A2A6A3Y10	AT	5.16	0°C to 75°C	0.003
2A2A6A3Y11	AT	1.850	0°C to 75°C	0.003
2A2A6A3Y12	AT	1.851	0°C to 75°C	0.003
2A2A6A3Y13	AT	1.852	0°C to 75°C	0.003
2A2A6A3Y14	AT	1.853	0°C to 75°C	0.003
2A2A6A3Y15	AT	1.854	0°C to 75°C	0.003
2A2A6A3Y16	AT	1.855	0°C to 75°C	0.003
2Z2A6A3Y17	AT	1.856	0°C to 75°C	0.003
2A2A6A3Y18	AT	1.857	0°C to 75°C	0.003
2A2A6A3Y19	AT	1.858	0°C to 75°C	0.003
2A2A6A3Y20	AT	1.859	0°C to 75°C	0.003

4-22. RADIO RECEIVER R-1051/URR, FUNCTIONAL DESCRIPTION.

4-23. Refer to Technical Manual for Radio Receiver R-1051/URR (NAVSHIPS 94841(A)) for functional description, circuit descriptions, test data, and schematic diagram coverage of the R-1051/URR.

4-24. RADIO TRANSMITTER T-827/URT, FUNCTIONAL DESCRIPTION.

4-25. The T-827/URT consists of eight plug-in electronic assemblies. One assembly consists of six electronic subassemblies. These electronic assemblies and subassemblies convert audio or coded intelligence to one of 56,000 possible operating rf frequencies in the 2.0-to-29.9995-mc frequency range for either LSB, USB, ISB, CW, FSK, or compatible AM mode of operation. The rf output from the T-827/URT is at a nominal 0.1-watt power level, with a maximum power output of 0.25 watt. Figure 4-2 illustrates the functional groups of circuits comprising the T-827/URT.

4-26. MAIN SIGNAL FLOW. The main signal flow in the T-827/URT originates in the 5 mc frequency standard. This circuit is housed in an oven assembly maintained at a nearly constant temperature of 85°C by the oven control circuit. The 5 mc frequency standard produces an accurate, stable reference frequency, upon which all frequencies used in the T-827/URT are based. The accurate output from the 5 mc frequency standard is applied to a switching and compare circuit. An external 5-mc frequency may also be applied to this circuit. The switching and compare circuit routes the internal or external 5-mc signal to the multiplier-divider circuits or to the compare circuit. The compare circuit compares the internal 5-mc frequency with the external 5-mc frequency for an indication of the internal frequency accuracy. The 5-mc output from the switching and compare circuit is applied to the multiplier-divider circuit, where it is converted to frequencies of 500 kc, 1 mc, and 10 mc. All three frequencies are used in the mixing processes required to produce the injection frequencies used in the rf conversion process. The 500-kc frequency output from the multiplier-divider circuit also serves as the local carrier for the T-827/URT. The 5 mc frequency standard, oven control, switching and compare, and multiplier-divider circuits comprise Frequency Standard Electronic Assembly 2A2A5.

4-27. The 500-kc local carrier output from the multiplier-divider circuit is applied to the 500 kc if. amplifiers. These circuits amplify the 500-kc local carrier to a level suitable for use in the balanced modulators. There are two balanced modulators, identical except for output filtering. The balanced modulator used is selected according to the mode of operation. One balanced modulator is used in the USB, FSK, AM, and ISB modes of operation. The other balanced modulator is used during the LSB and ISB modes of operation. Neither balanced modulator is used during the CW mode of operation. Audio intelligence from the audio amplifier is applied to the appropriate balanced modulator to modulate the 500-kc local carrier, resulting in a double sideband signal without a carrier. The double sideband signal is filtered according to the mode of operation to remove either the LSB or USB portion of the signal. The 500 kc if. amplifiers and the balanced modulators circuits comprise a part of Transmitter Mode Selector Electronic Assembly 2A2A1. The other portion of this assembly is the control gates-sidetone oscillator circuit, which is functionally explained in paragraphs 4-31 and 4-34.

4-28. The 500-kc if. output from the balanced modulators is applied to the if. amplifiers. The if. amplifiers, which comprise Transmitter IF. Amplifier Electronic Assembly 2A2A12, provide a 500-kc if. output at a level suitable for use in the low and mid-frequency mixers circuit. The level of the 500-kc if. output from the if. amplifiers is prevented from exceeding a predetermined peak and average power level by application of the average power control (apc) and the peak power control (ppc) signals produced in RF Amplifier AM-3007/URT. The 500-kc local carrier is re-inserted into the 500-kc if. signal during the AM mode of operation in the if. amplifiers circuit. The unmodulated 500-kc if. signal for CW mode of operation is also produced by this circuit. The 500-kc carrier required in both the AM and CW modes of operation is applied to the if. amplifiers circuit by the control gates-sidetone oscillator circuit contained in Transmitter Mode Selector Assembly 2A2A1.

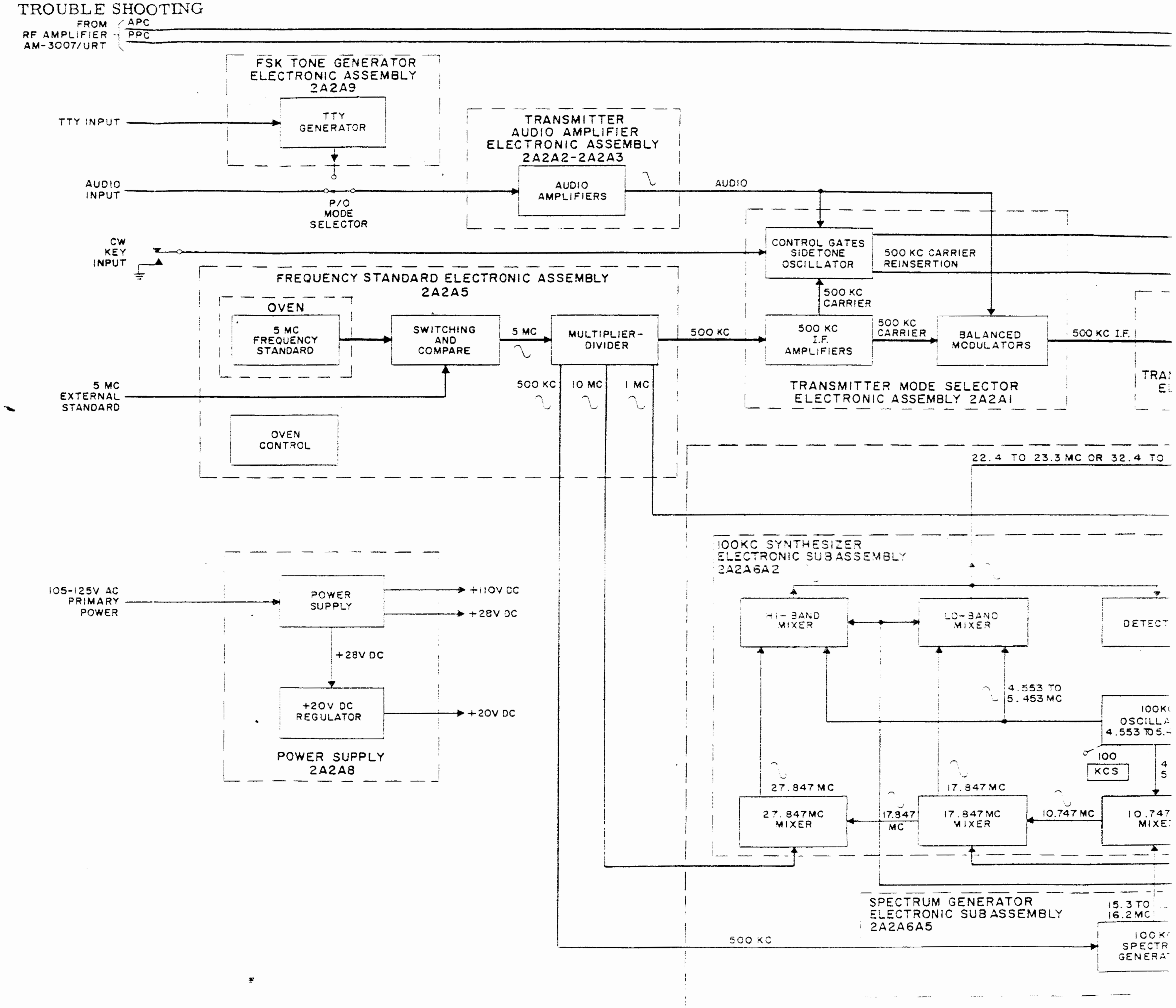
4-29. The output from the if. amplifiers circuit is applied to the low and mid frequency mixers. These two mixer circuits, which comprise a part of Translator Electronic Subassembly 2A2A6A6, in conjunction with the high frequency mixer circuit portion of RF Amplifier Electronic Assembly 2A2A12, convert the c if. signal to the desired rf frequency by le conversion process. The 500-kc if. l is mixed with the 1- and 10-kc injection ency by the low frequency mixer to pro- a second if. frequency between 2.8 and ıc (Refer to paragraph 4-39.) This fre- y is filtered and applied to the mid fre- y mixer. The second if. is mixed with 00-kc injection frequency by the mid fre- y mixer to produce a third if. between and 20.5 mc or between 29.5 and 30.5 mc r to paragraph 4-39.) The third if. used ermined by the hi/lo band control signal.

The output from the mid frequency is filtered and applied to the high fre- y mixer. The third if. is mixed with the jection frequency by the high frequency to produce the desired rf output frequen- The mc injection frequency is determined position at which the mc frequency gen- r is set by the code from the code genera- The output from the high frequency mixer lied to the rf amplifiers, which amplify frequency to a level suitable to drive the 007/URT. The input and output circuits rf amplifiers are automatically tuned by ning code produced by the code generator, ding to the frequency of the desired oper- channel. The high frequency mixer and amplifiers comprise RF Amplifier Elec- Assembly 2A2A12.

AUDIO SIGNAL FLOW. The intelligence d to the T-827/URT is either the coded for CW, the coded keying for FSK, or dio for all other modes of operation. The CW keying turns a gating circuit on and the control gates-sidetone oscillator t. Each time the key is depressed, the s turned on, allowing the 500-kc local r to pass from the 500 kc amplifiers to amplifiers. Also, each time the CW depressed, the output of a sidetone ator is gated through to the sidetone line. idetone signal is applied to the R-1051/ enabling the operator to monitor the CW . The audio output from the microphone lied to the audio amplifiers in Trans- Audio Amplifier Electronic Assemblies and 2A2A3. When operating in the USB, M, or FSK modes of operation, the input is amplified by assembly 2A2A2 applied to the appropriate balanced ator. When operating in the LSB and ISB of operation, the audio is amplified by bly 2A2A3 and is applied to the appro- priate balanced modulator. A gate for each assembly is turned on in the control gates-sidetone oscillator, when the corresponding assembly is turned on. This gate allows the audio to pass as a sidetone signal to the R-1051/URR, enabling the operator to monitor the respective transmission. When operating in the FSK mode of operation, the coded TTY input is applied to the TTY generator in FSK Tone Generator Electronic Assembly 2A2A9. The TTY generator produces the required mark and space frequencies and applies them to Transmitter Audio Amplifier Electronic Assembly 2A2A2. The gate for re-inserting the 500-kc carrier into the if. signal during AM operation is also contained in the control gates gates-sidetone oscillator circuit. This circuit also has a gating network for re-inserting a pilot local carrier into the if. signals during LSB, USB, or ISB operation. The pilot carrier is used when operating with radio sets less stable than the AN/WRC-1, providing them with a carrier for frequency locking and demodulating.

4-32. FREQUENCY GENERATION. The injection frequencies used in the first frequency conversion in the mixers circuit are generated within the 1 and 10 kc Synthesizer Electronic Subassembly 2A2A6A3. This circuit consists of two crystal oscillators, each of which has ten possible output frequencies. The output from the 1 kc oscillator (1.850 mc to 1.859 mc, in 1 kc steps) is determined by the setting of the front panel 1 kc (KCS) control, and the output from the 10 kc oscillator (5.25 mc to 5.16 mc, in 10 kc steps) is determined by the setting of the front panel 10 kc (KCS) control. The outputs from the two oscillators are subtractively mixed to produce one of 100 possible frequencies spaced at the 1 kc intervals between 3.301 and 3.400 mc. The output is applied to the low frequency mixer.

4-33. The injection frequencies used in the second frequency conversion in the mixers circuit are generated within the 100 KC Synthesizer Electronic Subassembly 2A2A6A2. This circuit consists of a crystal oscillator, the output from which is one of ten frequencies spaced at 100 kc intervals between 4.553 and 5.453 mc. The output frequency is determined by the setting of the front panel 100 kc (KCS) control. If a lo-band injection frequency is required (see paragraph 4-39) the 17.847 mc output from the 17.847 mc mixer is additively mixed in the hi-band mixer with the output from the 100 kc oscillator (4.553 mc to 5.453 mc, in 100 kc


FROM RF AMPLIFIER AM-3007/URT
APC
PPC
FSK TONE GENERATOR ELECTRONIC ASSEMBLY 2A2A9
TTY INPUT
TTY GENERATOR
AUDIO INPUT
P/O MODE SELECTOR
TRANSMITTER AUDIO AMPLIFIER ELECTRONIC ASSEMBLY 2A2A2-2A2A3
AUDIO AMPLIFIERS
AUDIO
CW KEY INPUT
CONTROL GATES SIDETONE OSCILLATOR
500 KC CARRIER REINSERTION
500 KC CARRIER
FREQUENCY STANDARD ELECTRONIC ASSEMBLY 2A2A5
OVEN
5 MC FREQUENCY STANDARD
SWITCHING AND COMPARE
5 MC
MULTIPLIER-DIVIDER
500 KC
500 KC I.F. AMPLIFIERS
500 KC CARRIER
BALANCED MODULATORS
500 KC I.F.
TRANSMITTER MODE SELECTOR ELECTRONIC ASSEMBLY 2A2A1
5 MC EXTERNAL STANDARD
500 KC
10 MC
1 MC
OVEN CONTROL
22.4 TO 23.3 MC OR 32.4 TO
100KC SYNTHESIZER ELECTRONIC SUBASSEMBLY 2A2A6A2
HI-BAND MIXER
LO-BAND MIXER
DETECT
105-125V AC PRIMARY POWER
POWER SUPPLY
+110V DC
+28V DC
+28V DC
+20V DC REGULATOR
+20V DC
POWER SUPPLY 2A2A8
4.553 TO 5.453 MC
100KC OSCILLA 4.553 TO 5.
100
KCS
27.847 MC
17.847 MC
27.847MC MIXER
17.847 MC
17.847MC MIXER
10.747MC
10.747 MIXE
SPECTRUM GENERATOR ELECTRONIC SUBASSEMBLY 2A2A6A5
15.3 TO 16.2MC
500 KC
100 KC SPECTR GENERA

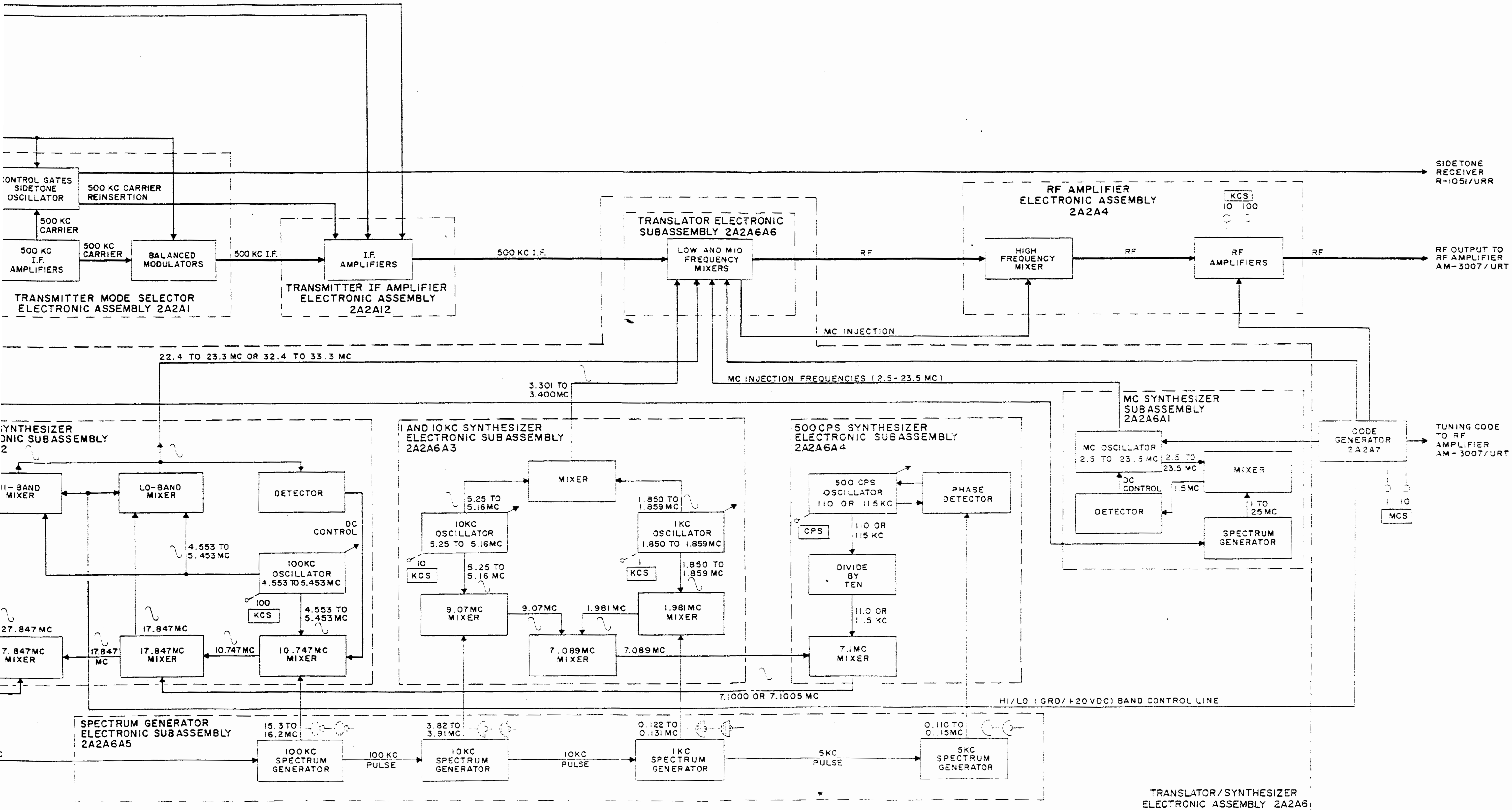


Figure 4-2. Radio Transmitter T-827/URT, Functional Block Diagram

steps) to provide a frequency in the 22.4 to 23.3 mc range. If a hi-band injection is required (see paragraph 4-39) the 27.847 mc output from the 27.847 mc mixer is additively mixed in the hi-band mixer with the output from the 100 kc oscillator (4.553 mc to 5.453 mc, in 100 kc steps) to provide a frequency in the 32.4 to 33.3 mc range. In either case, the resultant frequency is applied to the mid frequency mixer.

4-34. The injection frequencies used in the third frequency conversion in the mixers circuit are generated within the MC Synthesizer Electronic Subassembly 2A2A6A1. This circuit consists of a phase-locked crystal oscillator that is automatically tuned to produce one of seventeen frequencies between 2.5 mc and 23.5 mc. The output is applied to the high frequency mixer. The output frequency is determined by the setting of the front panel MCS controls.

4-35. ERROR CANCELLATION. A combination of error cancelling loops and phase-locked loops is used in the frequency synthesizer circuits of the T-827/URT to ensure that the injection frequencies applied to the mixers are correct. The MC Synthesizer Electronic Subassembly (2A2A6A1) employs a phase-locked loop to ensure the accuracy of the mc injection frequencies. The 1 mc output from the multiplier-divider in the Frequency Standard Electronic Assembly (2A2A5) is applied to the spectrum generator to produce a spectrum of frequencies spaced at 1 mc intervals between 1 mc and 25 mc. The output from the spectrum generator and the output from the mc oscillator are mixed. Any error in output from the mc oscillator is detected and an error voltage is produced. This error signal is applied to the mc oscillator to lock it to the correct frequency. The accuracy of the oscillator output is the same as that of the 5 mc frequency standard.

4-36. The 100 KC Synthesizer Electronic Subassembly (2A2A6A2) employs an error canceling loop to ensure the accuracy of the 100 kc injection frequencies. The 500 kc output from the multiplier-divider is applied to the 100 kc spectrum generator to produce a spectrum of frequencies spaced at 100 kc intervals between 15.3 mc and 16.2 mc. The output from the 100 kc oscillator (4.553 mc to 5.453 mc, in 100 kc steps) is applied to the 10.747 mc mixer, where it is mixed with that spectrum point of the 100 kc spectrum which will result in an output of 10.747 mc. The 10.747 mc signal is additively mixed with the 7.1 mc output from the 7.1 mc mixer to produce the 17.847 mc signal, which is used in one of two mixing processes. It is mixed with the 100 kc oscillator output to cancel any oscillator frequency error and produce the lo-band injection frequencies, or it is mixed with the 10 mc output from the multiplier-divider. This mixing produces a 27.847 mc signal, which is mixed with the 100 kc oscillator output to cancel any oscillator frequency error and produce the hi-band injection frequencies. The hi or lo-band of injection frequencies is determined by the voltage level on the hi/lo band control line output from the code generator. If an error were present in the 100 kc oscillator output, it would be cancelled in this mixing scheme. This is accomplished as follows. Assume that the output from the oscillator should be 4.553 mc, but is 200 cycles high (4.5532 mc), and that the desired frequency output is 22.4 mc (in the lo band). The subtractive mixing of the oscillator output with whichever 100 kc spectrum point will produce an output as close as possible to 10.747 mc, results in a 10.7468 mc output (15.3 mc - 4.5532 mc = 10.7468 mc). This signal is then additively mixed with the 7.1 mc signal, producing a 17.8468 mc output. The 17.8468 mc signal is then additively mixed with the oscillator output (17.8468 mc + 4.5532 mc = 22.4 mc), resulting in the desired 22.4 mc output. Assume that the output from the oscillator should be 4.953 mc, but is 300 cycles low (4.9527 mc), and that the desired frequency output should be 32.8 mc (in the hi-band). Subtractively mixing the 100 kc spectrum point (15.7 mc) with the 4.9527 mc signal results in an output of 10.7473 mc. This signal is then mixed with the 7.1 mc signal, resulting in a frequency of 17.8473 mc. The 17.8473 mc signal is further mixed with the 10 mc signal to obtain a frequency of 27.8473 mc, which is additively mixed with the 4.9527 mc output from the oscillator to obtain the required 32.8 mc output. Therefore, it can be seen that any error existing in the output from the 100 kc oscillator will be cancelled, resulting in the exact 100 kc injection frequency required.

4-37. Any error existing in the 1 and 10 kc oscillator is cancelled in the following manner. The 100 kc pulses from the 100 kc spectrum are applied to the 10 kc spectrum generator producing an output from 3.82 to 3.91 mc in 10 kc increments. The 10 kc spectrum generator also produces 10 kc pulses which are applied to the 1 kc spectrum generator to produce

spectrum of frequencies spaced at 1 kc inter-
ıls between 0.122 mc and 0.131 mc. The out-
ıt from the 10 kc oscillator (5.25 mc to 5.16
c, in 10 kc steps) is additively mixed with
hichever spectrum point of the 10 kc spec-
um will result in a frequency of 9.07 mc.
he output from the 1 kc oscillator (1.850 mc
1.859 mc, in 1 kc steps) is additively mixed
ith whichever spectrum point of the 1 kc
ectrum will result in a frequency of 1.981
c. The 1.981 mc and the 9.07 mc signals
e then subtractively mixed, producing the
089 mc signal, which contains the errors of
th oscillators. The 1 kc spectrum generator
so produces 5 kc pulses, which are applied
the 5 kc spectrum generator to produce an
tput consisting of two spectrum points, 110
and 115 kc. These spectrum points are
ed to lock the output frequency of the 500 cps
ase-locked oscillator to 110 kc or 115 kc,
en desired. With the front panel CPS switch
the 000 position, the output from the phase-
cked oscillator is 110 kc and is locked to that
act frequency by the 100 kc spectrum point
plied to the phase detector. This 110 kc
gnal is divided by ten and applied to the 7.1
c mixer, where it is additively mixed with
e 7.089 mc output from the 7.089 mc mixer.
e resulting 7.1 mc signal is then applied to
e error loop of the 100 KC Synthesizer Elec-
onic Subassembly (2A2A6A2). Therefore, if
error exists in the 1 or 10 kc oscillators,
e same error will exist in the 100 kc injection
equencies. This error is then cancelled in
e low and mid frequency mixers of the mixers
rcuit in the following manner. Assume that
e output from the 10 kc oscillator should be
25 mc, but is actually 5.2502. Also assume
t the output from the 1 kc oscillator should
1.852 mc but is actually 1.8521 mc. Sub-
ctively mixing these two frequencies results
an injection frequency to the low frequency
xer of 3.3981 mc, rather than the desired
3980 mc. Therefore, a 100 cycle error
sts in the injection signal. The additive
xing of the 5.2502 mc signal and the 10 kc
ectrum point (3.82 mc) results in a frequency
9.0702 mc. The additive mixing of the
8521 mc signal and the 1 kc spectrum point
129) results in a frequency of 1.9811 mc.
tractively mixing the 9.0702 mc and the
811 mc signals results in a frequency of
891 mc. The 7.0891 mc signal is mixed
h the 11 kc signal from the divider by ten
cuits resulting in a frequency of 7.1001 mc,
ch is mixed with the 10.747 mc signal to
duce a frequency of 17.8471 mc. If the out-
from the 100 kc oscillator is assumed to be
4.553 mc, then the 100 kc injection frequency would be 22.4001 mc. The 100 kc injection is then also 100 cycles high. Therefore, when the 1 and 10 kc injection frequency of 3.3981 mc (which is 100 cycles high) is subtractively mixed in the low frequency mixer with the output from the mid frequency mixer (which is 100 cycles high), the error will be cancelled. Therefore, since any error that existed in the 1 and 10 kc injection also exists in the 100 kc injection, the error is cancelled during the translation process.

4-38. The T-827/URT can be tuned in 0.5 kc increments. This is accomplished by locking the output of the 500 cps oscillator to 115 kc. Therefore, when the 11.5 kc (after division by ten) is mixed with the 7.089 mc error frequency, a frequency of 7.1005 mc is obtained. Therefore, the 100 kc injection frequency will be 500 cps high. Thus, the output from the mid frequency mixer may be varied in 500 cps increments. The 115 kc output from the 500 cps oscillator is obtained when the CPS switch is placed in the 500 position.

4-39. The 500-kc if. is converted to the desired rf as follows. Assume that the front panel controls are set for a frequency output of 13,492,500 cps. (Refer to figure 4-3 for the frequency scheme for the T-827/URT.) The 1-and 10-kc injection is that frequency of the 10kc oscillator corresponding to the 10-kc digit (9) minus that frequency of the 1 kc oscillator corresponding to the 1-kc digit (2). As shown on figure 4-3, this results in an injection frequency (5.16 mc minus 1.852 mc) of 3.308 mc. The 3.308 mc is subtractively mixed with the 500-kc if. in the low frequency mixer producing a second if. of 2.808 mc. This signal is filtered and applied to the mid frequency mixer to be subtractively mixed with the 100-kc injection. To determine the 100-kc injection frequency, it must be first noted whether the mc digit to be used results in a hi or lo frequency. In this case, the selected mc digits (13) are in the hi-band. Therefore, the 100-kc injection must correspond. It also must be noted that the CPS switch is in the 500 position. Therefore, the correct 100-kc injection frequency is 32.8005 mc. When the 2.808 mc is subtractively mixed with the 32.0005 mc in the mid frequency mixer, the resulting third if. is 29.9925 mc. This frequency is filtered and applied to the high frequency mixer, where it is subtractively mixed with the mc injection corresponding to

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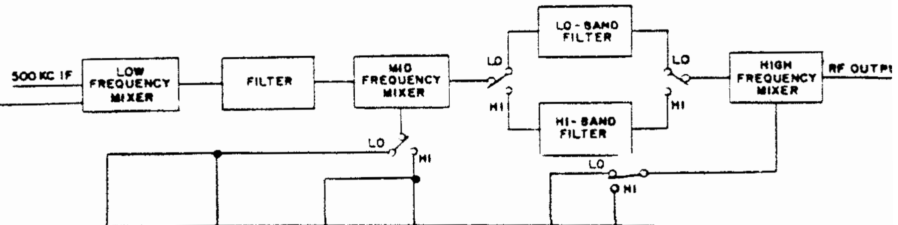

1 KCS	1 KC OSC	10 KCS	10 KC OSC	1 AND 10 KC INJ.	100 KCS	100 KC OSC	LO 000 CPS	LO 500 CPS	HI 000 CPS	HI 500 CPS	MCS	LO	HI
0	1.850	0	5.25	3.400 TO 3.391	0	4.553	22.4000	22.4005	32.4000	32.4005	2	17.5	
1	1.851	1	5.24	3.390 TO 3.381	1	4.653	22.5000	22.5005	32.5000	32.5005	3	16.5	
2	1.852	2	5.23	3.380 TO 3.371	2	4.753	22.6000	22.6005	32.6000	32.6005	4	15.5	
3	1.853	3	5.22	3.370 TO 3.361	3	4.853	22.7000	22.7005	32.7000	32.7005	5	14.5	
4	1.854	4	5.21	3.360 TO 3.351	4	4.953	22.8000	22.8005	32.8000	32.8005	6		23.5
5	1.855	5	5.20	3.350 TO 3.341	5	5.053	22.9000	22.9005	32.9000	32.9005	7	12.5	
6	1.856	6	5.19	3.340 TO 3.331	6	5.153	23.0000	23.0005	33.0000	33.0005	8	11.5	
7	1.857	7	5.18	3.330 TO 3.321	7	5.253	23.1000	23.1005	33.1000	33.1005	9		20.5
8	1.858	8	5.17	3.320 TO 3.311	8	5.353	23.2000	23.2005	33.2000	33.2005	10		19.5
9	1.859	9	5.16	3.310 TO 3.301	9	5.453	23.3000	23.3005	33.3000	33.3005	11	8.5	
											12	7.5	
											13		16.5
											14	5.5	
											15	4.5	
											16	3.5	
											17		12.5
											18		11.5
											19		10.5
											20		9.5
											21		8.5
											22	2.5	
											23	3.5	
											24		5.5
											25		4.5
											26		3.5
											27	7.5	
											28	8.5	
											29	9.5	

Figure 4-3. Frequency Translation, Functional Block Diagram

the selected mc digits (13). This results in the desired output frequency of 13.4925 mc (29.9925 - 16.5 = 13.4925). Similarly, the 500-kc if. frequency can be translated to any one of the possible 56,000 operating channels.

4-40. POWER SUPPLIES. The operating voltages for all circuits in the T-827/URT are produced by Power Supply Assembly 2A2A8 (see figure 4-2). The 105 to 125 vac primary power is converted to dc voltages of 110 vdc (rf amplifier tubes plate and screen supply), -30 vdc (rf amplifier tubes bias), and 28 vdc (general use). The 28 vdc is also regulated to 20 vdc. The 20 vdc is used for operating voltage in the semiconductor circuits of the T-827/URT.

4-41. RADIO TRANSMITTER T-827/URT, TEST DATA.

4-42. Pertinent references and applicable test data for the T-827/URT are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Radio Transmitter T-827/URT, Servicing Block Diagram, Figure 4-70.

c. Required Test Equipment:

(1) Oscilloscope, AN/USM-105A.

(2) RF Signal Generator, CAQI-606A.

(3) Audio Signal Generator, AN/URM-12

(4) Electronic Multimeter, AN/USM-116 (with T-Probe).

(5) Electronic Multimeter, ME-6 ( )/U.

(6) Multimeter, AN/PSM-4.

(7) Analyzer Test Set, TS-1379/U.

(8) Resistor, 50 ohms, 2 watts.

(9) Frequency Meter, CAQI-524D.

(10) Electronic Multimeter, CCVO-91CA.

(11) Electrical Dummy Load, DA-91A/U.

(12) Amplifier Test Set, TS-2132/WRC-1.

(13) Translator/Synthesizer Test Set, -2133/WRC-1.

(14) Frequency Standard Test Set, -2134/WRC-1.

(15) Common Electrical Circuits Test Set, -2135/WRC-1.

(16) Frequency Standard, AN/URQ-9.

(17) Heterodyne Voltmeter, Bruel and er, Model 2005.

l. Power Supply 2A2A8 Voltages:

(1) +19.9 to +20.1 vdc.

(2) +27 to +32 vdc.

(3) +105 to +115 vdc.

e. Power Output: 2.25 vac (represents 0.1 t, with 150 mv in).

. Carrier Suppression: -50 db SSB, 0 AM.

;. Adjustments:

(1) Audio Gain (paragraph 5-11).

(2) IF. Gain (paragraph 5-11).

(3) 5 MC (paragraph 5-11).

(4) 500 CPS Lock (paragraph 5-11).

(5) AM Modulation Percentage (para- h 5-11).

(6) Carrier Balance (paragraph 5-11).

(7) +20 VDC Regulator (paragraph 5-6).

. Components and Test Point Locations:

(1) Radio Transmitter T-827/URT, Top , Case Removed, Figure 5-24.

(2) Radio Transmitter T-827/URT, m View, Case Removed, Figure 5-26.

Refer to Maintenance Standards Book for Set AN/WRC-1 and Antenna Coupler CU-937/UR, NAVSHIPS 94840.42(A) for all test information.

4-43. RADIO TRANSMITTER T-827/URT, CIRCUIT DESCRIPTIONS.

4-44. 5 MC FREQUENCY STANDARD, FUNCTIONAL CIRCUIT DESCRIPTION. The 5 mc frequency standard (figure 4-4) consists of an oscillator (Q5) and a buffer amplifier (Q6). These circuits, which form a part of Frequency Standard Electronic Assembly 2A2A5, provide an accurate 5.000000-mc signal used as a standard throughout the T-827/URT. Assembly 2A2A5A2 is housed in an oven maintained at a constant 85°C temperature by the oven control circuit. The 5 mc frequency standard circuit is used during all modes of operation. The following paragraphs describe the operation of this circuit in detail.

4-45. The frequency of oscillator Q5 is 5.000000 mc as determined by the parallel resonant tuned circuit consisting of capacitor C7 and the primary of transformer T2. Oscillator frequency is controlled by the series resonant circuit consisting of parallel capacitors 2A2A5C1 and C10, and crystal Y1. To sustain oscillation, feedback for oscillator Q5 is obtained from a tap on the primary of transformer T2 and passed through trimmer capacitor 2A2A5C1, capacitors C10 and C9, and crystal Y1 to the emitter of oscillator Q5. The series resonant circuit allows only a 5.000000-mc signal to pass, holding oscillator Q5 to oscillations at exactly 5 mc. The amplitude of oscillator Q5 output is limited by diodes CR5 and CR6. Stable operating voltages of 15 vdc and 7.5 vdc are assured by resistor R12 and two 7.5-volt Zener diodes CR3 and CR4 in series across the 28 vdc supply. Base bias for oscillator Q5 is taken from the junction of Zener diodes CR3 and CR4 and is applied through resistor R14 to the base of oscillator Q5. Capacitor C8 is the bypass capacitor. Resistor R16 is the emitter load resistor.

4-46. The output from oscillator Q5 is coupled by transformer T2 to the base of buffer amplifier Q6, where it is amplified. The output load for buffer amplifier Q6 is tuned to transformer T3. A tap on the primary of transformer T3 supplies negative feedback to the emitter circuit of buffer amplifier Q6, assuring amplifier stability.

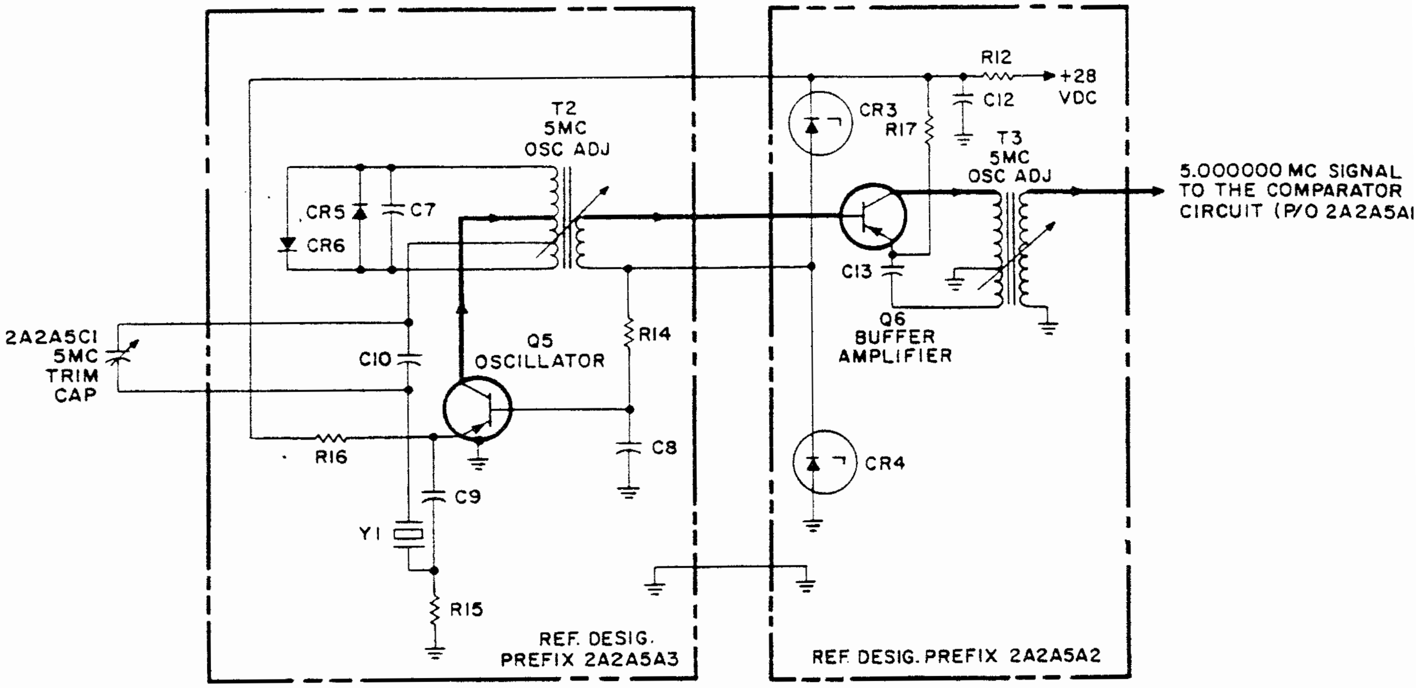

Figure 4-4. 5 MC Frequency Standard, Simplified Schematic Diagram

4-47. 5 MC FREQUENCY STANDARD, TEST DATA. Pertinent references and applicable test data for the 5 mc frequency standard are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Frequency Standard Electronic Assembly, Servicing Block Diagram, Figure 4-71.

c. Frequency Standard Electronic Assembly, Schematic Diagram, Figure 5-9.

d. Refer to paragraph 2-29 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR-2N Modules, NAVSHIPS 95700 for 5 mc oscillator circuit alignment.

e. Required Test Equipment:

(1) Frequency Standard, AN/URQ-9.

(2) Electronic Multimeter, CCVO-91CA.

(3) Frequency Meter, CAQI-524D.

(4) Multimeter, AN/PSM-4.

(5) Frequency Standard Test Set, TS-2134/WRC-1.

f. Output frequency: 5,000,000.5 to 4,999,999.5 cps.

g. 5 MC Frequency Standard, Component Location, Figure 5-73.

h. Oven Control and Buffer Amplifier, Component Location, Figure 5-72.

4-48. OVEN CONTROL, FUNCTIONAL CIRCUIT DESCRIPTION. The oven control (figure 4-5) consists of an oscillator (Q1, Q2), an emitter follower (Q3), a dc power amplifier (2A2A5Q4), and an oven heater (2A2A5HR1). These circuits, which form a part of Frequency Standard Electronic Assembly 2A2A5, maintain the 5 mc crystal oven at a constant 85°C (185°F) temperature. The oven control circuit is used during all modes of operation. The following paragraphs describe the operation of this circuit in detail.

4-49. The frequency of oscillator Q1, Q2 is approximately 18 kc, as determined by the tuned circuit consisting of capacitor C2 and the primary of transformer T1. The feedback for oscillator Q1, Q2 is produced by a bridge consisting of the center-tapped secondary of transformer T1 acting as two of the bridge legs. Resistor 2A2A5R1 and thermistor 2A2A5RT1, thermistor RT2, resistor R18, resistor R7 act as the other two legs. This

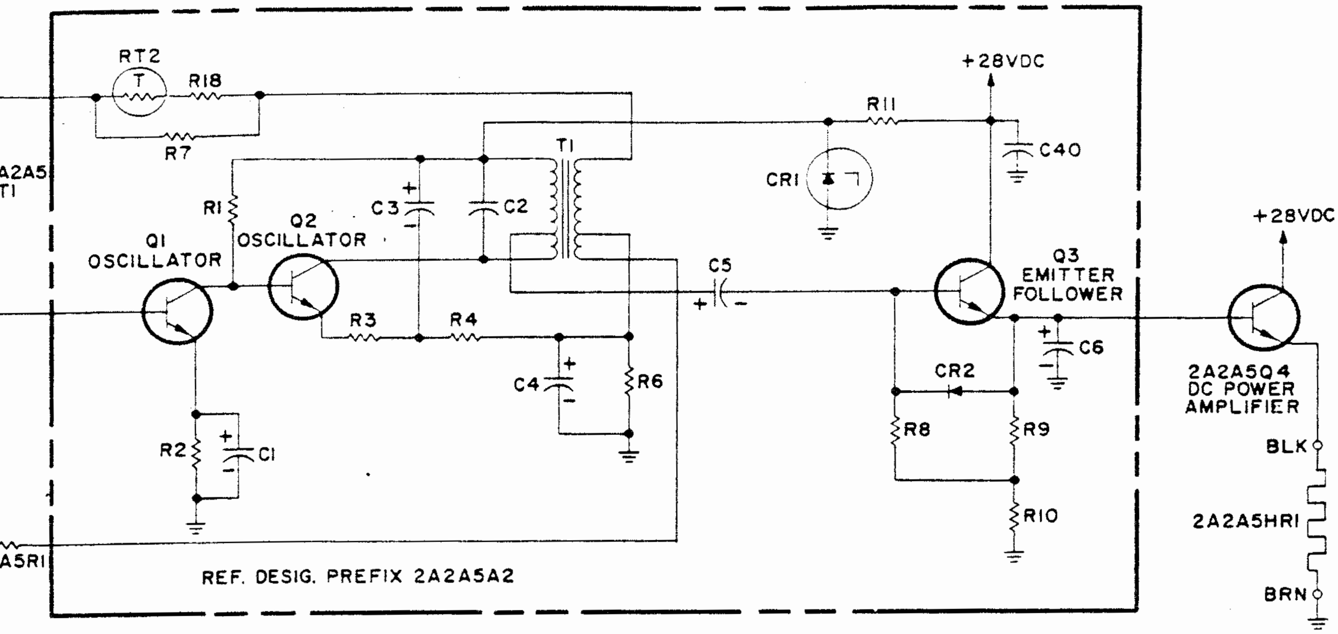

Figure 4-5. Oven Control, Simplified Schematic Diagram

: is designed to balance when thermistor
RT1 is at 85°C. Thermistor 2A2A5RT1
sically mounted underneath heater
HR1. The bridge will never become
ed due to heat lost to the surround-
therefore, the oscillator will never stop
iting. Emitter resistor R2 provides
as for oscillator Q1. Capacitor C1
ns as an emitter bypass capacitor.
r resistors R3, R4, and R6 provide
as for oscillator Q2. The dc bias is
ken from the junction of resistors R4
and applied through the secondary of
ormer T1 and resistor 2A2A5R1 to the
f oscillator Q1. Capacitors C3 and C4
itter bypass capacitors.

The 18-kc signal is taken from a tap on
mary of transformer T1 and coupled
h capacitor C5 to the base of emitter
r Q3, where it is rectified. Capacitor
oothes the rectified signal. Diode CR2
ts emitter follower Q3 against excessive
e-bias on the base-emitter junction.
he base voltage attempts to go more
e than the emitter voltage, diode CR2
forward-biased, thereby keeping the
oltage at the same level as the emitter
. From the emitter of emitter follower
e dc signal is applied to the base of dc
amplifier 2A2A5Q4 to control current
heater 2A2A5HR1 in the emitter circuit
ower amplifier 2A2A5Q4, and thereby,
perature of the oven. The current is
directly proportional to the unbalance caused in the bridge circuit, which determines the output signal amplitude of oscillator Q1, Q2.

4-51. Stable operating voltages for oscillator Q1,Q2 are provided by resistor R11 and zener diode CR1.

4-52. OVEN CONTROL, TEST DATA. Pertinent references and applicable test data for the oven control circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Frequency Standard Electronic Assembly, Servicing Block Diagram, Figure 4-71.

c. Frequency Standard Electronic Assembly, Schematic Diagram, Figure 5-9.

d. Required Test Equipment:

(1) Electronic Multimeter, CCVO-91CA.

(2) Multimeter, AN/PSM-4.

(3) Frequency Standard Test Set, TS-2134/WRC-1.

e. Oven Control and Buffer Amplifier, Component, Location, Figure 5-72.

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f. Refer to paragraph 2-27 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules NAVSHIPS 95700 for temperature adjustment procedure.

4-53. COMPARATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The comparator (figure 4-6) consists of a buffer amplifier (Q5), a comparator stage (Q7), and an amplifier (Q6). These circuits, which form a part of Frequency Standard Electronic Assembly 2A2A5, compare the 5.000000-mc signal received from the 5 mc frequency standard circuit with an accurate external 5-mc signal. This function is required to determine and maintain the accuracy of the internal 5 mc frequency standard signal. The following paragraphs describe the operation of this circuit in detail.

4-54. In the INT position of switch 2A2A5S1, the 5-mc signal from the 5 mc frequency standard is applied to buffer amplifier Q5 through 5 MC LEVEL ADJ potentiometer R22, contacts 2 and 4 of switch 2A2A5S1, and coupling capacitor C19. The amplified 5-mc signal output from this stage is applied to the 5-mc divide-by-five circuit through a portion of th primary winding of 5 MC ADJ transformer T With switch 2A2A5S1 in the INT position, the 5-mc signal is also applied to the 5 mc multiply-by-two circuit. Base-bias for buffer amplifier Q5 is provided by voltage divide R19, R21. Negative feedback to the emitte of buffer amplifier Q5 is provided by trans former coupling the 5-mc output through the center tapped primary winding of 5 MC ADJ transformer T5 and capacitor C18. This feedback provides frequency stabi for this amplification stage. No 5 mc signal applied to comparator Q7 and the subsequent amplifier Q6 when switch 2A2A5S1 is set at t INT position since contacts 7-8 of that switcl are open. Resistor R17 is the output load resistor for the 5 mc signal. Resistor R20 i the emitter resistor.

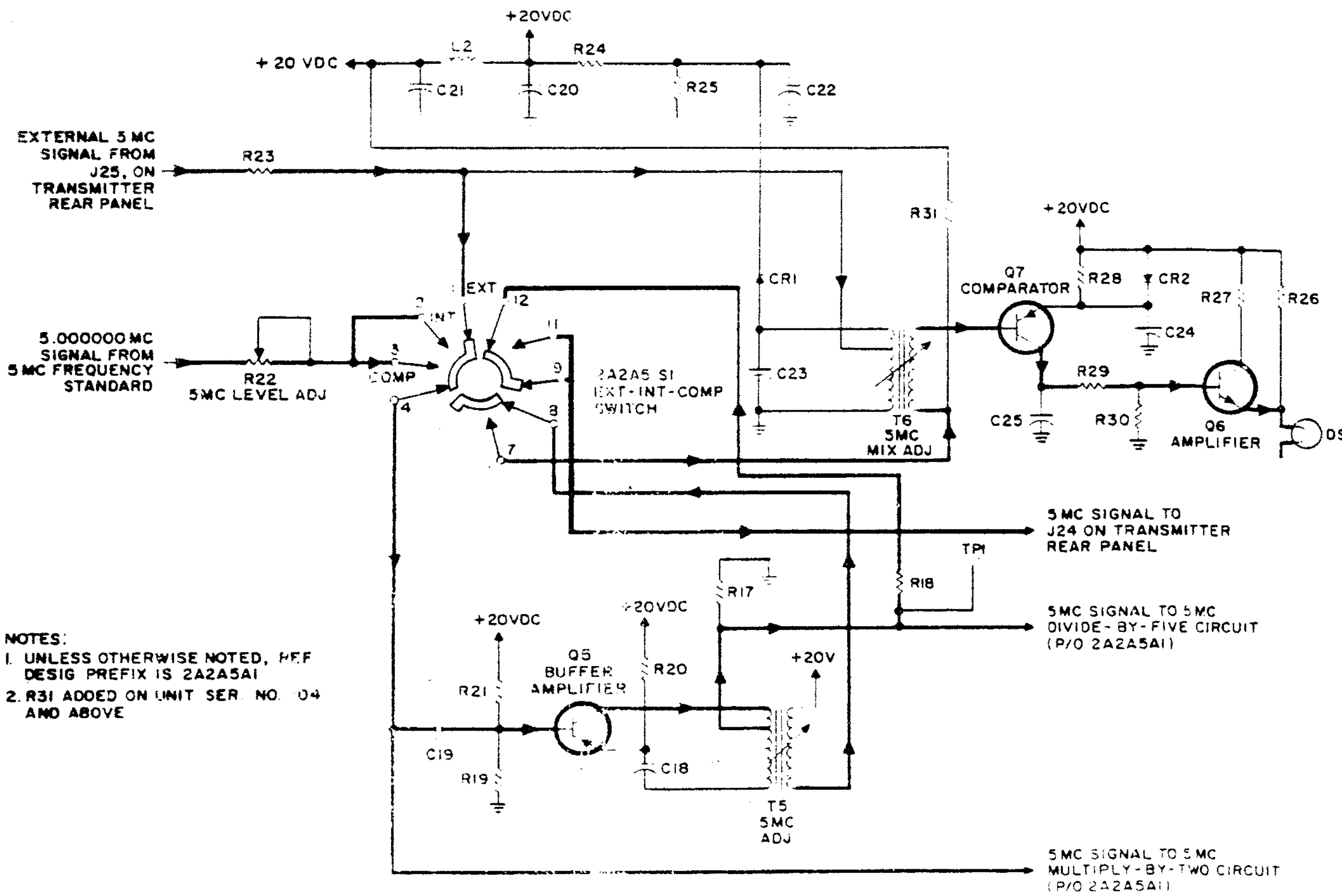

Figure 4-6. Comparator, Simplified Schematic Diagram

5. When switch 2A2A5S1 is in the EXT ition, the externally supplied 5-mc signal mplified by buffer amplifier Q5 and applied onnector J24 on the rear panel of the trans- ter and to the 5 mc divide-by-five circuits he same manner as described in paragraph 4. In a similar manner, the signal is ectly coupled to the 5 mc multiply-by-two cuit through contacts 1 and 4 of switch A5S1. Since contacts 7-8 are not closed, parator Q7 and its associated amplifier are not operative. The internally generated ic signal is compared with an externally plied 5-mc standard when switch 2A2A5S1 et at the COMP position. In this condition peration, the 5-mc external signal is lied to the primary winding of transformer from connector J25 on the rear panel of transmitter, through isolating resistor . Comparator Q7 and associated ampli- Q6 become operative since both the rnal and external 5 mc signal are avail- e to the circuit. The amplitude of the ernally applied signals is limited to roximately 300 millivolts peak by the age divider network consisting of istors R24, R25, and diode CR1. In the nt that the frequencies of the two signals different, the resulting difference fre- ncy is coupled to the base of comparator A portion of the output from comparator is dc coupled to the base of amplifier Q6 voltage divider-collector load resistors and R30. The output of amplifier Q6 is eloped across lamp DS1 in its emitter cuit, causing the lamp to flash at the erence frequency. Resistor R28 is the tter bias resistor, which is rf bypassed capacitor C24. Diode CR2 in the emitter cuit of comparator Q7 keeps the gain of stage constant in spite of temperature iations. This control occurs because the istance of diode CR2 varies with temp- ture change. Capacitor C25 bypasses all ing products except the difference fre- ncy to ground. Resistor R27 is the collector pping resistor for amplifier Q6. Resistor is a bleeder resistor for stablizing the escent emitter bias for dc amplifier Q6.

6. COMPARATOR, TEST DATA. Perti- t references and applicable test data for comparator circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Frequency Standard Electronic Assembly, Servicing Block Diagram, Figure 4-71.

c. Frequency Standard Electronic Assembly, Schematic Diagram, Figure 5-9.

d. Refer to paragraph 2-27 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for comparator adjustment procedures.

e. Required Test Equipment:

(1) Electronic Multimeter, CCVO-91CA.

(2) Multimeter, AN/PSM-4.

(3) RF Signal Generator, CAQI-606A.

(4) Frequency Standard Test Set, TS-2134/WRC-1.

f. 5 MC Multiplier, Dividers and Comparator, Component Location, Figure 5-71.

4-57. 5 MC DIVIDE-BY-FIVE, FUNCTIONAL CIRCUIT DESCRIPTION. The 5-mc divide-by-five circuit (figure 4-7) consists of a 4 mc amplifier (Q2) and a 1 mc amplifier (Q3). These circuits, which form a part of the multiplier-divider circuit group of Frequency Standard Electronic Assembly 2A2A5, derive a 1-mc signal for use in the spectrum generator mixer circuit of 1 MC Synthesizer Electronic Subassembly 2A2A6A1 from the 5-mc signal from the comparator circuit (Refer to paragraph 4-53.) The following paragraphs describe the operation of the circuits in detail.

4-58. Amplifiers Q2 and Q3 form a regenerative closed loop to provide a 1-mc output. At the instant power is applied, some circuit disturbance causes noise to be produced in the tuned outputs of amplifiers Q3 and Q2. The tuned output of amplifier Q3 allows only the 1-mc portion of the noise to pass. This

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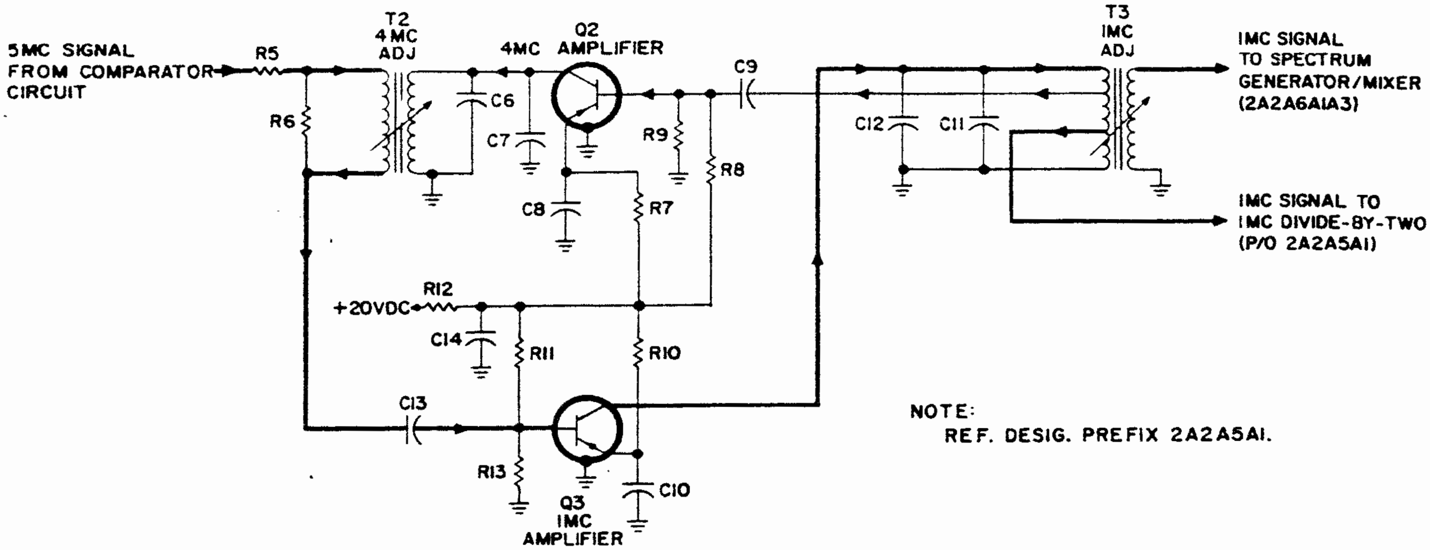


Figure 4-7. 5 MC Divide-by-Five, Simplified Schematic Diagram

low level 1-mc is applied to 4 mc amplifier Q2. Amplifier Q2 is biased in a non-linear condition so that the fourth harmonic of the 1-mc is amplified. The 4 mc is mixed with the 5-mc input, providing a 1-mc input to amplifier Q3. The 1 mc is amplified and applied to amplifier Q2. This flywheel effect is repeated until a stable 1-mc output is produced, which is locked to the 5 mc frequency standard.

4-59. The 5-mc signal, applied to the primary of transformer T2, is mixed with the 4-mc signal from the secondary, producing a 1-mc difference frequency. The 1-mc signal is coupled by capacitor C13 to the base of 1 mc amplifier Q3. The base bias for amplifier Q3 is provided by voltage divider R12, R11, R13. The output load for 1 mc amplifier Q3 consists of the primary of transformer T3 and capacitors C11 and C12. This output circuit is tuned to 1 mc. Capacitor C12 has a negative temperature coefficient to compensate for changes in the 1 mc amplifier caused by temperature changes. The 1-mc signal is taken from a tap on the primary of transformer T3 and coupled to the base of 4 mc amplifier Q2 by capacitor C9. Base bias for amplifier Q2 is provided by voltage divider R8, R9, R12. The output load for 4 mc amplifier Q2 consists of the primary of transformer T2 and capacitors C6 and C7. This output circuit is tuned to 4 mc. Capacitor C7 has a negative temperature coefficient to compensate for changes in the 4-mc amplifier output caused by temperature changes. Resistors R7 and R10 are emitter bias resistors, which are rf bypassed by capacitors C8 and C10, respectively. Resistor R12 and capacitor C14 provide decoupling for amplifiers Q2 and Q3. The two 1-mc outputs from the 5 mc divide-by-five circuits are taken from the primary and secondary of transformer T3 and applied to the 1 mc divide-by-two circuit and to the spectrum generator/mixer circuit in 1 MC Synthesizer Electronic Subassembly 2A2A6A1.

4-60. 5 MC DIVIDE-BY-FIVE, TEST DATA. Pertinent references and applicable test data for the 5 mc divide-by-five circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Frequency Standard Electronic Assembly, Servicing Block Diagram, Figure 4-71.

c. Frequency Standard Electronic Assembly, Schematic Diagram, Figure 5-9.

d. Refer to paragraph 2-25 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 5 mc divide-by-five alignment procedures.

e. Required Test Equipment:

(1) Electronic Multimeter, CCVO-91CA.

(2) Multimeter, AN/PSM-4.

(3) RF Signal Generator, CAQI-606A.

(4) Frequency Standard Test Set, S-2134/WRC-1.

f. Output Level:

g. 5 MC Multiplier, Divider and Comrator, Component Location, Figure 5-71.

-61. 1 MC DIVIDE-BY-TWO, FUNCTIONAL RCUIT DESCRIPTION. The 1 mc divide-by-o circuit produces a locked 500-kc signal from e locked 1-mc signal from the 5 mc divide-y-five circuit. The circuit consists of 500 amplifier Q1, in a regenerative oscillator onfiguration (figure 4-8) and forms a part of e multiplier-divider circuit group of Freuency Standard Electronic Assembly 2A2A5. he 500-kc signal is the local carrier used in e 500 kc if. amplifiers circuit 2A2A1A4 and iggers 100 kc spectrum generator circuit 2A6A5A1. The following paragraph deribes the operation of the 1 mc divide-by-two rcuit in detail.

-62. With no 1-mc input, the 1 mc divide-by-o circuit will not oscillate. When the 1-mc gnal is applied through isolating resistor R4, e feedback winding of transformer T1, and upling capacitor C4 and appears at the base 500 kc oscillator Q1, the transistor will be ased on. At this time, noise is produced due the transistor being turned on. Since transrmer T1 is tuned to 500 kc, the 500-kc poron of this noise passes through transformer T1 and mixes with the 1-mc signal producing a 500 kc difference frequency. This difference is amplified by 500 kc amplifier Q1 and again applied to transformer T1, thereby sustaining oscillations. Resistor R2 is the base bias resistor. Resistor R1 is the emitter resistor, which is rf bypassed by capacitor C1. Resistor R3 and capacitors C2 and C3 provide decoupling for 500 kc amplifier Q1. The 500 kc output is taken from the secondary of transformer T1 and applied to the 500 kc if. amplifiers circuit 2A2A1A4 and to the 100 kc spectrum generator circuit 2A2A6A5A1.

4-63. 1 MC DIVIDE-BY-TWO, TEST DATA. Pertinent references and applicable test data for the 1 mc divide-by-two circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Frequency Standard Electronic Assembly, Servicing Block Diagram, Figure 4-71.

c. Frequency Standard Electronic Assembly, Schematic Diagram, Figure 5-9.

d. Refer to paragraph 2-25 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 1 mc divide-by-two adjustment procedures.

e. Required Test Equipment:

(1) Electronic Multimeter, CCVO-91CA.

(2) Multimeter, AN/PSM-4.

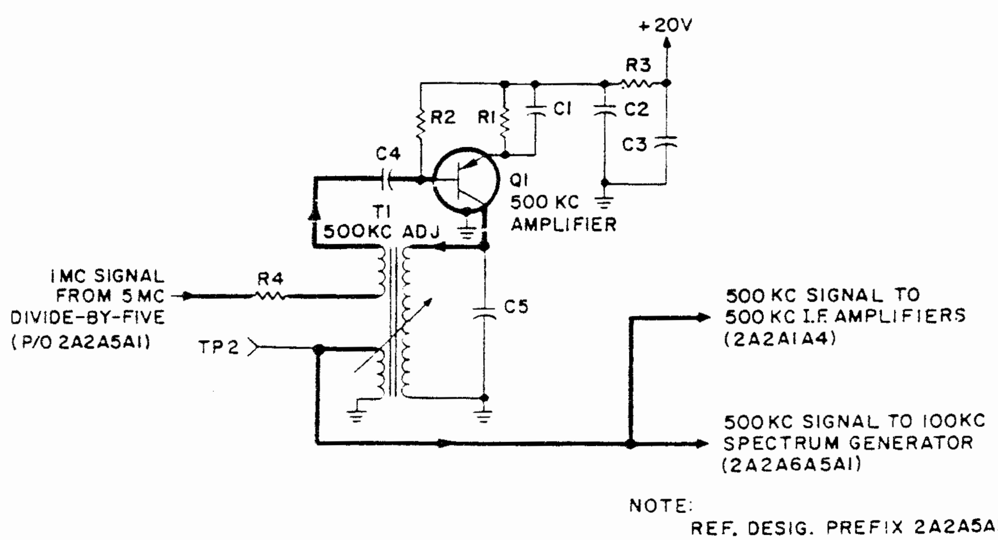


Figure 4-8. 1 MC Divide-By-Two, Simplified Schematic Diagram

(3) RF Signal Generator, CAQI-606A.

(4) Frequency Standard Test Set, TS-2134/WRC-1.

f. 5 MC Multiplier, Dividers and Comparator, Component and Test Point Location, Figure 5-71.

4-64. 500 KC AMPLIFIER, FUNCTIONAL CIRCUIT DESCRIPTION. The 500 kc amplifier (figure 4-9) consists of a diode gating circuit (CR11) and two amplifiers (Q6 and Q7). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, amplify the 500-kc output from the 1 mc divide-by-two circuit in Frequency Standard Electronic Assembly 2A2A5 to a level suitable for use in balanced modulators 2A2A1A1 and 2A2A1A2. The gating circuit prevents application of the 500-kc signal to the amplifiers during CW operation only. Amplifier Q6 is used during the USB, AM, and FSK modes of operation, and amplifier Q7 is used during the LSB mode of operation. Both amplifiers are used during the ISB mode of operation. The following paragraphs describe in detail the operation of these circuits for each indicated operation mode.

4-65. ISB Operation. The 500-kc signal is coupled to the anode of gating diode CR11 by capacitor C26. This gate is forward-biased result of the positive 18 vdc on the anode and the positive 10 vdc on the cathode. The two biases are instantaneous voltages, developed for all modes of operation except CW as a by voltage dividers R53, R54, and R55, R56. Positive 20 vdc is applied to the dividers from the front panel Mode Selector switch. When gate CR11 is conducting, both biases are approximately the same. The difference is the voltage drop caused by the forward resistance of the diode. Since gate CR11 is forward-biased, it will conduct, allowing the 500-kc signal to pass and be coupled by capacitors C27 and C30 to the bases of amplifiers Q6 and Q7, respectively. Operating voltage for amplifier Q6 is developed from the positive 20 vdc applied to voltage divider R57, R58 and emitter resistor R59 from the Mode Selector switch on the front panel. The amplified 500-kc output from amplifier Q6 is developed across the tuned tank circuit consisting of capacitor C28 and the primary of transformer T3. The 500-kc signal is coupled to balanced modulator 2A2A1A1 by transformer T3. Operating voltage for amplifier Q7 is developed from the positive 20 vdc applied to voltage

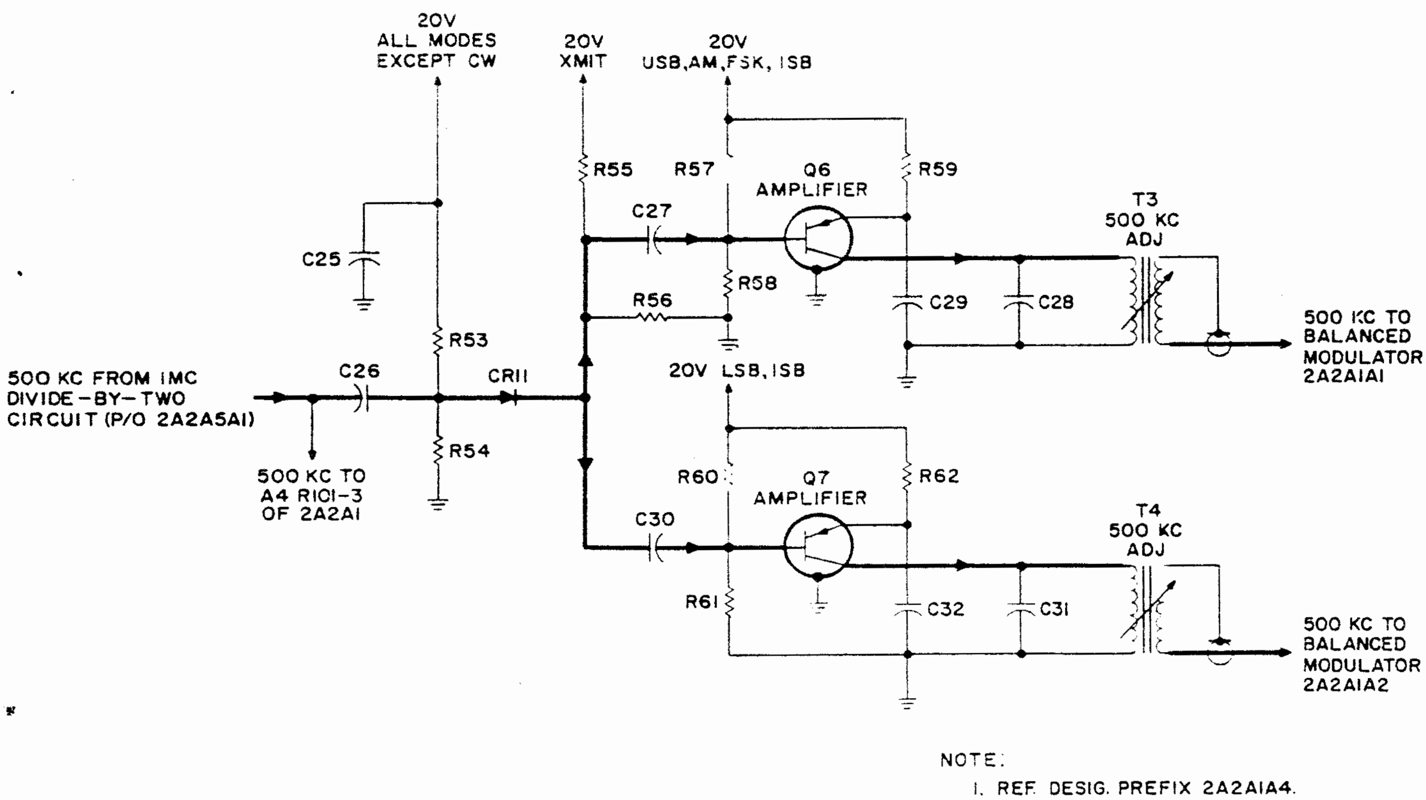


Figure 4-9. 500 KC Amplifiers, Simplified Schematic Diagram

vider R60, R61, and emitter resistor R62 ·om the Mode Selector switch on the front ınel. The amplified 500-kc output from am-ıifier Q7 is developed across the tuned tank ırcuit consisting of capacitor C31 and the ·imary of transformer T4. The 500-kc signal coupled to balanced modulator 2Z2A1A2 by ·ansformer T4.

66. USB, AM, FSK Operation. When the ode Selector switch on the front panel is set the USB, AM, or FSK position, the positive vdc operating voltage for Q7 is removed. ıe remaining circuits function as described paragraph 4-65.

67. LSB Operation. When the Mode Se-ːtor switch on the front panel is set at the ;B position, the positive 20 vdc operating ltage for amplifier Q6 is removed. The re-ıining circuits function as described in ragraph 4-65.

68. CW Operation. When the Mode Selector ·itch on the front panel is set at the CW posi-ın, the operating voltage for the amplifiers d the anode bias for gate CR11 is removed. .e 10 vdc cathode bias on CR11 is still ap-ed. Therefore, CR11 will be reverse-ısed.

69. 500 KC AMPLIFIER, TEST DATA. ·rtinent references and applicable test data ː the 500 kc amplifier circuit are as follows:

a. Radio Transmitter T-827/URT, Main ame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic sembly, Servicing Block Diagram, Figure 72.

c. Transmitter Mode Selector Electronic sembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic sembly, Adjustments, Paragraph 5-28.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1 and W7.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. 500 KC Amplifiers/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

4-70. BALANCED MODULATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The balanced modulator (figure 4-10) consists of a balanced resistive input network (R21, R22, R23, R24, R25), diode bridge (R27, CR5; R29, CR6; R28, CR7; R30, CR8), and a balanced reactive output network (C13, C14, C15, C16, C17, R31, R32, R33, R34, and the primary of T2). There are two balanced modulator circuits used; A1 and A2 (figure 5-6). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, modulate the 500-kc if. carrier with the desired intelligence. A balanced modulator is a device for obtaining the sideband components of modulation without passing the carrier. Balanced modulator A1 is used during the USB, AM, and FSK modes of operation. Balanced modulator A2 is used during the LSB mode of operation. Both balanced modulators are used during the ISB mode of operation. The following paragraphs describe the operation of the balanced modulator circuit in detail.

4-71. The 500-kc output from 500 kc amplifier A4Q6 is applied to the center of the balanced resistive input network. Balancing resistor R23 is adjusted to compensate for the tolerance of fixed resistors R21, R22, R24, and R25. Proper adjustment of resistor R23 insures that the resistance from the center to either side of the resistive input network will be equal (balanced). The output from this network is applied to one side of the diode bridge and the intelligence is applied to the other side. Each arm of the diode bridge has a 100-ohm precision resistor in series with the respective diode. Since the forward resistance of the diode is small, the resistance of each arm will be effectively 100 ohms, thereby balancing the bridge. The audio voltage across the bridge varies in frequency and amplitude. When the instantaneous polarity of the audio signal is positive, diode CR6 conducts; when the audio signal goes instantaneously negative, diode CR5 conducts. Therefore, the output from the diode bridge will consist of two sidebands with a suppressed carrier. The two sidebands are coupled to the primary of trans-

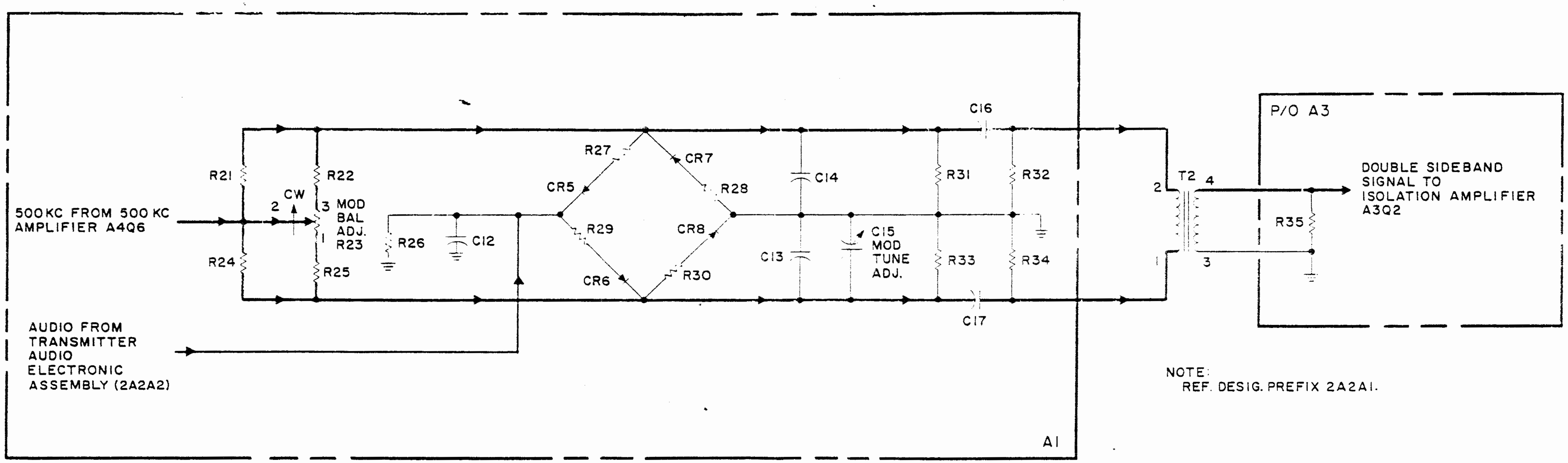


Figure 4-10. Balanced Modulator, Simplified Schematic Diagram

former T2 by capacitors C16 and C17. Resistors R31, R32, R33, and R34 provide resistive balance from the center to either side of the output of the balanced modulator circuit. Capacitors C13, C14, and C15 tune the primary of transformer T2. Balancing resistor R23 and tuning capacitor C15 provide resistive and reactive balance in the balanced modulator circuit, insuring a high degree of carrier suppression. Transformer T2 couples the double sideband signal to isolation amplifier A3Q2. Resistor A3R35 is the terminating resistor for transformer T2.

4-72. Balanced modulator A2 is identical to balanced modulator A1. The 500-kc signal is applied to balanced modulator A2 from 500 kc amplifier A4Q7. The output from balanced modulator A2 is developed across transformer T1, which also couples it to isolation amplifier A3Q1. Resistor A3R15 is a damping resistor for transformer T1.

4-73. BALANCED MODULATOR, TEST DATA. Pertinent references and applicable test data for the balanced modulators are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic Assembly, Adjustments, Paragraph 5-11.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Audio Signal Generator, AN/URM-127.

(3) Electronic Multimeter, CCVO-91CA.

(4) Analyzer Test Set, TS-1379/U.

(5) Cable Assembly, W1 and W7.

(6) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. Balanced Modulator, Component and Test Point Location, Figure 5-35.

g. Balanced Modulator, Component and Test Point Location, Figure 5-36.

h. Transmitter Mode Selector Electronic Assembly, Right Side View, Component and Test Point Location, Figure 5-33.

4-74. ISOLATION AMPLIFIER/FILTER, FUNCTIONAL CIRCUIT DESCRIPTION. The isolation amplifier/filter (figure 4-11) consists of an isolation amplifier (Q2) and a filter (FL2). A similar circuit (Q1 and FL1) is also used (figure 5-6). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, isolate the balanced

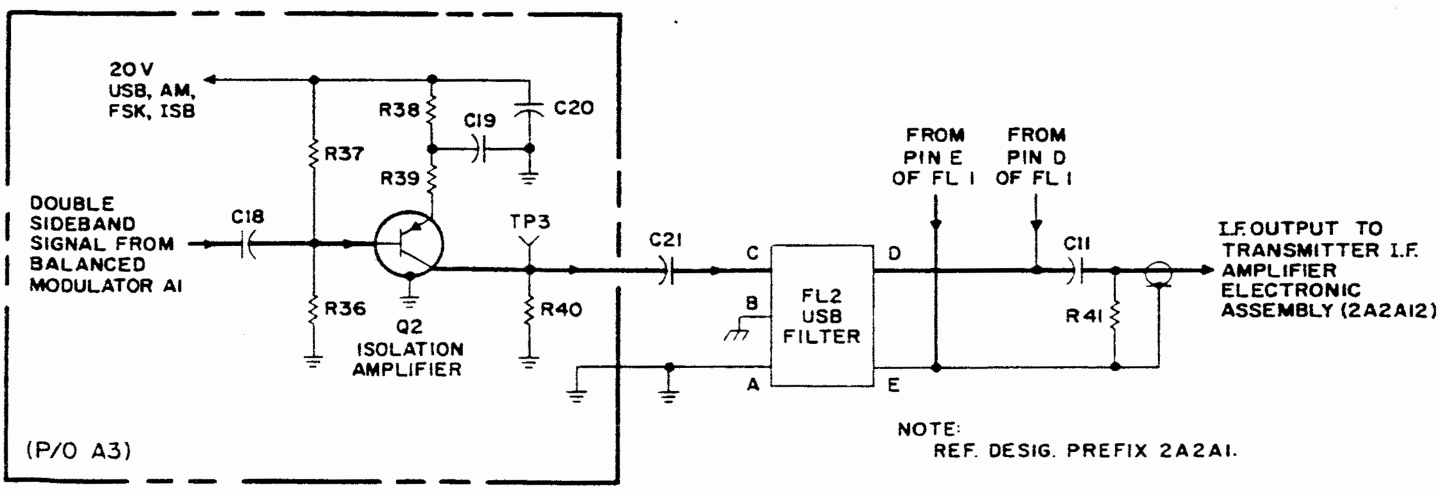


Figure 4-11. Isolation Amplifier/Filter, Simplified Schematic Diagram

modulator from the filter, provide amplification for the output of the balanced modulator, filter the undesired sideband from the double sideband output from the balanced modulator, and provide additional suppression of the 500-kc carrier. The carrier should be 50-db below the desired sideband at the output of the filter. Isolation amplifier Q2 and filter FL2 are used during the FSK, USB, and AM modes of operation. Isolation amplifier Q1 and filter FL1 are used during the LSB mode of operation. Both amplifiers and filters are used during the ISB mode of operation. The following paragraphs describe the operation of the isolation amplifier/filter circuit in detail.

4-75. The output from balanced modulator A1 is coupled to the base of isolation amplifier Q2 by capacitor C18. Operating voltage for amplifier Q2 is developed from the 20 vdc applied to voltage divider R36, R37 and emitter resistor R38 by the Mode Selector switch on the front panel (USB, ISB, AM, and FSK positions). Unbypassed emitter resistor R39 provides a small amount of degeneration to improve the stability of the circuit. Isolation amplifier Q2 provides amplification for the double sideband output from the balanced modulator. This amplification is required because of the insertion loss of the filter. The output from isolation amplifier Q2 is coupled to the input of filter FL2 by capacitor C21.

4-76. Filter FL2 is a mechanical filter that passes only the upper sideband portion of the double sideband output of isolation amplifier Q2. During FSK operation, the square wave used to modulate the 500-kc carrier is filtered so that only that portion of the if. that is modulated by the fundamental frequency of the square wave passes. Coupler capacitor C21 is selected to provide a 500-kc series resonant input circuit for the filter.

4-77. Isolation amplifier Q1 (figure 5-6) is identical to isolation amplifier Q2. The operating voltage for Q1 is only applied during LSB or ISB modes of operation. The 500-kc if. output from balanced modulator A2 is applied to isolation amplifier Q1, which provides the amplification required to drive filter FL1. Filter FL1 passes only the lower sideband portion of the double sideband output from isolation amplifier Q1. The output from filter FL1 or FL2, or from both filters, is coupled to the if. amplifiers in Transmitter IF. Amplifier Electronic assembly 2A2A12 by capacitor C11. Resistor R41 provides the necessary resistive termination for the two filters.

4-78. ISOLATION AMPLIFIER/FILTER, TEST DATA. Pertinent references and applicable test data for the isolation amplifier/filter circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Required Test Equipment.

(1) RF Signal Generator, CAQI-606A.

(2) Audio Signal Generator, AN/URM-127.

(3) Analyzer Test Set, TS-1379/U.

(4) Multimeter, AN/PSM-4.

(5) Cable Assembly, W1.

(6) Common Electronic Circuits Test Set, TS-2135/WRC-1.

e. Isolation Amplifiers, Component and Test Point Location, Figure 5-37.

f. Transmitter Mode Selector Electronic Assembly, Right Side View, Component and Test Point Location, Figure 5-33.

4-79. PEAK POWER CONTROLLED IF. AMPLIFIER, FUNCTIONAL CIRCUIT DESCRIPTION. The peak power controlled if. amplifier (figure 4-12) consists of an emitter follower (Q1) and an if. amplifier (Q2). These circuits, which form a part of Transmitter IF. Amplifier Electronic Assembly 2A2A12, prevent the peak power of the if. amplifier from exceeding a predetermined level and thereby limit the peak power of the AM-3007/URT. The following paragraphs describe the operation of this circuit in detail.

4-80. The if. signal from the isolation amplifier/filter circuit in Transmitter Mode Selector Electronic Assembly 2A2A1 is coupled through capacitor C1 to the base of if. amplifier Q2.

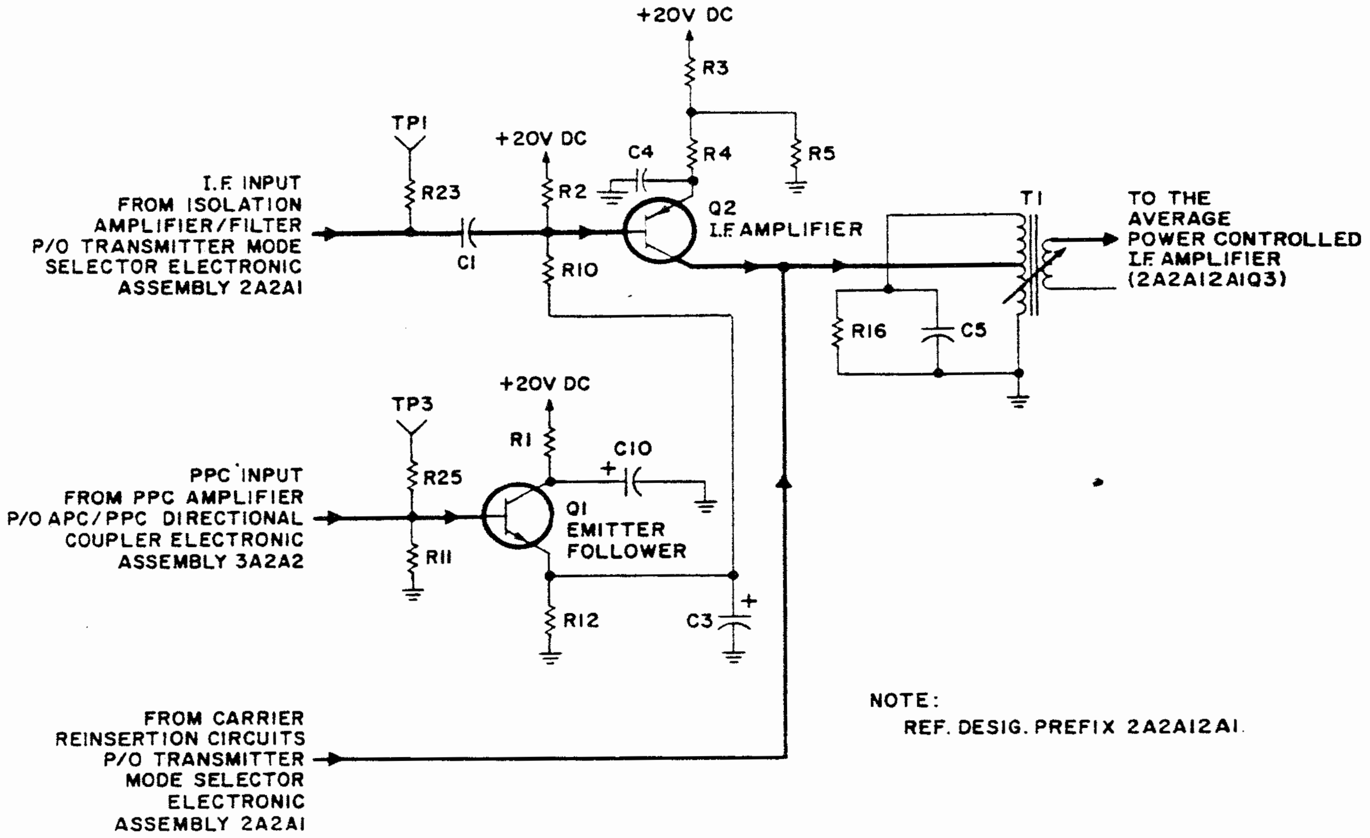


Figure 4-12. Peak Power Controlled IF. Amplifier, Simplified Schematic Diagram

The base bias for if. amplifier Q2 is provided by 20 vdc applied to voltage divider R2, R10, R12. Since resistor R12 is also in the emitter circuit of emitter follower Q1, any increase in the emitter current of emitter follower Q1 increases the voltage across resistor R12. This increases the base voltage on if. amplifier Q2, which decreases the forward bias from emitter to base of if. amplifier Q2, thereby decreasing the gain of the stage. Emitter current in emitter follower Q1 will flow when the final power amplifier V2 in the AM-3007/URT draws grid current. This produces a PPC output from the AM-3007/URT consisting of voltage pulses which are representative of final power amplifier V2 grid current. These pulses are applied to the base of emitter follower Q1, forward-biasing it and causing emitter current pulses to charge capacitor C3. This action raises the voltage level on the base of if. amplifier Q2, decreasing its forward bias, and therefore the gain of the stage. The output from if. amplifier Q2 is developed across a 500-kc tuned circuit consisting of the primary of transformer T1 and capacitor C5.

4-81. When the T-827/URT is operating in the compatible AM or CW mode, a 500-kc carrier signal from the carrier re-insertion circuits in Transmitter Mode Selector Electronic Assembly 2A2A1 is re-inserted into the if. signal at the collector of if. amplifier Q2. The pilot carrier, when used, is also applied to the collector of if. amplifier Q2 for re-insertion.

4-82. PEAK POWER CONTROLLED IF. AMPLIFIER, TEST DATA. Pertinent references and applicable test data for the peak power controlled if. amplifier circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter IF. Amplifier Electronic Assembly, Servicing Block Diagram, Figure 4-73.

c. Transmitter IF. Amplifier Electronic Assembly, Schematic Diagram, Figure 5-18.

d. Transmitter IF. Amplifier Electronic Assembly 2A2A12, Adjustments, Paragraph 5-22.

e. Required Test Equipment:

(1) Multimeter, AN/PSM-4.

(2) Electronic Multimeter, CCVO-91CA.

(3) Cable Assembly, W2.

(4) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. Transmitter IF. Amplifier, Component and Test Point Location, Figure 5-114.

4-83. AVERAGE POWER CONTROLLED IF. AMPLIFIER, FUNCTIONAL CIRCUIT DESCRIPTION. The average power controlled if. amplifier (figure 4-13) consists of emitter follower (Q4) and an if. amplifier (Q3). These circuits, which form a part of Transmitter IF. Amplifier Electronic Assembly 2A2A12, control the amplitude of the 500-kc if. signal in accordance with the average power of the output signal of RF Amplifier AM-3007/URT. The following paragraphs describe the operation of this circuit in detail.

4-84. The if. signal from peak power controlled if. amplifier Q2 is applied to the base of if. amplifier Q3 through transformer T1. The base bias for if. amplifier Q2 is provided by 20 vdc applied to voltage divider R6, R15, R13, R17. The bias may be manually adjusted with potentiometer R15. The APC input signal is a dc level which is dependent upon the average power output from the AM-3007/URT. This level, applied to the base of emitter follower Q4, will forward-bias the is a d-c level which is dependent upon the average power output from RF Amplifier AM-3007/URT. This level, applied to the base of emitter follower Q4, will forward-bias the transistor, causing emitter current to flow through resistor R14. The APC input signal will not affect if. amplifier Q3 until the magnitude of the signal is sufficient to cause enough emitter current to flow through resistor R14

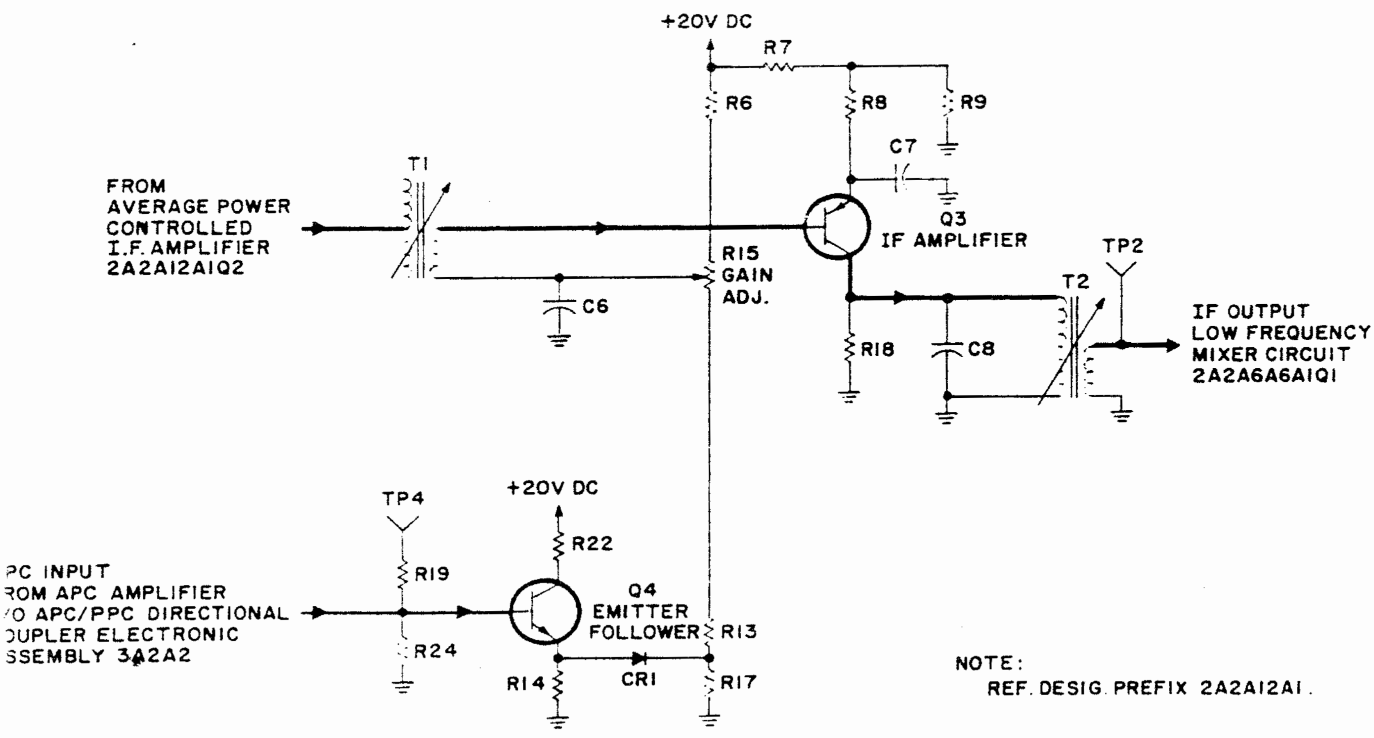


Figure 4-13. Average Power Controlled IF. Amplifier, Simplified Schematic Diagram

so that the voltage across resistor R14 will exceed the voltage across resistor R17. This condition will forward-bias diode CR1, causing the voltage across resistor R17 to rise to nearly the same level as the voltage across resistor R14. Raising the voltage across resistor R17 causes the base bias voltage on if. amplifier Q3 to rise, thereby reducing the base-to-emitter forward bias, resulting in a decrease in gain for the stage. The output from if. amplifier Q3 is developed across the 500-kc tuned circuit consisting of the primary of transformer T2 and capacitor C8.

4-85. AVERAGE POWER CONTROLLED IF. AMPLIFIER, TEST DATA. Pertinent references and applicable test data for the average power controlled if. amplifier circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter IF. Amplifier Electronic Assembly, Servicing Block Diagram, Figure 4-73.

c. Transmitter IF. Amplifier Electronic Assembly, Schematic Diagram, Figure 5-18.

d. Transmitter IF. Amplifier Electronic Assembly 2A2A12, Adjustment, Paragraph 5-22.

e. Required Test Equipment:

(1) Multimeter, AN/PSM-4.

(2) Electronic Multimeter, CCVO-91CA.

(3) Cable Assembly, W2.

(4) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. Transmitter IF. Amplifier, Component and Test Point Location, Figure 5-114.

4-86. LOW FREQUENCY MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The low frequency mixer (figure 4-14) consists of the first transmitter mixer (Q5) and an emitter follower (Q7). These circuits, which form a part of RF Translator Electronic Subassembly 2A2A6A6 mix the 500-kc if. signal from the average power controlled if. amplifier in Transmitter IF. Amplifier Electronic Assembly 2A2A12 with the 1 and 10-kc injection from 1 and 10 kc output and blanker circuit

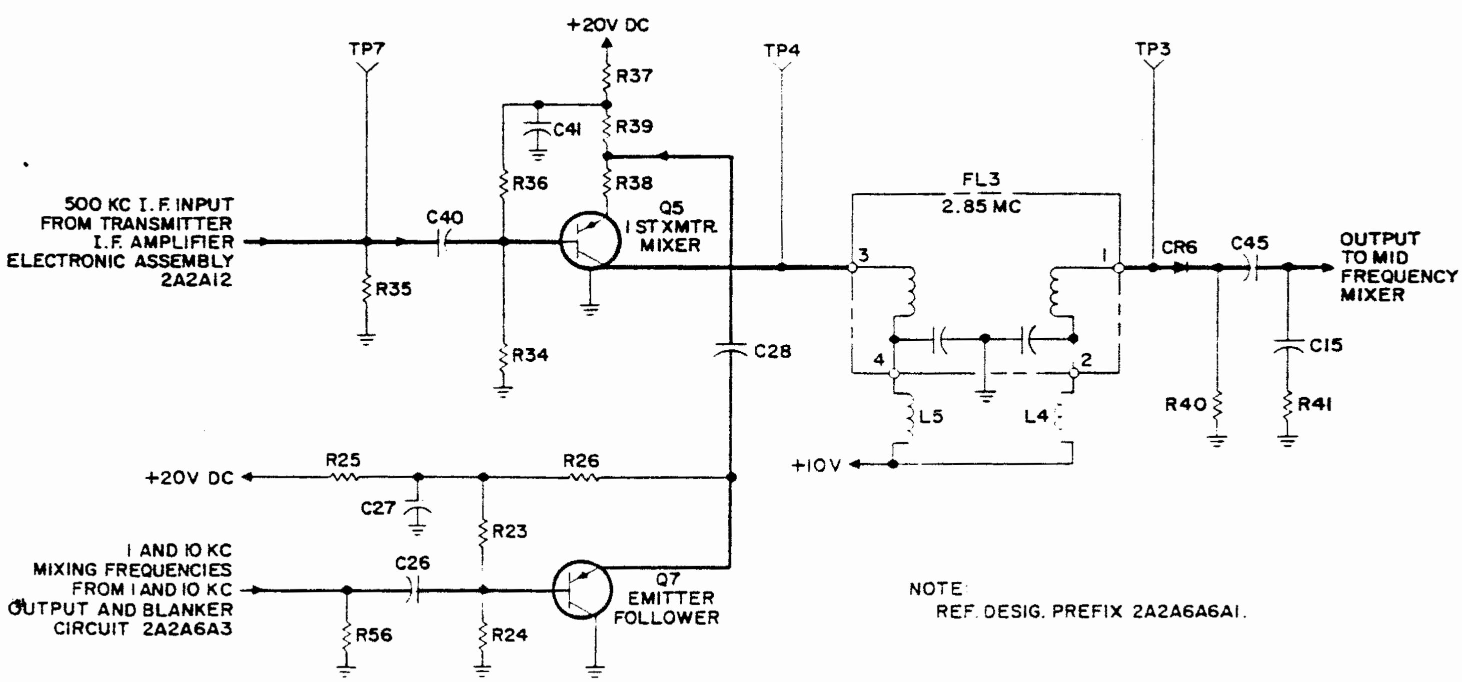


Figure 4-14. Low Frequency Mixer, Simplified Schematic Diagram

2A2A6A3A3, producing a second if. frequency between 2.8 and 2.9 mc. The following paragraphs describe the operation of this circuit in detail.

4-87. The 1 and 10-kc injection signal is coupled through capacitor C26 to the base of emitter follower Q7. The base bias for emitter follower Q7 is produced from the 20 vdc applied to voltage divider R25, R23, R24. The emitter follower isolates the 1 and 10 kc output and blanker circuit from first transmitter mixer Q5 and provides a low impedance source to the emitter circuit of the mixer. The 1 and 10-injection signal covers the range of 3.301 to 3.400 mc in 1 kc steps. The output from emitter follower Q7 is coupled through capacitor C28 and resistor R38 to the emitter of first transmitter mixer Q5. The 500-kc if. input signal is coupled through capacitor C40 to the base of first transmitter mixer Q5. The base bias for first transmitter mixer Q5 is provided by 20 vdc applied to voltage divider R34, R36, R37. Filter FL3, which has a bandwidth from 2.8 to 2.9 mc, is in the output circuit of first transmitter mixer Q5. This filter will reject all the products from the mixer except the desired difference frequency. Inductors L4 and L5 decouple the 10-vdc line. Diode CR6 is forward-biased through resistor R40, inductor L4, and filter FL3. The output from filter FL3 passes through diode CR6 and is coupled through capacitor C45 to the mid frequency mixer circuit. Resistor R41 supplies the a-c load required for filter FL3. Capacitor C15 dc isolates resistor R41.

4-88. LOW FREQUENCY MIXER, TEST DATA. Pertinent references and applicable test data for the low frequency mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. RF Translator Electronic Subassembly, Servicing Block Diagram, Figure 4-74.

c. RF Translator Electronic Subassembly, Schematic Diagram, Figure 5-15.

d. RF Translator, Component and Test Point Location, Figure 5-110.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Translator/Synthesizer Test Set, TS-2134/WRC-1.

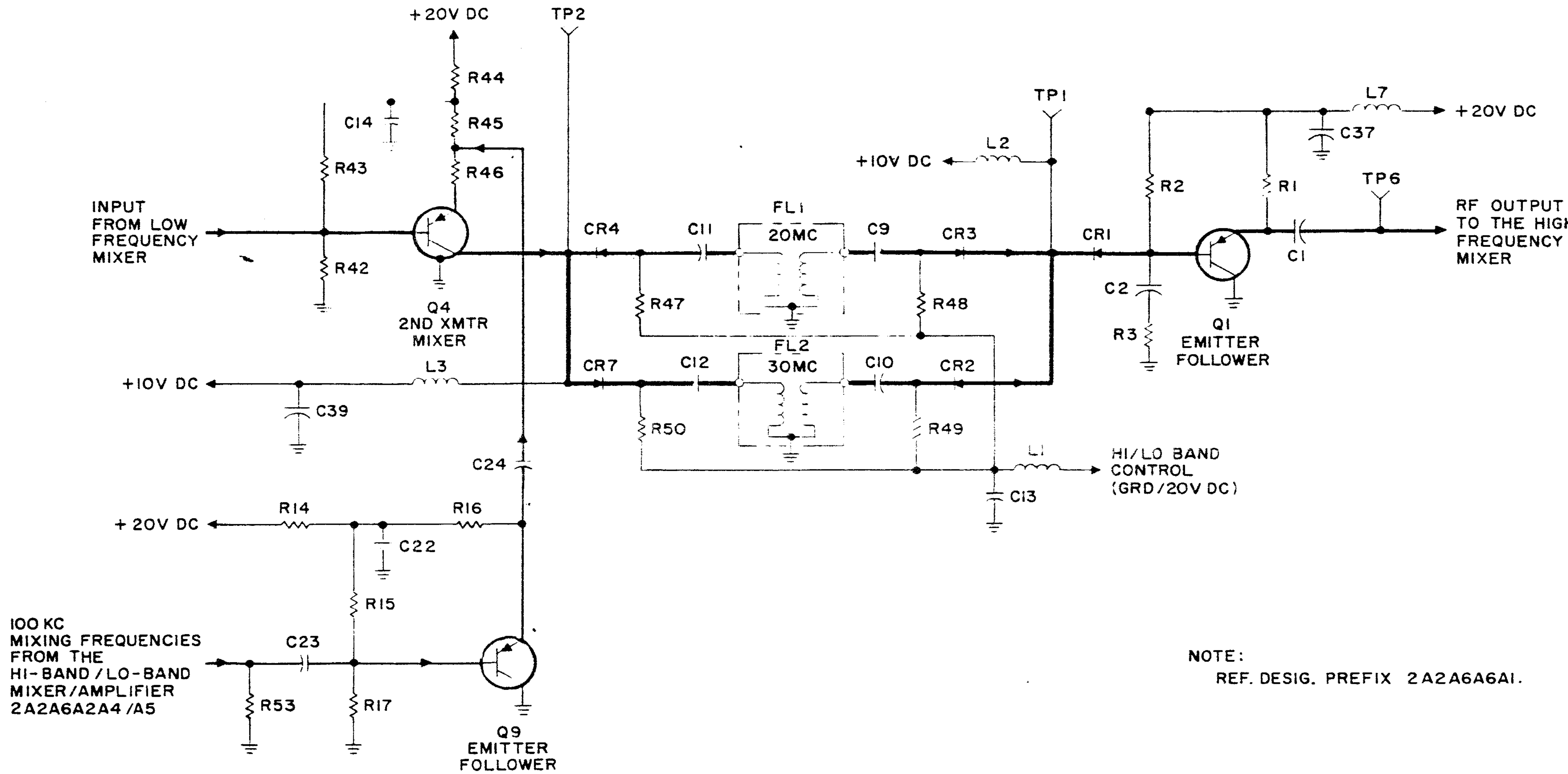
(3) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(4) Multimeter, AN/PSM-4.

f. Refer to paragraph 3-36 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for low frequency mixer adjustment procedures.

4-89. MID FREQUENCY MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The mid frequency mixer (figure 4-15) consists of the second transmitter mixer (Q4) and two emitter followers (Q1 and Q9). These circuits, which form a part of RF Translator Electronic Subassembly 2A2A6A6, mix the signal from the low frequency mixer with the 100-kc injection from hi-band/lo-band mixer/amplifier in 100 KC Synthesizer Electronic Subassembly 2A2A6A2. The following paragraphs describe the operation of this circuit in detail.

4-90. The 100-kc mixing frequencies signal is coupled by capacitor C23 to the base of emitter follower Q9. The base bias for emitter follower Q9 is provided by 20 vdc applied to voltage divider R14, R15, R17. The emitter follower isolates the hi-band/lo-band mixer/amplifier circuit from second transmitter mixer Q4 and provides a low impedance source to the mixer. The frequency of the 100-kc mixing frequencies signal is in 100-kc steps between 22.4 to 23.3 mc or 32.4 to 33.3 mc, depending on the potential on the hi/lo band control line. The output from emitter follower Q9 is coupled through capacitor C24 and resistor R46 to the emitter of second transmitter mixer Q4. The input from the low frequency mixer (2.8 to 2.9 mc) is applied to the base of second transmitter mixer Q4. The base bias for second transmitter mixer Q4 is provided by 20 vdc applied to voltage divider R44, R43, R42. The output circuit of second transmitter mixer Q4 consists of 20 mc filter FL1 and 30 mc filter FL2; each has a bandwidth of 1 mc (19.5 to 20.5 mc and 29.5 to 30.5 mc, respectively). When the hi/lo band control line is at ground potential (as determined by the code generator), diode CR7 is forward-biased by the 10 vdc applied through inductor L3 and resistor R50. Diode CR2 is also forward-biased by 10 vdc applied through inductor L2 and resistor R49. In this condition, the output from the second transmitter



NOTE:
REF. DESIG. PREFIX 2A2A6A6A1.

Figure 4-15. Mid Frequency Mixer, Simplified Schematic Diagram mixer is coupled through capacitor C12 to 30 mc filter FL2, where all mixing products except the desired difference frequency are rejected. The output from 30 mc filter FL2 is coupled through capacitor C10 to the base of emitter follower Q1 since diode CR1 is forward-biased by 20 vdc applied through resistor R2 and inductor L2. When the hi/lo band control line is at 20 vdc, diode CR4 is forward-biased by 20 vdc applied through inductor L1 and resistor R47. Diode CR3 is also forward-biased by 20 vdc applied through inductor L1 and resistor R48. In this condition, the output from the second transmitter mixer is coupled through capacitor C11 to 20 mc filter FL1, where all mixing products except the desired difference frequency are rejected. The output from 20 mc filter FL1 is coupled through capacitor C9 to the base of emitter follower Q1 since diode CR1 is forward-biased by 20 vdc applied through resistor R2. Resistor R3 supplies the ac load that is required by filters FL1 and FL2. Capacitor C2 dc isolates resistor R3. The output from emitter follower Q1 is coupled through capacitor C1 to the high frequency mixer in RF Amplifier Electronic Assembly 2A2A4.

4-91. MID FREQUENCY MIXER TEST DATA. Pertinent references and applicable test data for the mid frequency mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. RF Translator Electronic Subassembly Servicing Block Diagram, Figure 4-74.

c. RF Translator Electronic Subassembly Schematic Diagram, Figure 5-15.

d. RF Translator, Component and Test Point Location, Figure 5-39.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Translator/Synthesizer Test Set, TS-2134/WRC-1.

(3) Multimeter, AN/PSM-4.

4-92. HIGH FREQUENCY MIXER/AMPLIFIER, FUNCTIONAL DESCRIPTION. The high frequency mixer/amplifier (figure 4-16) consists of an amplifier (2A2A4A38Q1), a mixer (2A2A4A38Q2), and an emitter follower (2A2A6A6A1Q8). These circuits, which form a part of RF Amplifier Electronic Assembly 2A2A4 and RF Translator Electronic Sub-Assembly 2A2A6A6, mix the signal from the mid frequency mixer circuit with the mc injection from the mc oscillator circuit in 1 MC Synthesizer Electronic Subassembly 2A2A6A1. The following paragraphs describe the operation of this circuit in detail.

4-93. The reference designator prefix for the components named in this paragraph is 2A2A6A6A1, unless otherwise noted. The mc mixing frequencies signal is coupled through capacitor C21 to the base of emitter follower Q8. Resistor R55 is the load for the mc mixing frequencies. Base bias is provided by 20 vdc applied to voltage divider R10, R11, R13. The emitter follower isolates the mc oscillator circuit (2A2A6A1A1) from mixer 2A2A4A38Q2 and provides a low impedance source for the emitter circuit of the mixer. The mc mixing frequencies signal consists of a frequency in the 2.5 to 23.5-mc range. The output from emitter follower Q8 is coupled through capacitors C7 and 2A2A4A38C4 to the base of mixer 2A2A4A38Q2.

4-94. The reference designator prefix for the components named in this paragraph is 2A2A4A38, unless otherwise noted. The input signal from the mid frequency mixer circuit is coupled to the base of amplifier Q1 by capacitor C1. Base bias is provided by 20 vdc applied to voltage divider R2, R3. The output from amplifier Q1 is coupled to the base of mixer Q2 by capacitor C3. The mc injection signal and the signal from amplifier Q1 are subtractively mixed and applied to the rf amplifier V1 circuit. The base bias is provided by 20 vdc applied to voltage divider R7, R8.

4-95. HIGH FREQUENCY MIXER, TEST DATA. Pertinent references for the high frequency mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. RF Amplifier Electronic Assembly, Servicing Block Diagram, Figure 4-75.

c. RF Translator Electronic Subassembly, Servicing Block Diagram, Figure 4-74.

d. RF Amplifier Electronic Assembly, Schematic Diagram, Figure 5-8.

e. RF Translator Electronic Subassembly,

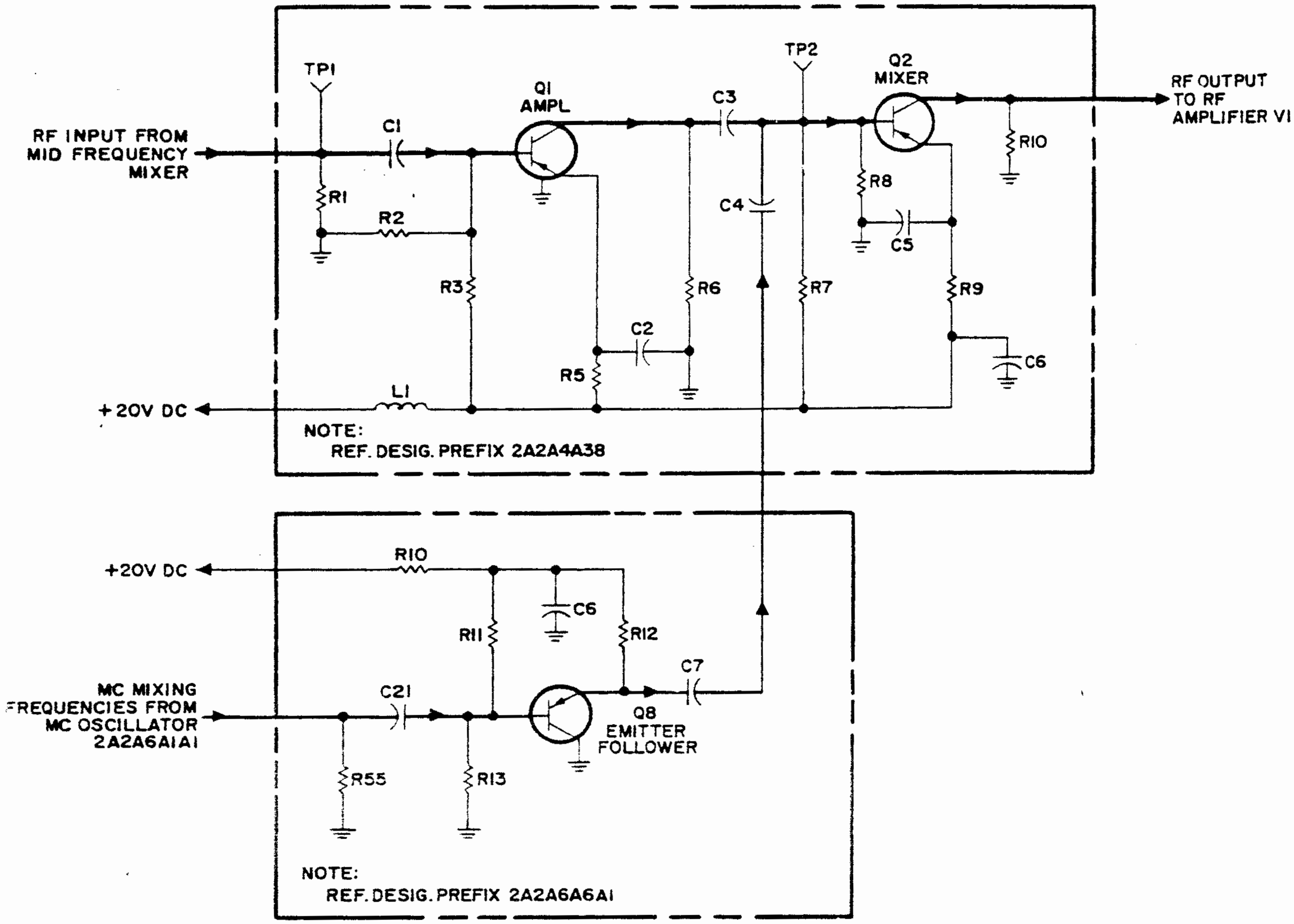


Figure 4-16. High Frequency Mixer, Simplified Schematic Diagram

Schematic Diagram, Figure 5-15.

f. High Frequency Mixer/Amplifier, Component and Test Point Location, Figure 5-74.

g. RF Translator, Component and Test Point Location, Figure 5-39.

h. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Translator/Synthesizer Test Set, TS-2134/WRC-1.

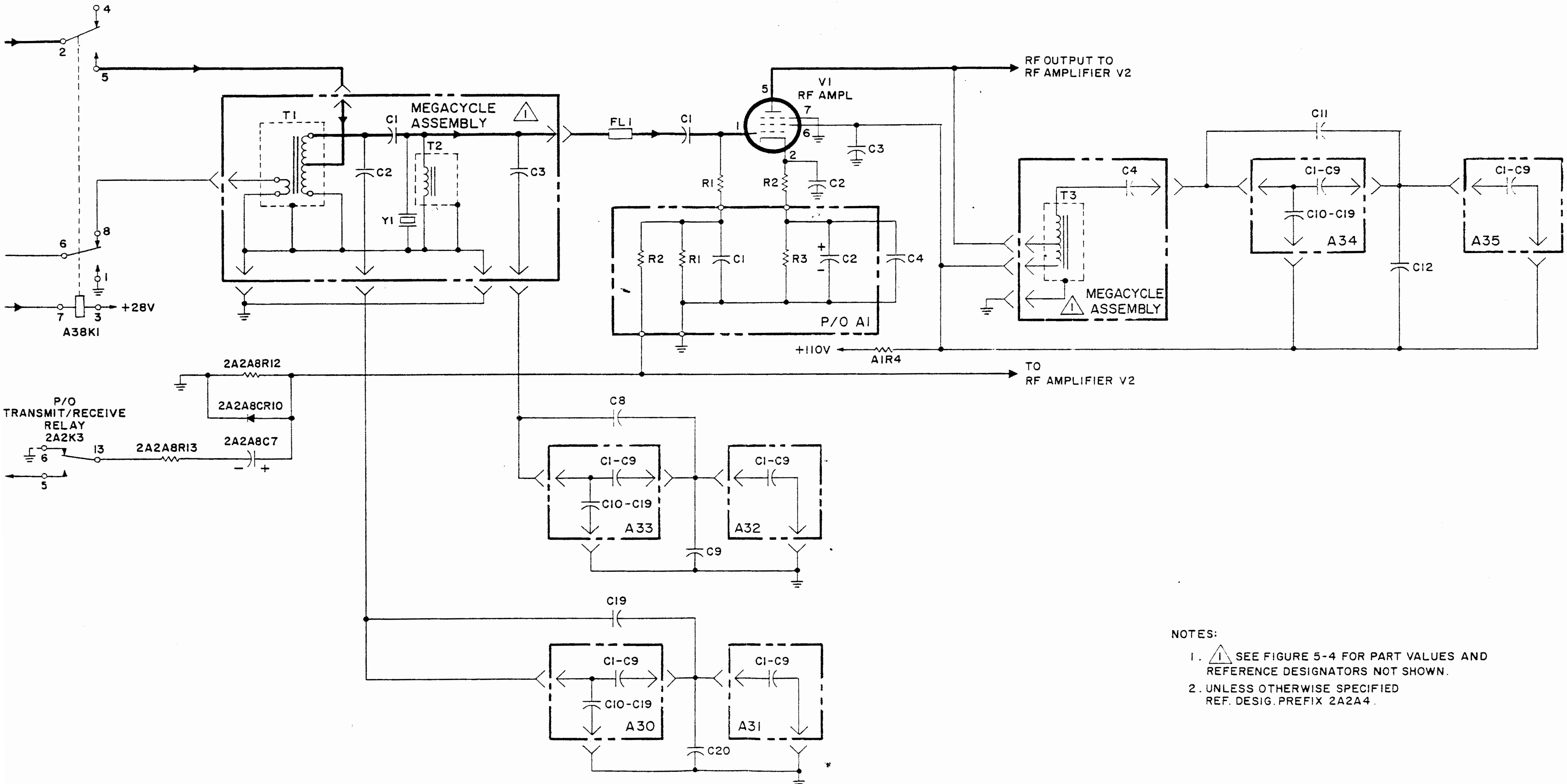
(3) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(4) Multimeter, AN/PSM-4.

i. Refer to paragraph 3-36 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for high frequency mixer adjustment procedures.

4-96. RF AMPLIFIER V1, FUNCTION CIRCUIT DESCRIPTION. RF Amplifier V1 (figure 4-17), which forms a part of RF Amplifier Electronic Assembly 2A2A4, amplifies the rf signal from the high frequency mixer/amplifier circuit for application to rf amplifier V2. The following paragraphs describe the operation of this circuit in detail.

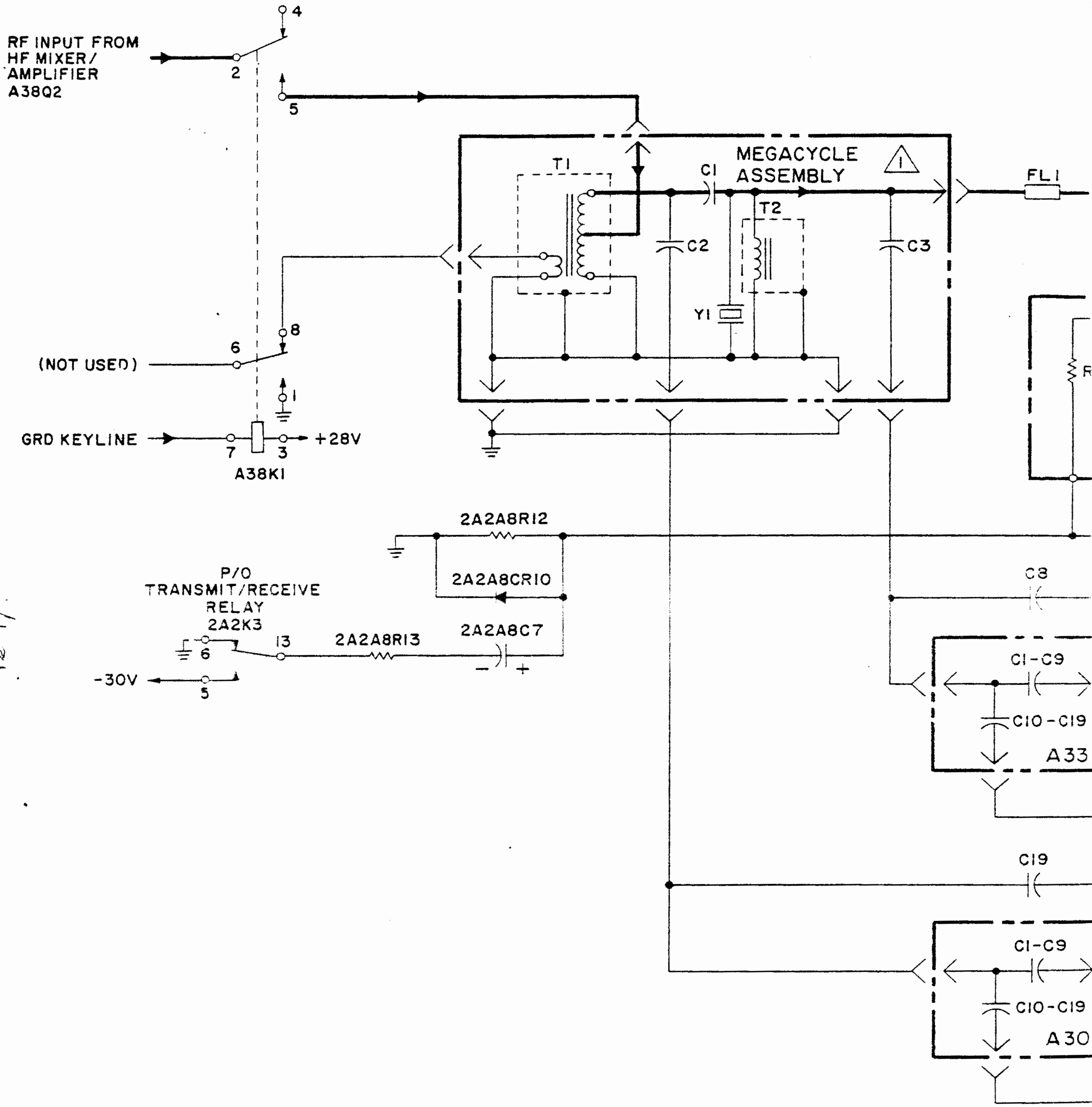
4-97. The signal from the high frequency mixer/amplifier circuit passes through contacts 2 and 5 of relay A38K1 and is applied to the secondary of transformer T1 in the megacycle assembly. The megacycle assembly is made up of a double-tuned circuit with capacity coupling. The secondary of transformer T1 forms part of a parallel tuned circuit. The other part consists of capacitor C2 in series with a capacitance network composed of



NOTES:

1. ⚠1 SEE FIGURE 5-4 FOR PART VALUES AND REFERENCE DESIGNATORS NOT SHOWN.
2. UNLESS OTHERWISE SPECIFIED REF. DESIG. PREFIX 2A2A4.

Figure 4-17. RF Amplifier V1, Simplified Schematic Diagram


RF INPUT FROM
HF MIXER/
AMPLIFIER
A38Q2
(NOT USED)
GRD KEYLINE
+28V
A38K1
MEGACYCLE
ASSEMBLY
T1
C1
C2
C3
T2
Y1
FL1
2A2A8R12
2A2A8CR10
P/O
TRANSMIT/RECEIVE
RELAY
2A2K3
2A2A8R13
2A2A8C7
-30V
C8
C1-C9
C10-C19
A33
C19
C1-C9
C10-C19
A30

capacitors C19 and C20 and the capacitors on circuit board assemblies A30 and A31. The signal is coupled from transformer T1 to inductor T2 by capacitor C1. Inductor T2 forms part of a parallel tuned circuit. The other part consists of capacitor C3 in series with a capacitance network composed of capacitors C8 and C9 and the capacitors on circuit board assemblies A32 and A33.

4-98. A separate megacycle assembly (A2 through A29) is automatically switched into the circuit for each setting of the front panel MCS controls (2 through 29 mc). The values of the components of these assemblies are shown in chart C on figure 5-8. For each of the ten settings of the 100 kc (KCS) control, different combinations of capacitors on the A30 and A33 assemblies (C1 through C9 and C10 through C19, respectively) are switched into the circuit. The values of these components are shown in chart B on figure 5-8. Also, for each of the ten settings of the 10 kc (KCS) control, different capacitors on assemblies A31 and A32 (C1 through C9) are switched into the circuit. The values of these components are shown in chart A on figure 5-8.

4-99. From the megacycle assembly, the signal passes through parasitic suppressor FL1 and is coupled through capacitor C1 to the control grid of rf amplifier V1. Screen voltage (110 vdc) for rf amplifier V1 is applied through decoupling resistor A1R4. Plate voltage (110 vdc) for rf amplifier V1 is applied through decoupling resistor A1R4 and transformer T3. The cathode bias for rf amplifier V1 is developed across resistors R2 and A1R3.

4-100. The output circuit for rf amplifier V1 consists of inductor T3 and capacitor C4 in series with a capacitance network comprised of capacitors C11 and C12 and the capacitors on circuit board assemblies A34 and A35. These components form a parallel tuned circuit. See paragraph 4-96 for a discussion of this tuned circuit, except note that the 100 kc capacitors are located on assembly A34 and the 10 kc capacitors are located on assembly A35.

4-101. When transmit/receive relay 2A2K3 is de-energized (receive mode), the negative lead of capacitor 2A2A8C7 is connected through resistor 2A2A8R13 and through contacts 13 and 6 of the relay to ground. When transmit/receive relay 2A2K3 is energized (transmit mode), the negative lead of capacitor 2A2A8C7 is connected through resistor 2A2A8R13 and through contacts 13 and 5 of the relay to -30 vdc. At the instant of energizing, capacitor 2A2A8C7 will present a short circuit (due to the fact there was no previous charge); therefore, the -30 vdc will be applied through voltage divider A1R1, A1R2 and resistor R1 to the grid of rf amplifier V1, which cuts off the stage. As the charge on capacitor 2A2A8C7 builds up through resistors 2A2A8R12 and 2A2A8R13, the dc voltage on the grid of rf amplifier V1 will approach zero, thereby permitting the stage to function. The reason for this action is that the controlled build up of excitation to the AM-3007/URT matches the response time of the system feedback loop controlling transmitted power and thereby prevents large bursts of output at the first instant of transmit operation.

4-102. The signal, after being amplified by rf amplifier V1, is applied to the second rf amplifier V2 circuit.

4-103. RF AMPLIFIER V1, TEST DATA. Pertinent references and applicable test data for rf amplifier V1 are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. RF Amplifier Electronic Assembly, Servicing Block Diagram, Figure 4-75.

c. RF Amplifier Electronic Assembly, Schematic Diagram, Figure 5-8.

d. RF Amplifier Bias Circuit Board, Component Location, Figure 5-45.

e. Megacycle Assemblies (2A2A4A2 through 2A2A4A29), Component Location, Figures 5-47 through 5-62.

f. 100 KC Rotor Assembly 2A2A4A30, Component Location, Figure 5-66.

g. 10 KC Rotor Assembly 2A2A4A31, Component Location, Figure 5-64.

h. 10 KC Rotor Assembly 2A2A4A32, Component Location, Figure 5-64.

i. 100 KC Rotor Assembly 2A2A4A33, Component Location, Figure 5-65.

j. 100 KC Rotor Assembly 2A2A4A34, Component Location, Figure 5-68.

k. 10 KC Rotor Assembly 2A2A4A35, Component Location, Figure 5-64.

l. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Amplifier Test Set, TS-2132/WRC-1.

(4) Electronic Multimeter, AN/USM-116.

(5) Multimeter, AN/PSM-4.

m. Refer to paragraph 1-17 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700, for rf amplifier V1 megacycle assembly adjustments.

4-104. RF AMPLIFIER V2, FUNCTIONAL CIRCUIT DESCRIPTION. RF amplifier V2 circuit (figure 4-18), which forms a part of RF Amplifier Electronic Assembly 2A2A4, amplifies the rf signal from rf amplifier V1 to a level suitable for driving the AM-3007/URT. The following paragraphs describe the operation of this circuit in detail.

4-105. The signal from rf amplifier V1 is coupled through capacitor C5, passes through parasitic suppressor FL2, and is applied to the control grid of rf amplifier V2. Screen voltage (110 vdc) for rf amplifier V2 is applied through decoupling resistor A1R6. Plate voltage (110 vdc) for rf amplifier V2 is applied through decoupling resistor A1R6, the primary rf transformer T4, and parasitic suppressor FL3. Capacitor C7 is an RF bypass. The cathode bias for rf amplifier V2 is developed across resistor A1R5. The output circuit for rf amplifier V2 consists of transformer T4 and capacitor C5 in series with a capacitance network comprised of capacitors C13 and C14 and the capacitors on circuit board assemblies A37 and A36. These components form a parallel tuned circuit. See paragraph 4-98 for a discussion of this tuned circuit, except note that the 100 kc capacitors are located on assembly A37 and the 10 kc capacitors are located on assembly A36.

4-106. The rf signal, amplified by rf amplifier V2, is applied to RF Amplifier AM-3007/URT.

4-107. RF AMPLIFIER V2, TEST DATA. Pertinent references for the rf amplifier V2 circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. RF Amplifier Electronic Assembly, Servicing Block Diagram, Figure 4-75.

c. RF Amplifier Electronic Assembly, Schematic Diagram, Figure 5-8.

d. RF Amplifier Bias Circuit Board, Component Location, Figure 5-45.

e. Megacycle Assemblies (2A2A4A2 through 2A2A4A29), Component Location, Figures 5-47 through 5-62.

f. 10 KC Rotor Assembly 2A2A4A36, Component Location, Figure 5-66.

g. 100 KC Rotor Assembly 2A2A4A37, Component Location, Figure 5-67.

h. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Amplifier Test Set, TS-2132/WRC-1.

(4) Electronic Multimeter, AN/USM-116.

(5) Multimeter, AN/PSM-4.

i. Refer to paragraph 1-17 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700, for rf amplifier V2 megacycle assembly adjustments.

4-108. TTY MARK GENERATOR AND LINE ISOLATION OSCILLATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The TTY mark generator and line isolation oscillator (figure 4-19) consists of a modified Colpitts oscillator (Q1) and an input polarity protection diode (CR1). This circuit, which forms a part of FSK Tone Generator Electronic Assembly 2A2A9, provides a burst of frequency representative of the presence of a "mark" at the input termin-

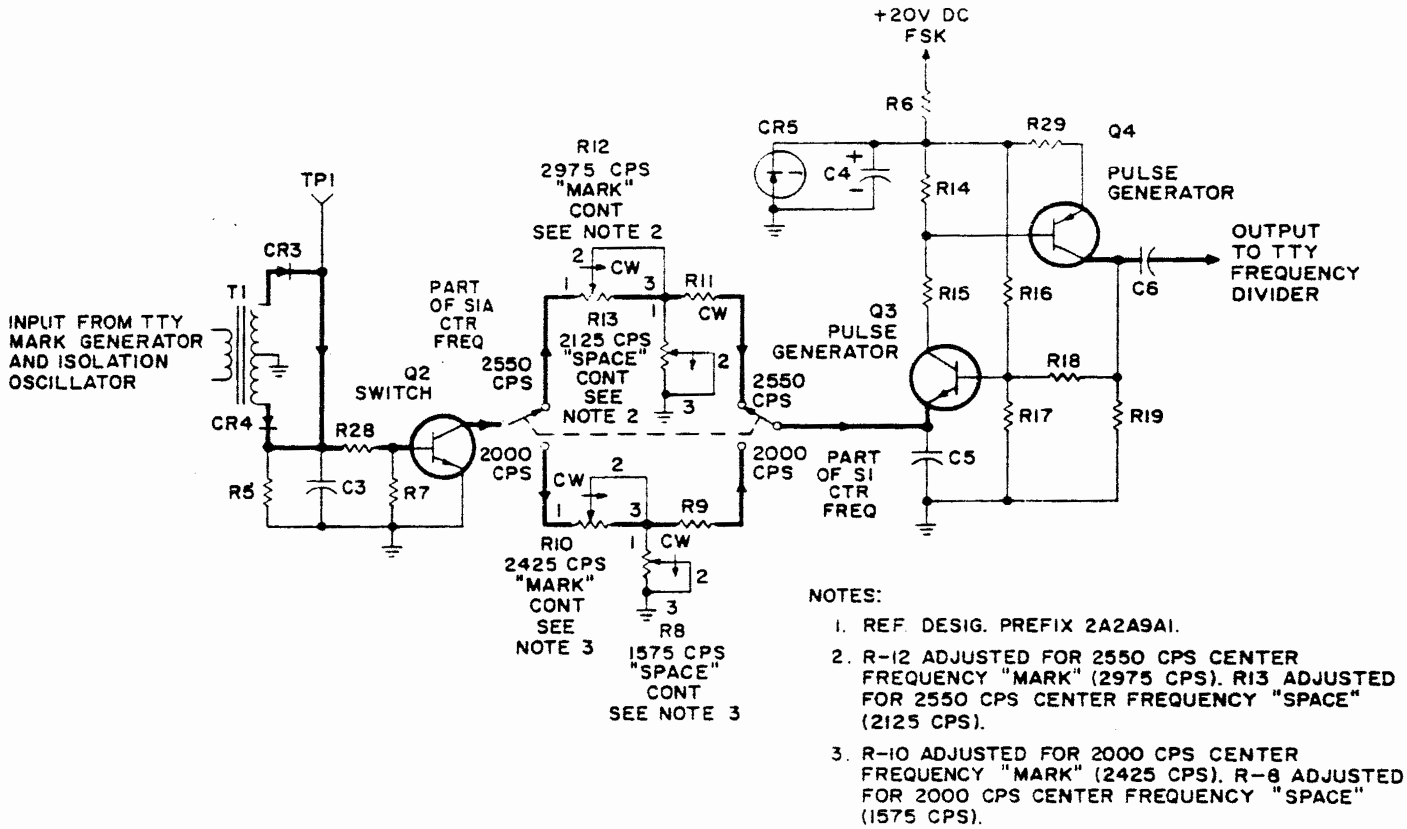


Figure 4-20. TTY Pulse Generator, Simplified Schematic Diagram

4-114. When a "mark" is applied to the input, the a-c output from the TTY mark generator and line isolation oscillator is coupled to diodes CR3 and CR4 by transformer T1. Regardless of signal polarity, the signal is rectified by either diode CR3 or CR4, and the resulting dc voltage is developed across resistor R5. Capacitor C3 smoothes the rectified voltage output from diode CR3 or CR4. The voltage developed across resistor R5 is applied to voltage divider R28, R7, which develops the base bias for switch Q2. With this voltage on the base of switch Q2, it is forward-biased and conducts, effectively placing ground on one side of resistor R12. This ground parallels resistors R12 and R13, and the resulting change in the discharge time constant for capacitor C5 shifts the repetition rate of relaxation oscillator Q3, Q4 to 5950 pps. As soon as the "mark" is removed from the base of transistor Q2, the frequency of oscillator Q3, Q4 returns to the "space" repetition rate of 4250 pps.

4-115. With switch S1 in the 2000-cps position, the "space" repetition rate of relaxation oscillator Q3, Q4 is 3150 pps. When a "mark" is applied to the base of switch Q2, the repetition rate is shifted to 4850 pps. When the "mark" is removed from the base of switch Q2, the repetition rate of relaxation oscillator Q3, Q4 returns to 3150 pps. The negative sawtooth pulses present at the collector of transistor Q4 are coupled to the TTY frequency divider by capacitor C6.

4-116. TTY PULSE GENERATOR, TEST DATA. Pertinent references and applicable test data for the TTY pulse generator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. FSK Tone Generator Electronic Assembly, Schematic Diagram, Figure 5-17.

c. FSK Tone Generator Electronic Assembly, Servicing Block Diagram, Figure 4-76.

d. FSK Tone Generator, Component and Test Point Location, Figure 5-112.

e. Required Test Equipment:

(1) Oscilloscope, AN/USM-105A.

(2) Frequency Meter, CAQI-524D.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W9.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. FSK Tone Generator Electronic Assembly, Adjustments, Paragraph 5-40.

4-117. TTY FREQUENCY DIVIDER, FUNCTIONAL CIRCUIT DESCRIPTION. The TTY frequency divider (figure 4-21) is a bistable multivibrator consisting of two transistors (Q5 and Q6). This circuit, which forms a part of FSK Tone Generator Electronic Assembly 2A2A9, divides the output from the TTY pulse generator by two, producing a series of pulses having a 50 per cent duty cycle. The 50 per cent duty cycle is required to ensure that the even harmonics are not generated in the FSK tone output. The following paragraph describes the operation of the TTY frequency divider in detail.

4-118. The output from the TTY pulse generator is coupled to steering diodes CR7 and CR8 by capacitor C6. Assuming that transistor Q6 is turned on and transistor Q5 is turned off, the negative portion of the input pulse applied to the base of transistor Q6 (through diode CR8, resistor R24, and capacitor C8) will turn off transistor Q6. With transistor Q6 turned off, the voltage on the base of transistor Q5 becomes more positive, thus turning on transistor Q5. Capacitor C7 discharges through diodes CR7 and CR6. When the next negative pulse is applied, it is coupled through diode CR7, resistor R21, and capacitor C7 to the base of transistor Q5, turning the transistor off. Capacitor C8 will now discharge through diodes CR8 and CR6. Therefore, transistor Q5 provides one output pulse for every two pulses applied to the input of the TTY frequency divider. The pulsed output at the collector of transistor Q5, which has a 50 per cent duty cycle, is coupled to the TTY pulse shaper by capacitor C11. Diode CR6 aids recovery of the circuit by providing a low resistance path through which capacitors C7 and C8 can discharge. The diode also prevents loading of the input pulses.

4-119. TTY FREQUENCY DIVIDER, TEST DATA. Pertinent references and applicable

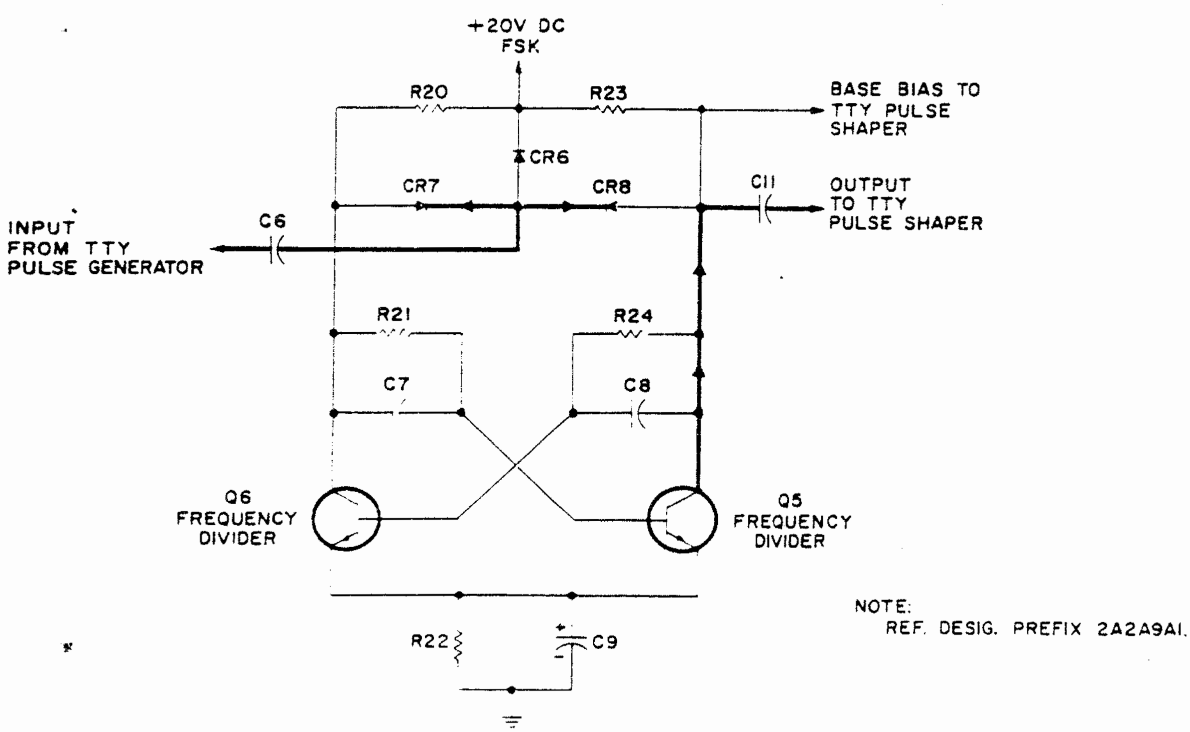


Figure 4-21. TTY Frequency Divider, Simplified Schematic Diagram

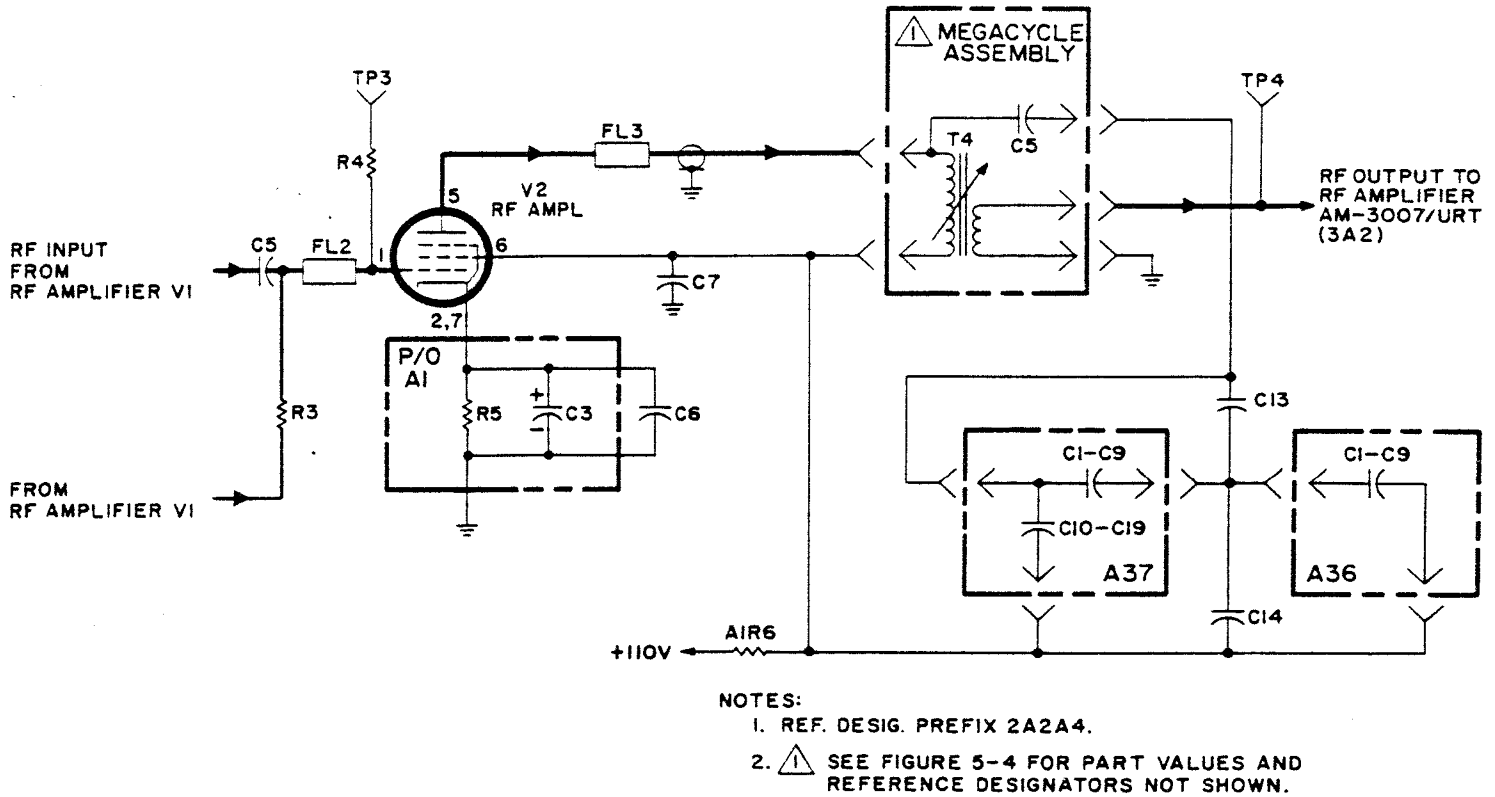


Figure 4-18. RF Amplifier V2, Simplified Schematic Diagram

als. This circuit also provides line isolation between the external teletype equipment and FSK Tone Generator Electronic Assembly 2A2A9. The following paragraph describes the operation of the TTY mark generator and line isolation oscillator in detail.

4-109. The TTY mark generator and line isolation oscillator input is either a "space" (0 ma) or a "mark" (no less than 5 ma). In order for this circuit to operate, the positive output from the teletype equipment must be connected to the anode of diode CR1. When a "mark" is

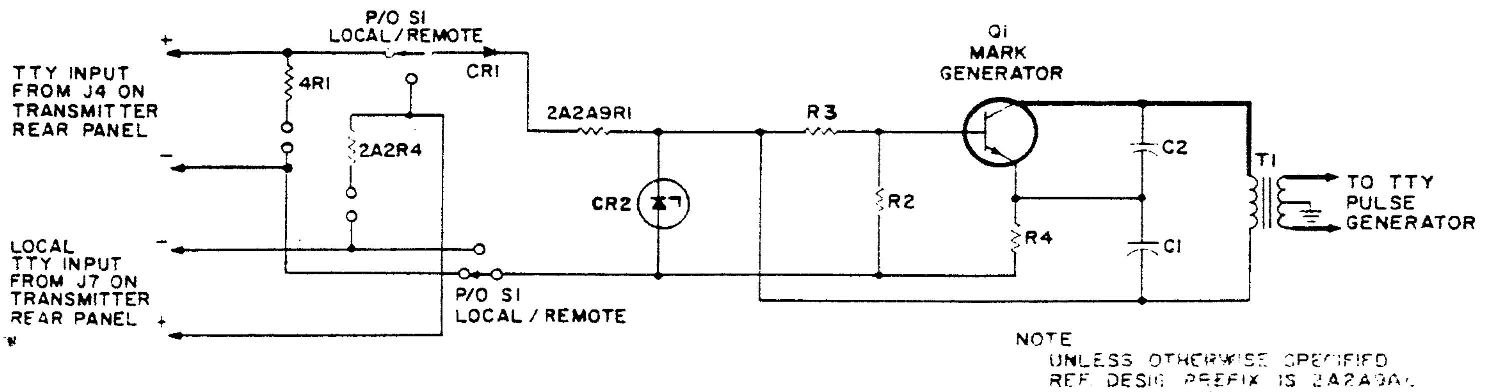


Figure 4-19. TTY Mark Generator and Line Isolation Oscillator, Simplified Schematic Diagram

applied to the input of the TTY mark generator the voltage used to produce the "mark" is held at a constant 18-vdc level by zener diode CR2, which draws enough current to drop the remaining applied voltage across resistor 2A2A9R1. When high TTY loop currents (up to 75 ma) are required, for local operation, resistor 2A2R4 on the transmitter main frame must be shunted across the input terminals. For remote operation, resistor 4R1, in the J-1265/U, must be shunted across the input terminals. These two resistors enable the TTY loop to operate at the higher current levels. The regulated 18 vdc is applied to voltage divider network R2, R3 which develops the base bias voltage to turn on modified Colpitts oscillator Q1. When a "mark" is applied, transistor Q1 will turn on, allowing the tank circuit, which consists of capacitors C1, C2, and the primary of transformer T1 to oscillate at a 50-to 80-kc rate. This signal is coupled to the TTY pulse generator by transformer T1. The positive feedback (collector to emitter) required to sustain oscillation for the period during which a "mark" is present at the input terminals, is developed by voltage divider network C1, C2. When a "space" (0 ma) is present at the input to the TTY mark generator and isolation oscillator, transistor Q1 is turned off.

4-110. TTY MARK GENERATOR AND LINE ISOLATION OSCILLATOR, TEST DATA. Pertinent references and applicable test data for the TTY mark generator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. FSK Tone Generator Electronic Assembly, Schematic Diagram, Figure 5-17.

c. FSK Tone Generator Electronic Assembly Servicing Block Diagram, Figure 4-76.

d. FSK Tone Generator, Component and Test Point Location, Figure 5-112.

e. Required Test Equipment:

(1) Oscilloscope, AN/USM-105A.

(2) Frequency Meter, CAQI-524D.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W9.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

4-111. TTY PULSE GENERATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The TTY pulse generator (figure 4-20) consists of a switch (Q2) and a relaxation oscillator (Q3, Q4). This circuit, which forms a part of FSK Tone Generator Electronic Assembly 2A2A9, produces two series of trigger pulses to the TTY frequency divider, the repetition rates of which are representative of either a "space" or a "mark". Each series is generated around a different discrete center frequency. The following paragrapns describe the operation of the TTY pulse generator in detail.

4-112. The positive 20 vdc applied to the TTY pulse generator from the Mode Selector switch on the front panel is regulated to 18 vdc by Zener diode CR5, which draws enough current in addition to the load current to maintain a 2-volt drop across resistor R6. Capacitor C4 maintains a nearly constant charge, thereby providing additional regulation for the 18 vdc. Voltage divider R16, R17 develops the base bias for pulse generator Q3 from the regulated 18 vdc output from Zener diode CR5. Voltage divider R14, R15 develops the base bias for pulse generator Q4 from the regulated 18 vdc output from zener diode CR5.

4-113. With switch S1 in the 2550 cps position, relaxation oscillator Q3, Q4 is free-running at the "space" repetition rate of 4250 pps. When transistor Q3 is conducting, transistor Q4 is also conducting, charging capacitor C5 until the voltage across it equals the base voltage of transistor Q3. At this time, transistor Q3 is back-biased and turns off. When transistor Q3 turns off, the base voltage on transistor Q4 will increase to the same level as the voltage on the emitter, turning it off. With both transistors Q3 and Q4 turned off, capacitor C5 discharges through resistors R13 and R11. When the voltage across capacitor C5 decreases to less than the base voltage of transistor Q3, transistor Q3 will turn back on. When transistor Q3 turns back on, the voltage on the base of transistor Q4 will decrease to less than the emitter voltage, and it will turn on. The output at the collector of transistor Q4 is applied to the base of transistor Q3 through voltage divider R17, R18. Therefore, this turn-on/turn-off procedure is sustained at the desired 4250-pps rate.

test data for the TTY frequency divider are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. FSK Tone Generator Electronic Assembly, Schematic Diagram, Figure 5-17.

c. FSK Tone Generator Electronic Assembly, Servicing Block Diagram, Figure 4-76.

d. FSK Tone Generator Electronic Assembly, Component and Test Point Location, Figure 5-112.

e. Required Test Equipment:

(1) Oscilloscope, AN/USM-105A.

(2) Frequency Meter, CAQI-524D.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W9.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

4-120. TTY PULSE SHAPER, FUNCTIONAL CIRCUIT DESCRIPTION. The TTY pulse shaper (figure 4-22) is a squaring amplifier consisting of one transistor (Q7). This circuit, which forms a part of FSK Tone Generator Assembly 2A2A9, shapes the pulsed output from the TTY frequency divider to form a good square wave output. The following paragraph describes the operation of the TTY pulse shaper in detail.

4-121. When the output from the TTY frequency divider is coupled to the base of squaring amplifier Q7 by capacitor C11, amplifier Q7 is driven into saturation, thus producing a square-wave output. The amplitude of the square wave is controlled by the setting of potentiometer R26. The base bias for squaring amplifier Q7 is applied from the TTY frequency square-wave output. The amplitude of the square wave is controlled by the setting of resistor R26. The base bias for squaring amplifier Q7 is applied from the TTY frequency divider through resistor R27. The square-wave output is coupled by capacitor C10 to the Mode Selector switch on the front panel. The square-wave output is applied through the Mode Selector switch to Transmitter Audio Amplifier Electronic Assembly 2A2A2, where it is amplified and applied to balanced modulator A1 in Mode Selector Electronic Assembly 2A2A1 to modulate the 500-kc carrier during the FSK mode of operation. The odd harmonics are eliminated from the FSK tone output by the sideband filter in the Transmitter Mode Selector Electronic Assembly.

4-122. TTY PULSE SHAPER, TEST DATA. Pertinent references and applicable test data for the TTY pulse shaper are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

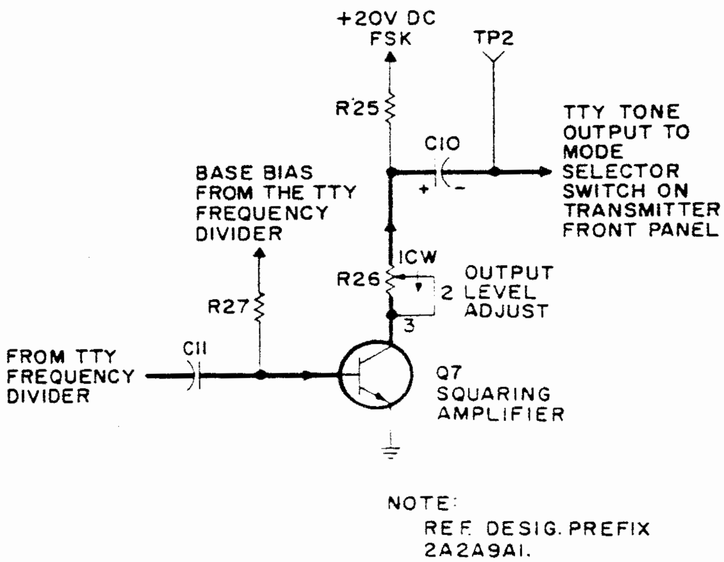


Figure 4-22. TTY Pulse Shaper, Simplified Schematic Diagram

b. FSK Tone Generator Electronic Assembly, Schematic Diagram, Figure 5-17.

c. FSK Tone Generator Electronic Assembly, Servicing Block Diagram, Figure 4-76.

d. FSK Tone Generator Electronic Assembly, Component and Test Point Location, Figure 5-112.

e. Required Test Equipment:

(1) Oscilloscope, AN/USM-105A.

(2) Frequency Meter, CAQI-524D.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W9.

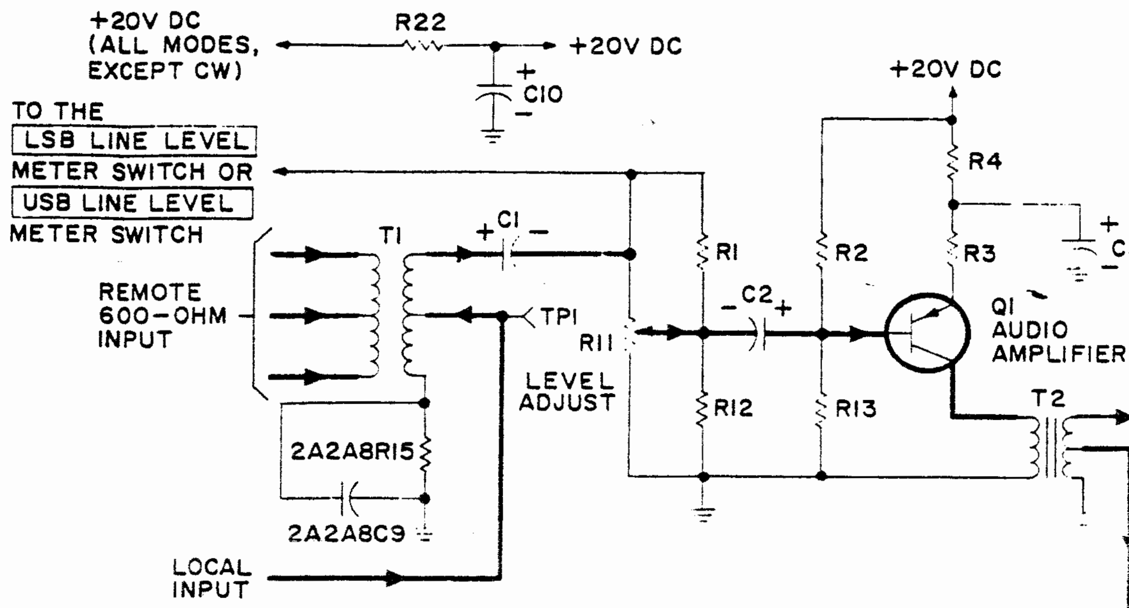
(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. FSK Tone Generator Electronic Assembly, Adjustments, Paragraph 5-40.

4-123. AUDIO AMPLIFIERS, FUNCTIONAL CIRCUIT DESCRIPTION. The audio amplifiers (figure 4-23) consist of two audio amplification circuits (Q1 and Q4), two emitter follower isolation stages (Q3 and Q5), and a speech compression circuit (T2, CR1, RV1, RV2, and Q2). These circuits, which form a part of Transmitter Audio Amplifier Electronic Assemblies 2A2A2 and 2A2A3, provide a constant usable audio input signal to the balanced modulator circuits. The speech compression circuit reduces the peak-to-average ratio of voice signals to maintain a constant average percentage of modulation above 60 per cent. The emitter followers are used for isolation and impedance matching. The circuits of Transmitter Audio Amplifier Electronic Assembly 2A2A2 are used during the USB, AM, and FSK modes of operation. The circuits of Transmitter Audio Amplifier Electronic Assembly 2A2A3 are used during the LSB mode of operation. The circuits of both electronic assemblies are used during the ISB mode of operation. The following paragraphs describe the operation of these circuits in detail.

4-124. The remote audio signals are applied to the primary of transformer T1, which is a balanced (grounded center tap) or unbalanced (open center tap) 600-ohm line input. The local audio signals are applied to the secondary of transformer T1, which is an unbalanced input. Transformer T1 couples the audio to potentiometer R11, which establishes the level of the audio signals coupled to the base of amplifier Q1 by capacitor C2. The audio is also coupled to the USB LINE LEVEL meter switch or LSB LINE LEVEL meter switch for application to the corresponding meter amplifier circuit. The parallel-series combination of resistors R12, R1, and R11 provides an approximate 600-ohm terminating resistance for transformer T1. Resistor 2A2A8R15, which is bypassed by capacitor 2A2A8C9, limits the dc current flow through the microphone. The applied audio signals are raised in level by amplifier Q1 and are developed across the primary of transformer T2. A small amount of degeneration (produced by resistor R3) increases the stability of the circuit. The operating voltage for amplifier Q1 is developed by voltage divider R2, R13 and emitter resistors R3 and R4 from the positive 20 vdc applied from the Mode Selector switch on the front panel.

4-125. The output from amplifier Q1 is coupled to voltage divider R15, RV2 by transformer T2. The resistance of varistors RV1 and RV2 varies with the dc voltage applied to it. The amplified audio voltage at the output of amplifier Q1 is coupled to the base of agc amplifier Q2 by transformer T2. The audio voltage is detected by agc amplifier Q2 and the resulting dc voltage is developed across resistor R16 and varistors RV1 and RV2. Diode CR1 protects the base-emitter junction of agc amplifier Q2 against excessive reverse bias. A varistor is a voltage-sensitive device, the resistance of which varies inversely with the applied voltage. Filter C5 smoothes the compression effect of varistors RV1 and RV2 and also filters the dc voltage output from agc amplifier Q2. As the input audio voltage increases, the resistance of varistors RV1 and RV2 decreases, and as the input audio voltage decreases, the resistance of varistors RV1 and RV2 increases. Therefore, since the resistance of varistors RV1 and RV2 varies inversely with the input audio voltage, the output from voltage divider R15, RV1 and RV2 is maintained at a nearly constant level. As far as the audio signal is concerned, RV1 and RV2 are in parallel and constitutes the lower leg of the voltage divider. The operating voltage for emitter follower Q2 is applied directly from the Mode Selector switch on the front panel.


+20V DC
(ALL MODES,
EXCEPT CW)
R22
+20V DC
C10
+20V DC
TO THE
LSB LINE LEVEL
METER SWITCH OR
USB LINE LEVEL
METER SWITCH
R4
T1
C1
R1
R2
R3
REMOTE
600-OHM
INPUT
TP1
C2
R11
Q1
AUDIO
AMPLIFIER
LEVEL
ADJUST
T2
R12
R13
2A2A8R15
2A2A8C9
LOCAL
INPUT

139/140

4-126. The audio output from voltage divider R15, RV1 and RV2 is coupled to the base of emitter follower Q3 by capacitor C4. Emitter follower Q3 is an isolation stage which prevents loading of voltage divider R15, RV1 and RV2. The operating voltage for emitter follower Q3 is developed by voltage divider R23, R5, R17 and emitter resistor R6 from the positive 20 vdc applied from the Mode Selector switch on the front panel.

4-127. The output audio signals from emitter follower Q3, developed across resistor R6, are coupled to the base of amplifier Q4 by capacitor C6. The applied signals are raised in level by amplifier Q4 and developed across collector resistor R19. A small amount of degeneration, produced by resistor R20, increases the stability of the circuit. The operating voltage for amplifier Q4 is developed by voltage divider R7, R18 and emitter resistors R8 and R20 from the positive 20 vdc applied from the Mode Selector switch on the front panel.

4-128. The amplified output signals from amplifier Q4 are coupled to the base of emitter follower Q5 by capacitor C7. Emitter follower Q5 provides the audio amplifier circuit with a low impedance output. The operating voltage for emitter follower Q5 is developed by voltage divider R9, R21 and emitter resistor R10 from the positive 20 vdc applied from the Mode Selector switch on the front panel.

4-129. The audio output signals from emitter follower Q5, developed across resistor R10, are coupled to one of the balanced modulator circuits by capacitor C9. The outputs from Transmitter Audio Amplifier Electronic Assembly 2A2A2 are coupled to balanced modulator A1. The outputs from Transmitter Audio Amplifier Electronic Assembly 2A2A3 are coupled to balanced modulator A2.

4-130. AUDIO AMPLIFIERS, TEST DATA. Pertinent references and applicable test data for the audio amplifiers circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Audio Amplifier Electronic Assembly, Servicing Block Diagram, Figure 4-73.

c. Transmitter Audio Amplifier Electronic Assembly, Schematic Diagram, Figure 5-7.

d. Refer to Maintenance Standards Book for Radio Set AN/WRC-1 and Antenna Coupler CU-937/UR, NAVSHIPS 94840.42A for all adjustment information.

e. Required Test Equipment:

(1) Audio Signal Generator, AN/URM-127.

(2) Multimeter, AN/PSM-4.

(3) Electronic Multimeter, ME-6( )/U.

(4) Cable Assembly, W5.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. Audio Amplifiers, Component and Test Point Location, Figure 5-40.

4-131. CW CARRIER REINSERTION GATE, FUNCTIONAL CIRCUIT DESCRIPTION. The CW carrier reinsertion gate (figure 4-24) consists of three gating circuits (CR16, CR17, CR18). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, gate the 500-kc local carrier into if. amplifiers for re-insertion during the CW mode of operation. In all modes of operation except CW, gate CR18 is biased on to prevent any leakage from this circuit. Gate CR17 controls the bias on gate CR16 each time the transmitter is keyed during the CW mode of operation. The following paragraphs describe the operation of the CW carrier reinsertion gate circuit in detail.

4-132. The 500-kc signal (from Frequency Standard Electronic Assembly 2A2A5) is coupled through capacitor C41 and isolating resistor R86 to the anode of gate CR16. A positive 13.3-vdc anode bias is developed on gate CR16 by voltage divider R85, R87 from the positive 20 vdc applied from the Mode Selector switch (set at CW position) on the front panel. The cathode of diode CR16 is biased at approximately 17 vdc until the transmitter is keyed. A ground is then applied through diode CR17 to resistor R89. This reduces the cathode bias instantaneously to 9.9 vdc as a result of the voltage divider action of resistors R115, R90, R89, and R88. When a gate is conducting, both biases are approximately the same; the

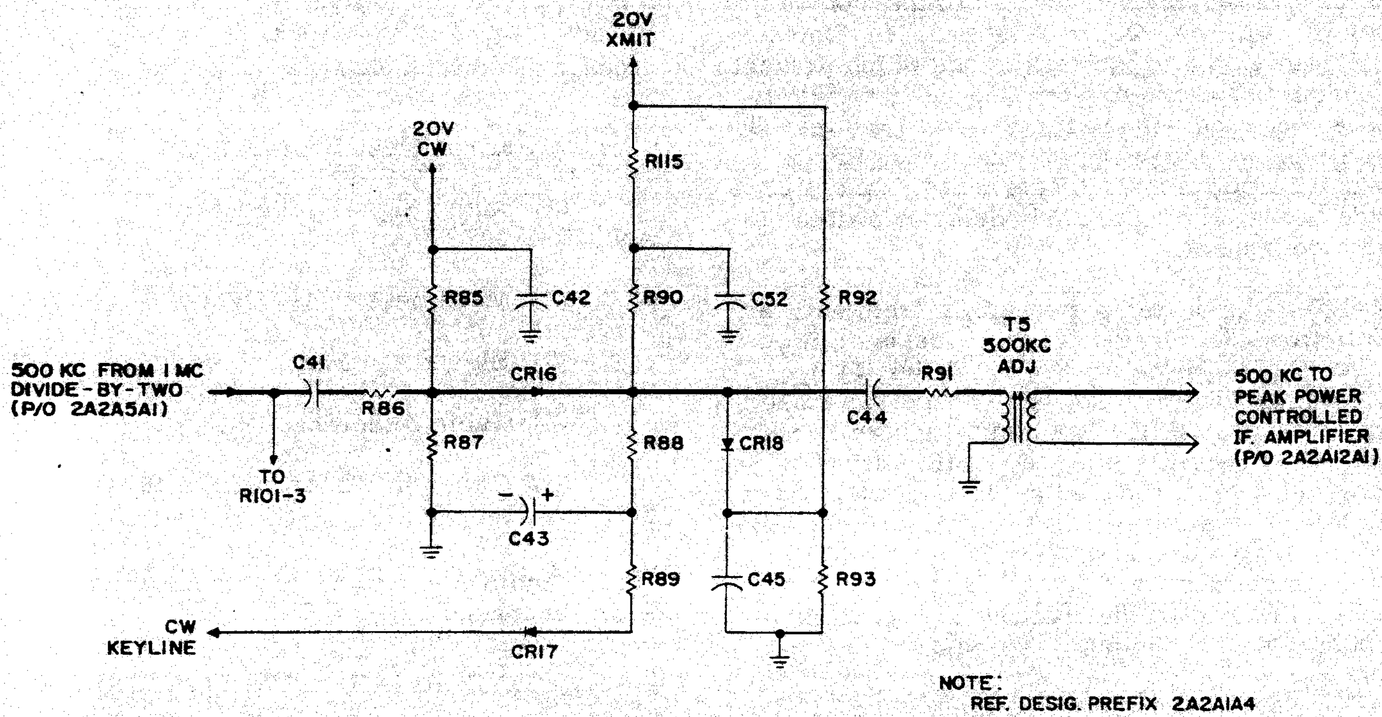


Figure 4-24. CW Carrier Reinsertion Gate, Simplified Schematic Diagram

difference is the voltage drop caused by the forward resistance of the diode. Thus, when the transmitter is keyed, gate CR16 is forward-biased and conducts, allowing the 500-kc signal to pass. The 500-kc signal is coupled by capacitor C44 to the primary of transformer T5. Transformer T5 couples the 500-kc signal to the peak power controlled if. amplifier circuit.

4-133. In each mode of operation, except when the transmitter is keyed in the CW mode, the cathode of gate CR16 is biased at approximately 17 vdc, which is also the anode bias for gate CR18. The cathode of gate CR18 is biased at approximately 17 vdc also. This bias is developed by voltage divider R115, R92, R93 from the 20 vdc applied from the Mode Selector switch on the front panel. Therefore, gate CR18 will be forward-biased and will conduct, effectively shorting gate CR16 to ground through capacitor C45. This insures that any leakage through gate CR16 will be bypassed to ground when the transmitter is not being keyed in the CW mode of operation. When the transmitter is keyed, the cathode bias of gate CR16 drops instantaneously to 9.9 vdc; consequently, the anode bias of gate CR18 is at the same level. Since the cathode of gate CR18 is still biased at approximately 17, gate CR18 is now reverse-biased, removing the short from gate CR16.

4-134. CW CARRIER REINSERTION GATE, TEST DATA. Pertinent references and applicable test data for the CW carrier reinsertion gate circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic Assembly, Adjustments, Paragraph 5-28.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. 500 KC Amplifiers/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

4-135. CW SIDETONE OSCILLATOR/GATE, FUNCTIONAL CIRCUIT DESCRIPTION. The CW sidetone oscillator/gate (figure 4-25) consists of a phase shift oscillator (Q8) and a gating diode (CR13). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, produce an audio tone that is applied to the receiver, enabling the operator to monitor the keying when operating in the CW mode of operation. The following paragraphs describe the operation of the CW sidetone oscillator/gate circuit in detail.

4-136. Since the signal between base and collector is reversed 180 degrees in phase, in a common emitter phase-shift oscillator an additional 180-degree phase shift is necessary to keep the feedback signal (from output to input) positive. The phase shift occurs in an RC network consisting of three sections, each contributing a 60-degree phase shift at the frequency of oscillation. In figure 4-25, the three RC sections are R68 and C36, R67 and C35, and conducts, allowing the audio output of phase-shift oscillator Q8 to pass. When gate CR13 conducts, both biases are approximately equal. The difference in biases is the voltage and R66 and C34. When operating in the CW mode, operating voltage for this circuit is developed from the 20 vdc applied to voltage divider R65, R64, RT1 and emitter resistor R63 from the Mode Selector switch on the front panel. Thermistor RT1 stabilizes the circuit for any ambient temperature changes. Voltage divider R69, R70 determines the level of the audio tone (approximately 1 kc), produced by phase-shift oscillator Q8, and coupled to the cathode of gate CR13 by capacitor C37.

4-137. When the transmitter is not keyed for CW operation, gate CR13 is reverse-biased as a result of the positive 13.2 vdc on the cathode and the positive 10 vdc on the anode. The two biases are developed by voltage dividers R71, R74 and R75, R76 from the positive 20 vdc applied from the power supply on the main frame of the transmitter. Each time the CW key is depressed, ground is applied through diode CR12 to resistor R73. This causes the cathode bias to drop to 8.3 vdc. This instantaneous bias voltage is developed by the new voltage divider, consisting of R71 and the parallel combination of R72, R73, and R74. Since the anode of the diode is still biased at 10 vdc, gate CR13 becomes forward-biased

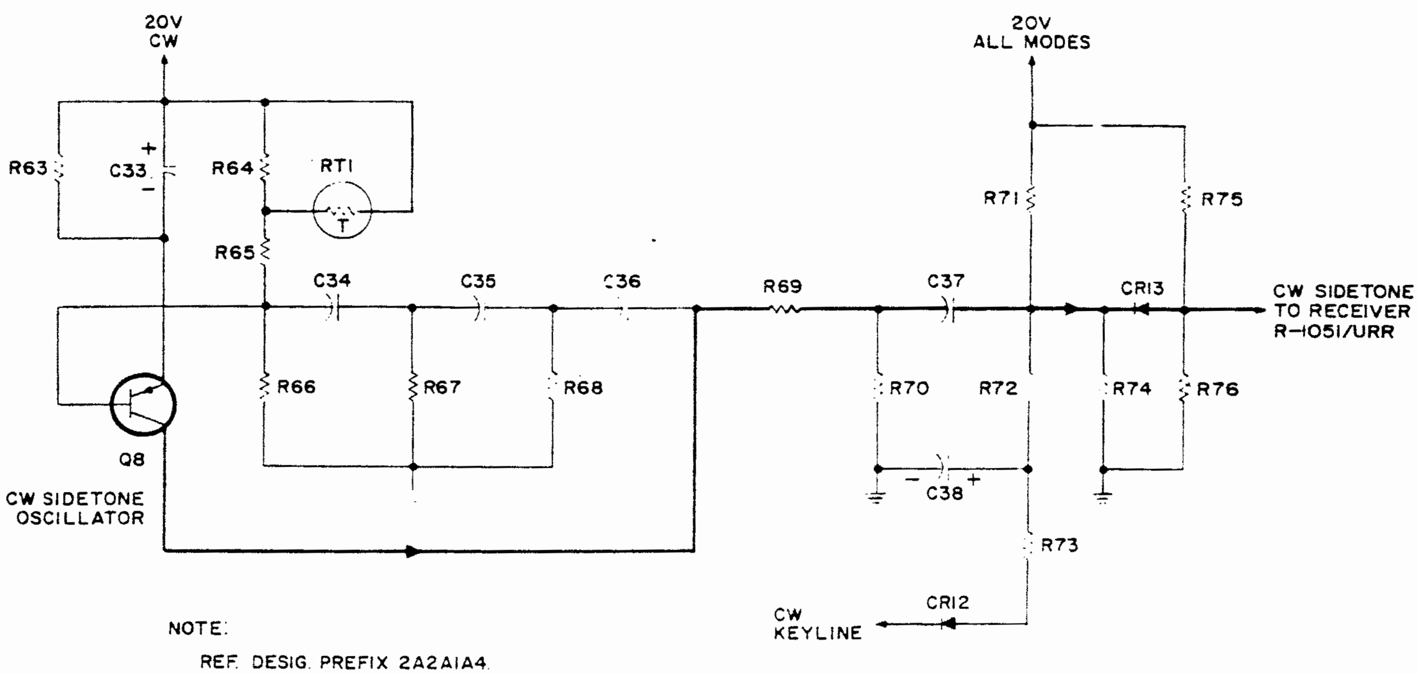


Figure 4-25. CW Sidetone Oscillator/Gate, Simplified Schematic Diagram

drop caused by the forward resistance of the diode. The audio tone is applied to the receiver, where it is amplified in the audio amplifiers and applied to the headset and the 600-ohm USB audio output line. This tone allows the operator to monitor the keying when operating in the CW mode of operation.

4-138. CW SIDETONE OSCILLATOR/GATE, TEST DATA. Pertinent references and applicable test data for the CW sidetone oscillator/gate circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Required Test Equipment:

(1) Electronic Multimeter, CCVO-91CA.

(2) Frequency Meter, CAQI-524D.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

e. 500 KC Amplifiers/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

4-139. SIDETONE GATE, FUNCTIONAL CIRCUIT DESCRIPTION. Sidetone gate CR14 or CR15 (figure 4-26), which forms a part of Transmitter Mode Selector Assembly 2A2A1, gates the audio intelligence to the receiver, enabling the operator to monitor the transmissions. Gate CR14 is used during the USB, AM and FSK modes of operation. Gate CR15 is used during the LSB mode of operation. Both gates are used during the ISB mode of operation. The following paragraphs describe the operation of the sidetone gate circuit in detail.

4-140. The audio applied to balanced modulator A1, from Transmitter Audio Amplifier Electronic Assembly 2A2A2, is coupled to the anode of gate CR14 through coupling capacitor C39 and isolating resistor R77. This gate will

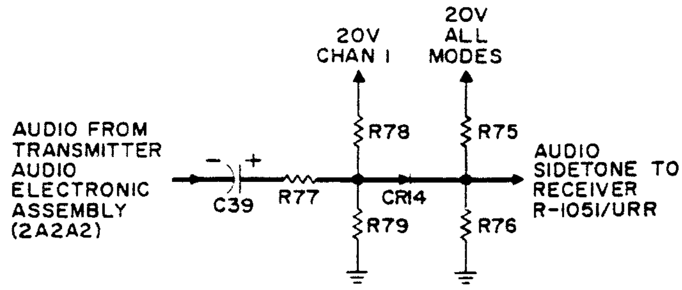


Figure 4-26. Sidetone Gate, Simplified Schematic Diagram

be forward-biased in the USB, AM, FSK, or ISB modes of operation by the positive 16.7 vdc on the anode and the positive 10 vdc on the cathode. The two biases are instantaneous voltages, which are developed from the positive 20 vdc applied to the voltage dividers R78, R79 and R75, R76 by the Mode Selector switch on the front panel. When gate CR14 is conducting, both biases are approximately equal. The difference in biases is the voltage drop caused by the forward resistance of the diode. The gate is forward-biased and will conduct, allowing the audio to pass. This audio is applied to the receiver, where it is amplified by the audio amplifier and applied to the headset and the USB 600-ohm audio output line. This tone allows the operator to monitor the audio intelligence being transmitted.

4-141. Sidetone gate CR15 is identical to sidetone gate CR14 (figure 5-6). This gate is biased on during the LSB and ISB modes of operation. The audio to be gated by gate CR15 is applied from balanced modulator A2. The amplified output from the receiver is applied to the headset and LSB 600-ohm audio line for monitoring.

4-142. SIDETONE GATE, TEST DATA. Pertinent references and applicable test data for the sidetone gate circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. 500 KC Amplifier/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

e. Required Test Equipment:

(1) Multimeter, AN/PSM-4.

(2) Cable Assembly, W1.

(3) Common Electronic Circuits Test Set, TS-2135/WRC-1.

4-143. AM CARRIER REINSERTION GATE, FUNCTIONAL CIRCUIT DESCRIPTION. The AM carrier reinsertion gate circuit (figure 4-27) consists of three gating circuits (CR19, CR20, CR21). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, gate the 500-kc local carrier into the peak power controlled if. amplifier circuit for reinsertion into the if. signal during the AM mode of operation. Gate CR20 is biased on in all modes of operation except AM, to prevent any leakage from this circuit, when it is not being used. Gate CR21 provides dc isolation between the two 20-vdc lines when gate CR20 is biased on. The following paragraphs describe the operation of the AM carrier reinsertion gate in detail.

4-144. The 500-kc signal from 1 mc divide-by-two circuit (part of 2A2A5A1) is applied to potentiometer R101. The potentiometer sets the percentage of modulation of the AM signal. The output from the potentiometer is coupled to voltage divider R95, R96 by capacitor C46. Gate CR19 is forward-biased during AM operation with an anode bias of 16.7 vdc and a cathode bias of 13.3 vdc. These two biases are instantaneous voltages which are developed by voltage dividers R94, R96 and R98, R97 from the positive 20 vdc applied from the Mode Selector switch on the front panel. When a gate is conducting, both biases are approximately equal. The difference in biases is the voltage drop caused by the forward resistance of the diode. Since gate CR19 is forward-biased, it will conduct, allowing the 500-kc signal to pass. The 500-kc signal is coupled to the primary of transformer T5 by capacitor C47. Transformer T5 couples the 500-kc carrier to the peak power controlled if. amplifiers for reinsertion into the if. signal.

4-145. In each mode of operation, the cathode of gate CR19 is biased at 13.3 vdc. This bias also serves as the anode bias for gate CR20. Since gate CR21 is forward-biased only in AM operation, the anode will be open during the other modes of operation. Therefore, the cathode of gate CR20 is at zero voltage. As a result, gate CR20 will be forward-biased and will conduct, effectively shorting gate CR19 to ground through capacitor C49. This insures that any leakage through gate CR19 will be by-passed to ground whenever the transmitter is not being operated in the AM mode. When the transmitter is placed in the AM mode of operation, the anode of gate CR21 is biased at 20 vdc applied from the Mode Selector switch on the front panel. Since there is no voltage on

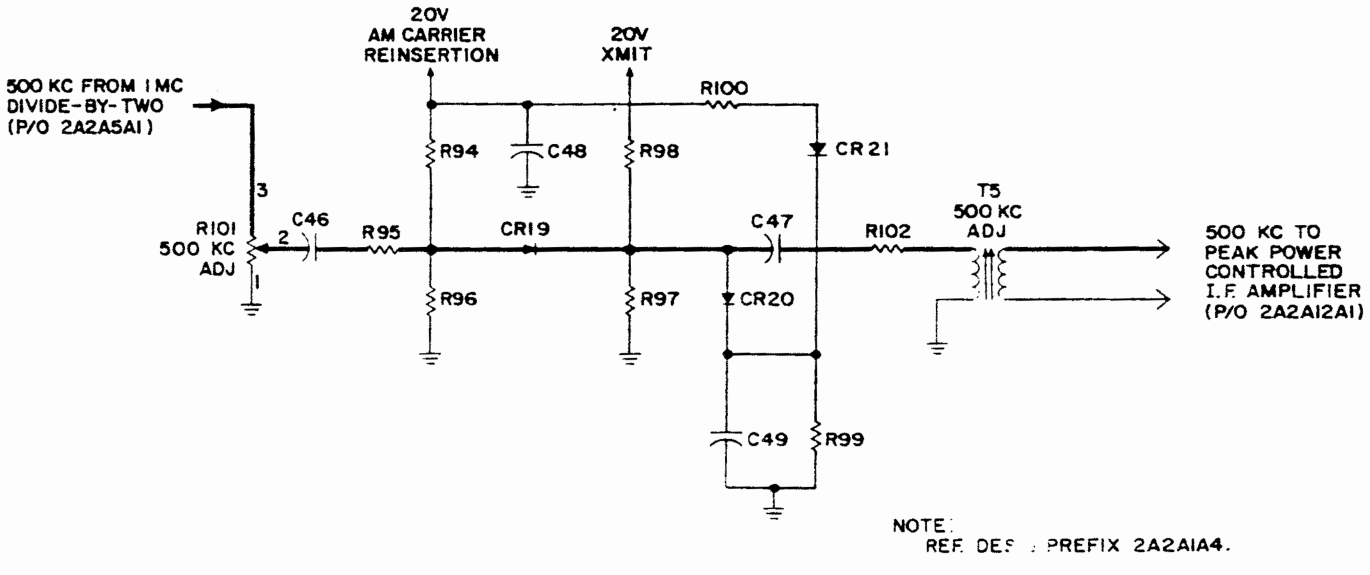


Figure 4-27. AM Carrier Reinsertion Gate, Simplified Schematic Diagram

the cathode of gate CR21, it is forward-biased and thus conducts. When gate CR21 conducts, the cathode of gate CR20 is biased at 16.5 vdc. This bias is developed by voltage divider R99, R100 from the positive 20 vdc applied from the Mode Selector switch on the front panel. Since the anode of gate CR20 is biased at 13.3 vdc, it will be reverse-biased and prevent the 500-kc signal from being applied to the 20-vdc supply lines.

4-146. AM CARRIER REINSERTION GATE, TEST DATA. Pertinent references and applicable test data for the AM carrier reinsertion gate circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic Assembly, Adjustments, Paragraph 5-28.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1.

(5) Common Electronic Circuit Test Set, TS-2135/WRC-1.

f. 500 KC Amplifiers/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

4-147. CARRIER REINSERTION LEVEL CONTROL FUNCTIONAL CIRCUIT DESCRIPTION. The carrier reinsertion level control (figure 4-28) consists of a gating circuit (CR100) and a variable attenuator circuit (S1). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, provide a pilot carrier for reinsertion into the if. signal to enable other radio sets with less stability than the AN/WRC-1 to receive transmissions from the T-827/URT. This carrier is used in these receivers for frequency-locking and demodulating. For normal use of the AN/WRC-1 the carrier is fully suppressed. These circuits provide a pilot carrier, when required, for the LSB, ISB, or USB modes of operation.

4-148. The 500-kc signal is coupled from the center of potentiometer R101 to voltage divider R110, R112 by capacitor C50. Potentiometer R101 is set so that the carrier is the same magnitude as the sideband when switch S1 is placed in the zero suppression position. The voltage divider limits the level of the 500-kc signal that is applied to the anode of gate CR100. During the USB, ISB, or LSB modes of operation, gate CR100 is forward-biased by the positive 16.7 vdc anode bias and the positive 13.3 vdc cathode bias. The two biases are instantaneous voltages, which are developed by voltage dividers R110, R111 and R108, R109 from the positive 20 vdc applied through contacts 11, and 10, 9, or 8 of switch S1. When gate CR100 is conducting, both biases are approximately equal. The difference in biases is the voltage drop caused by the forward resistance of the diode. Since gate CR100 is forward-biased, it will conduct, allowing the 500-kc signal to pass. The output from gate CR100 is coupled to one of three attenuator circuits by capacitor C51. The attenuator circuit used depends upon the position of switch S1. When switch S1 is set at the 0 DB SUPPR, 10 DB SUPPR, or 20 DB SUPPR position, the 500-kc signal is applied through the respective attenuator network and contacts 2, 3, or 4 and 5 of switch S1 to transformer T5. Transformer T5 couples the 500-kc signal to the peak power controlled if. amplifier for reinsertion into the if. signal.

4-149. CARRIER REINSERTION LEVEL CONTROL, TEST DATA. Pertinent references and applicable test data for the carrier reinsertion level control circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic Assembly, Adjustments, Paragraph 5-28.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

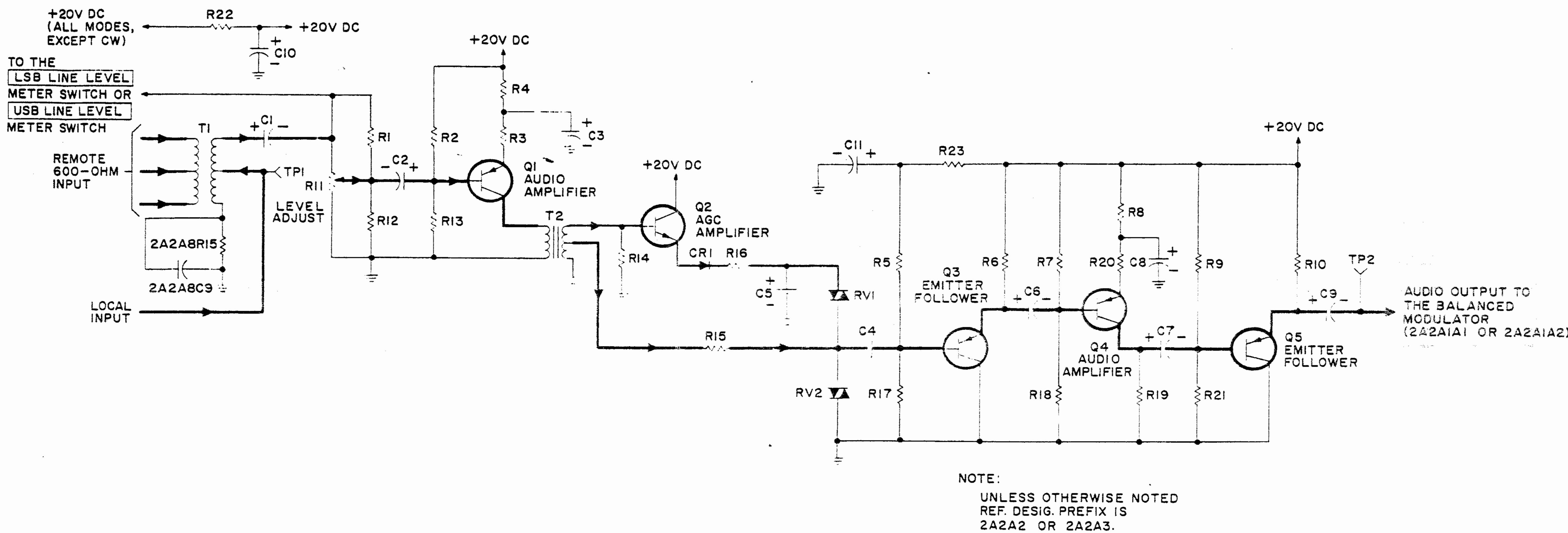


Figure 4-23, Audio Amplifier, Simplified Schematic Diagram

4-126. The audio output from voltage divider R15, RV1 and RV2 is coupled to the base of emitter follower Q3 by capacitor C4. Emitter follower Q3 is an isolation stage which prevents loading of voltage divider R15, RV1 and RV2. The operating voltage for emitter follower Q3 is developed by voltage divider R23, R5, R17 and emitter resistor R6 from the positive 20 vdc applied from the Mode Selector switch on the front panel.

4-127. The output audio signals from emitter follower Q3, developed across resistor R6, are coupled to the base of amplifier Q4 by capacitor C6. The applied signals are raised in level by amplifier Q4 and developed across collector resistor R19. A small amount of degeneration, produced by resistor R20, increases the stability of the circuit. The operating voltage for amplifier Q4 is developed by voltage divider R7, R18 and emitter resistors R8 and R20 from the positive 20 vdc applied from the Mode Selector switch on the front panel.

4-128. The amplified output signals from amplifier Q4 are coupled to the base of emitter follower Q5 by capacitor C7. Emitter follower Q5 provides the audio amplifier circuit with a low impedance output. The operating voltage for emitter follower Q5 is developed by voltage divider R9, R21 and emitter resistor R10 from the positive 20 vdc applied from the Mode Selector switch on the front panel.

4-129. The audio output signals from emitter follower Q5, developed across resistor R10, are coupled to one of the balanced modulator circuits by capacitor C9. The outputs from Transmitter Audio Amplifier Electronic Assembly 2A2A2 are coupled to balanced modulator A1. The outputs from Transmitter Audio Amplifier Electronic Assembly 2A2A3 are coupled to balanced modulator A2.

4-130. AUDIO AMPLIFIERS, TEST DATA. Pertinent references and applicable test data for the audio amplifiers circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Audio Amplifier Electronic Assembly, Servicing Block Diagram, Figure 4-73.

c. Transmitter Audio Amplifier Electronic Assembly, Schematic Diagram, Figure 5-7.

d. Refer to Maintenance Standards Book for Radio Set AN/WRC-1 and Antenna Coupler CU-937/UR, NAVSHIPS 94840.42A for all adjustment information.

e. Required Test Equipment:

(1) Audio Signal Generator, AN/URM-127.

(2) Multimeter, AN/PSM-4.

(3) Electronic Multimeter, ME-6( )/U.

(4) Cable Assembly, W5.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. Audio Amplifiers, Component and Test Point Location, Figure 5-40.

4-131. CW CARRIER REINSERTION GATE,

FUNCTIONAL CIRCUIT DESCRIPTION. The CW carrier reinsertion gate (figure 4-24) consists of three gating circuits (CR16, CR17, CR18). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, gate the 500-kc local carrier into if. amplifiers for re-insertion during the CW mode of operation. In all modes of operation except CW, gate CR18 is biased on to prevent any leakage from this circuit. Gate CR17 controls the bias on gate CR16 each time the transmitter is keyed during the CW mode of operation. The following paragraphs describe the operation of the CW carrier reinsertion gate circuit in detail.

4-132. The 500-kc signal (from Frequency Standard Electronic Assembly 2A2A5) is coupled through capacitor C41 and isolating resistor R86 to the anode of gate CR16. A positive 13.3-vdc anode bias is developed on gate CR16 by voltage divider R85, R87 from the positive 20 vdc applied from the Mode Selector switch (set at CW position) on the front panel. The cathode of diode CR16 is biased at approximately 17 vdc until the transmitter is keyed. A ground is then applied through diode CR17 to resistor R89. This reduces the cathode bias instantaneously to 9.9 vdc as a result of the voltage divider action of resistors R115, R90, R89, and R88. When a gate is conducting, both biases are approximately the same; the

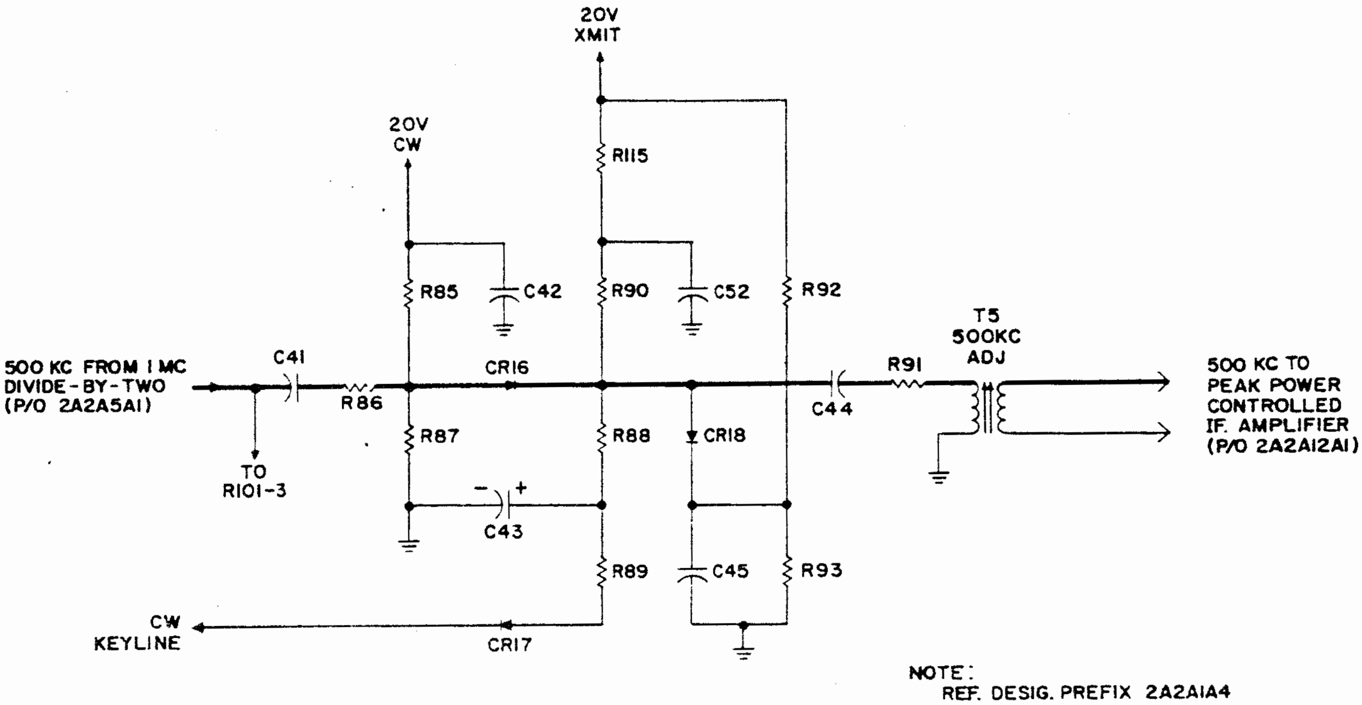


Figure 4-24. CW Carrier Reinsertion Gate, Simplified Schematic Diagram

ifference is the voltage drop caused by the orward resistance of the diode. Thus, when he transmitter is keyed, gate CR16 is forward-iased and conducts, allowing the 500-kc signal o pass. The 500-kc signal is coupled by :apacitor C44 to the primary of transformer T5. Transformer T5 couples the 500-kc signal o the peak power controlled if. amplifier cir-uit.

-133. In each mode of operation, except when ıe transmitter is keyed in the CW mode, the athode of gate CR16 is biased at approxi-ıately 17 vdc, which is also the anode bias ır gate CR18. The cathode of gate CR18 is iased at approximately 17 vdc also. This bias ; developed by voltage divider R115, R92, R93 ·om the 20 vdc applied from the Mode Selec-ır switch on the front panel. Therefore, gate R18 will be forward-biased and will conduct, fectively shorting gate CR16 to ground ırough capacitor C45. This insures that any akage through gate CR16 will be bypassed · ground when the transmitter is not being eyed in the CW mode of operation. When the ansmitter is keyed, the cathode bias of gate R16 drops instantaneously to 9.9 vdc; con-equently, the anode bias of gate CR18 is at e same level. Since the cathode of gate R18 is still biased at approximately 17, gate CR18 is now reverse-biased, removing the short from gate CR16.

4-134. CW CARRIER REINSERTION GATE, TEST DATA. Pertinent references and applicable test data for the CW carrier reinsertion gate circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic Assembly, Adjustments, Paragraph 5-28.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1.

(5) Common Electronic Circuits Test Set, TS-2135/WRC-1.

f. 500 KC Amplifiers/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

4-135. CW SIDETONE OSCILLATOR/GATE, FUNCTIONAL CIRCUIT DESCRIPTION. The CW sidetone oscillator/gate (figure 4-25) consists of a phase shift oscillator (Q8) and a gating diode (CR13). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, produce an audio tone that is applied to the receiver, enabling the operator to monitor the keying when operating in the CW mode of operation. The following paragraphs describe the operation of the CW sidetone oscillator/gate circuit in detail.

4-136. Since the signal between base and collector is reversed 180 degrees in phase, in a common emitter phase-shift oscillator an additional 180-degree phase shift is necessary to keep the feedback signal (from output to input) positive. The phase shift occurs in an RC network consisting of three sections, each contributing a 60-degree phase shift at the frequency of oscillation. In figure 4-25, the three RC sections are R68 and C36, R67 and C35, and conducts, allowing the audio output of phase-shift oscillator Q8 to pass. When ga CR13 conducts, both biases are approximat equal. The difference in biases is the volta and R66 and C34. When operating in the CV mode, operating voltage for this circuit is c veloped from the 20 vdc applied to voltage d der R65, R64, RT1 and emitter resistor R6 from the Mode Selector switch on the front panel. Thermistor RT1 stabilizes the circu for any ambient temperature changes. Volt divider R69, R70 determines the level of the audio tone (approximately 1 kc), produced b phase-shift oscillator Q8, and coupled to the cathode of gate CR13 by capacitor C37.

4-137. When the transmitter is not keyed fo CW operation, gate CR13 is reverse-biased a result of the positive 13.2 vdc on the catho and the positive 10 vdc on the anode. The tw biases are developed by voltage dividers R71, R74 and R75, R76 from the positive 20 v applied from the power supply on the main frame of the transmitter. Each time the CW key is depressed, ground is applied through diode CR12 to resistor R73. This causes the cathode bias to drop to 8.3 vdc. This instantaneous bias voltage is developed by the new voltage divider, consisting of R71 and the parallel combination of R72, R73, and R74. Since the anode of the diode is still biased at 10 vdc, gate CR13 becomes forward-biased

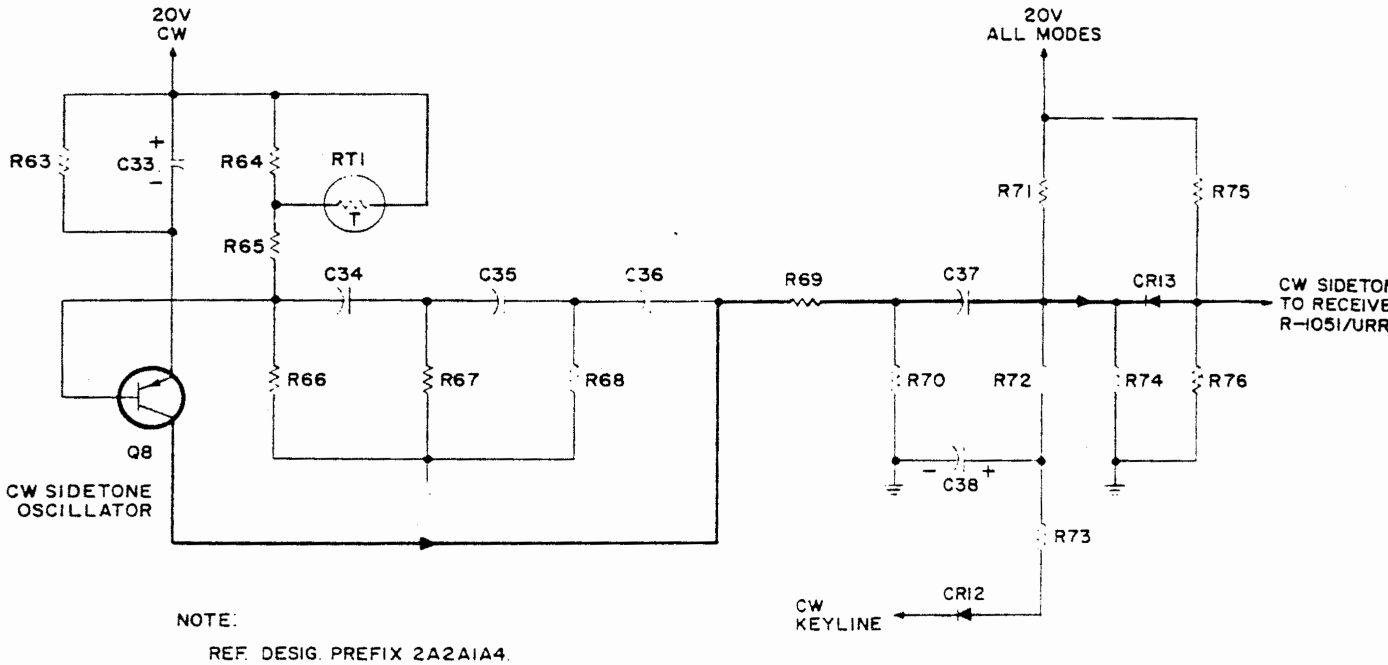


Figure 4-25. CW Sidetone Oscillator/Gate, Simplified Schematic Diagram

›p caused by the forward resistance of the ›de. The audio tone is applied to the receiv- where it is amplified in the audio amplifiers ‹l applied to the headset and the 600-ohm B audio output line. This tone allows the ›rator to monitor the keying when operating the CW mode of operation.

138. CW SIDETONE OSCILLATOR/GATE, ;ST DATA. Pertinent references and ap- cable test data for the CW sidetone oscil- or/gate circuit are as follows:

a. Radio Transmitter T-827/URT, Main ame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic sembly, Servicing Block Diagram, Figure 72.

c. Transmitter Mode Selector Electronic sembly, Schematic Diagram, Figure 5-6.

d. Required Test Equipment:

(1) Electronic Multimeter, CCVO-91CA.

(2) Frequency Meter, CAQI-524D.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1.

(5) Common Electronic Circuits Test t, TS-2135/WRC-1.

e. 500 KC Amplifiers/Gates and Sidetone scillator/Gates, Component and Test Point ›cation, Figure 5-38.

139. SIDETONE GATE, FUNCTIONAL RCUIT DESCRIPTION. Sidetone gate CR14 CR15 (figure 4-26), which forms a part of ransmitter Mode Selector Assembly 2A2A1, tes the audio intelligence to the receiver, abling the operator to monitor the transmis- ons. Gate CR14 is used during the USB, AM d FSK modes of operation. Gate CR15 is ed during the LSB mode of operation. Both tes are used during the ISB mode of opera- on. The following paragraphs describe the eration of the sidetone gate circuit in detail.

140. The audio applied to balanced modula- r A1, from Transmitter Audio Amplifier ectronic Assembly 2A2A2, is coupled to the ode of gate CR14 through coupling capacitor 39 and isolating resistor R77. This gate will

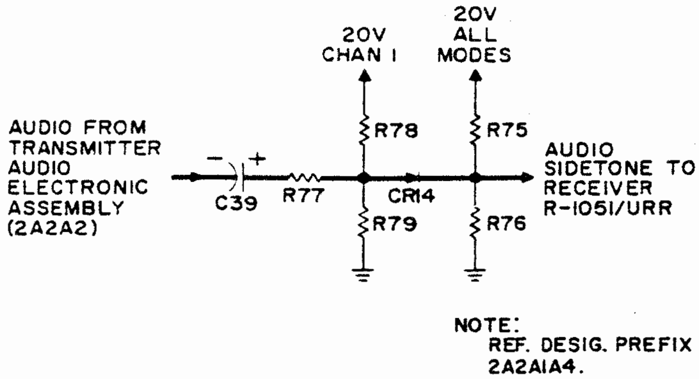


Figure 4-26. Sidetone Gate, Simplified Schematic Diagram

be forward-biased in the USB, AM, FSK, or ISB modes of operation by the positive 16.7 vdc on the anode and the positive 10 vdc on the cathode. The two biases are instantaneous voltages, which are developed from the positive 20 vdc applied to the voltage dividers R78, R79 and R75, R76 by the Mode Selector switch on the front panel. When gate CR14 is conducting, both biases are approximately equal. The difference in biases is the voltage drop caused by the forward re- sistance of the diode. The gate is forward- biased and will conduct, allowing the audio to pass. This audio is applied to the receiver, where it is amplified by the audio amplifier and applied to the headset and the USB 600-ohm audio output line. This tone allows the opera- tor to monitor the audio intelligence being transmitted.

4-141. Sidetone gate CR15 is identical to side- tone gate CR14 (figure 5-6). This gate is biased on during the LSB and ISB modes of operation. The audio to be gated by gate CR15 is applied from balanced modulator A2. The amplified output from the receiver is applied to the headset and LSB 600-ohm audio line for monitoring.

4-142. SIDETONE GATE, TEST DATA. Per- tinent references and applicable test data for the sidetone gate circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. 500 KC Amplifier/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

e. Required Test Equipment:

(1) Multimeter, AN/PSM-4.

(2) Cable Assembly, W1.

(3) Common Electronic Circuits Test Set, TS-2135/WRC-1.

4-143. AM CARRIER REINSERTION GATE, FUNCTIONAL CIRCUIT DESCRIPTION. The AM carrier reinsertion gate circuit (figure 4-27) consists of three gating circuits (CR19, CR20, CR21). These circuits, which form a part of Transmitter Mode Selector Electronic Assembly 2A2A1, gate the 500-kc local carrier into the peak power controlled if. amplifier circuit for reinsertion into the if. signal during the AM mode of operation. Gate CR20 is biased on in all modes of operation except AM, to prevent any leakage from this circuit, when it is not being used. Gate CR21 provides dc isolation between the two 20-vdc lines when gate CR20 is biased on. The following paragraphs describe the operation of the AM carrier reinsertion gate in detail.

4-144. The 500-kc signal from 1 mc divide-by-two circuit (part of 2A2A5A1) is applied to potentiometer R101. The potentiometer sets the percentage of modulation of the AM signal. The output from the potentiometer is coupled to voltage divider R95, R96 by capacitor C4(Gate CR19 is forward-biased during AM ope ation with an anode bias of 16.7 vdc and a cathode bias of 13.3 vdc. These two biases are instantaneous voltages which are develo by voltage dividers R94, R96 and R98, R97 fr the positive 20 vdc applied from the Mode Selector switch on the front panel. When a gate is conducting, both biases are approximately equal. The difference in biases is tl voltage drop caused by the forward resistan of the diode. Since gate CR19 is forward-biased, it will conduct, allowing the 500-kc signal to pass. The 500-kc signal is couple to the primary of transformer T5 by capacit C47. Transformer T5 couples the 500-kc ca rier to the peak power controlled if. amplifie for reinsertion into the if. signal.

4-145. In each mode of operation, the catho of gate CR19 is biased at 13.3 vdc. This bia also serves as the anode bias for gate CR20. Since gate CR21 is forward-biased only in Al operation, the anode will be open during the other modes of operation. Therefore, the cathode of gate CR20 is at zero voltage. As result, gate CR20 will be forward-biased anc will conduct, effectively shorting gate CR19 t ground through capacitor C49. This insures that any leakage through gate CR19 will be bypassed to ground whenever the transmitter is not being operated in the AM mode. When th transmitter is placed in the AM mode of operation, the anode of gate CR21 is biased at 20 vdc applied from the Mode Selector switch on the front panel. Since there is no voltage on

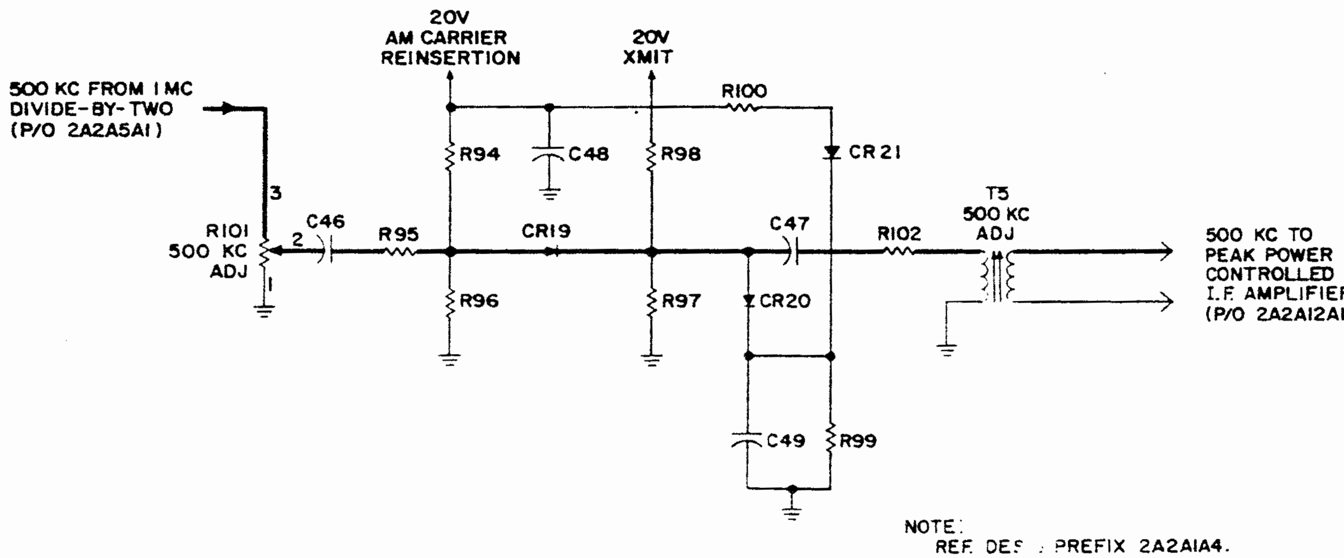


Figure 4-27. AM Carrier Reinsertion Gate, Simplified Schematic Diagram

e cathode of gate CR21, it is forward-biased d thus conducts. When gate CR21 conducts, e cathode of gate CR20 is biased at 16.5 vdc. is bias is developed by voltage divider R99, 100 from the positive 20 vdc applied from the ode Selector switch on the front panel. Since e anode of gate CR20 is biased at 13.3 vdc, will be reverse-biased and prevent the 500- signal from being applied to the 20-vdc pply lines.

146. AM CARRIER REINSERTION GATE, EST DATA. Pertinent references and appli- ble test data for the AM carrier reinsertion te circuit are as follows:

a. Radio Transmitter T-827/URT, Main ame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic ssembly, Servicing Block Diagram, Figure 72.

c. Transmitter Mode Selector Electronic ssembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic ssembly, Adjustments, Paragraph 5-28.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1.

(5) Common Electronic Circuit Test Set, 5-2135/WRC-1.

f. 500 KC Amplifiers/Gates and Sidetone scillator/Gates, Component and Test Point ocation, Figure 5-38.

147. CARRIER REINSERTION LEVEL

ONTROL FUNCTIONAL CIRCUIT DESCRIP- ON. The carrier reinsertion level control gure 4-28) consists of a gating circuit R100) and a variable attenuator circuit (S1). ese circuits, which form a part of Trans- tter Mode Selector Electronic Assembly 2A1, provide a pilot carrier for reinsertion o the if. signal to enable other radio sets th less stability than the AN/WRC-1 to re- ive transmissions from the T-827/URT. This rrier is used in these receivers for fre- ency-locking and demodulating. For normal use of the AN/WRC-1 the carrier is fully sup- pressed. These circuits provide a pilot carrier, when required, for the LSB, ISB, or USB modes of operation.

4-148. The 500-kc signal is coupled from the center of potentiometer R101 to voltage divider R110, R112 by capacitor C50. Potentiometer R101 is set so that the carrier is the same magnitude as the sideband when switch S1 is placed in the zero suppression position. The voltage divider limits the level of the 500-kc signal that is applied to the anode of gate CR100. During the USB, ISB, or LSB modes of operation, gate CR100 is forward-biased by the positive 16.7 vdc anode bias and the posi- tive 13.3 vdc cathode bias. The two biases are instantaneous voltages, which are developed by voltage dividers R110, R111 and R108, R109 from the positive 20 vdc applied through con- tacts 11, and 10, 9, or 8 of switch S1. When gate CR100 is conducting, both biases are approx- imately equal. The difference in biases is the voltage drop caused by the forward resistance of the diode. Since gate CR100 is forward- biased, it will conduct, allowing the 500-kc signal to pass. The output from gate CR100 is coupled to one of three attenuator circuits by capacitor C51. The attenuator circuit used depends upon the position of switch S1. When switch S1 is set at the 0 DB SUPPR, 10 DB SUPPR, or 20 DB SUPPR position, the 500-kc signal is applied through the respective atten- uator network and contacts 2, 3, or 4 and 5 of switch S1 to transformer T5. Transformer T5 couples the 500-kc signal to the peak power controlled if. amplifier for reinsertion into the if. signal.

4-149. CARRIER REINSERTION LEVEL CONTROL, TEST DATA. Pertinent references and applicable test data for the carrier rein- sertion level control circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram, Figure 4-72.

c. Transmitter Mode Selector Electronic Assembly, Schematic Diagram, Figure 5-6.

d. Transmitter Mode Selector Electronic Assembly, Adjustments, Paragraph 5-28.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

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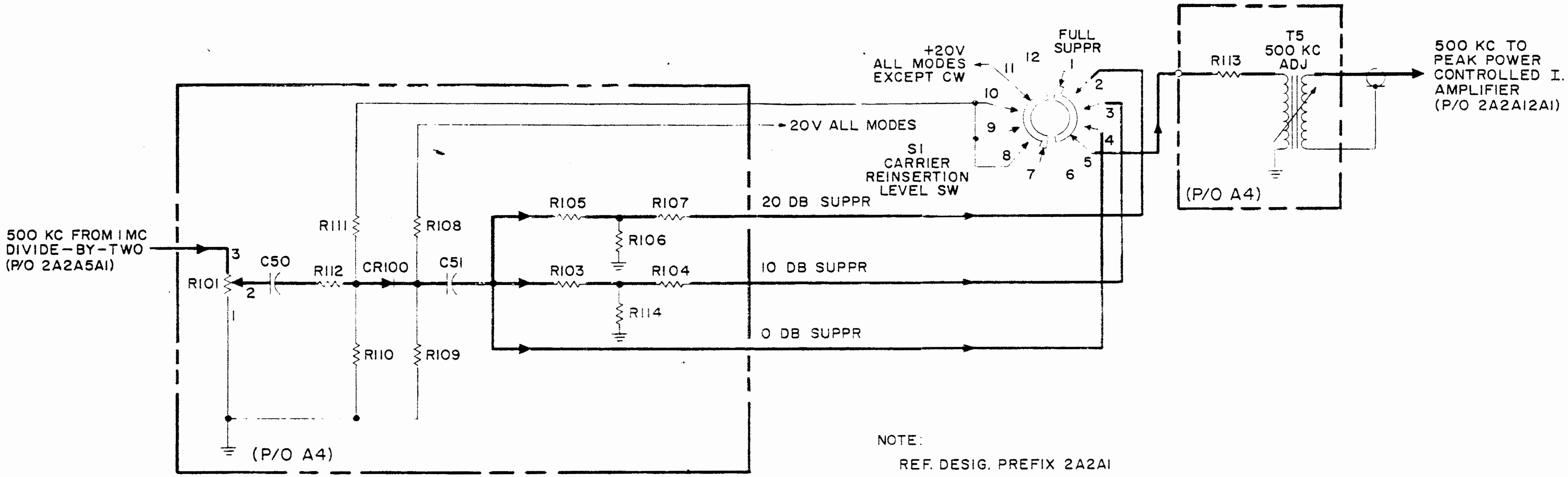


Figure 4-28. Carrier Reinsertion Level Control, Simplified Schematic Diagram

(2) Electronic Multimeter, CCVO-91CA.

(3) Multimeter, AN/PSM-4.

(4) Cable Assembly, W1.

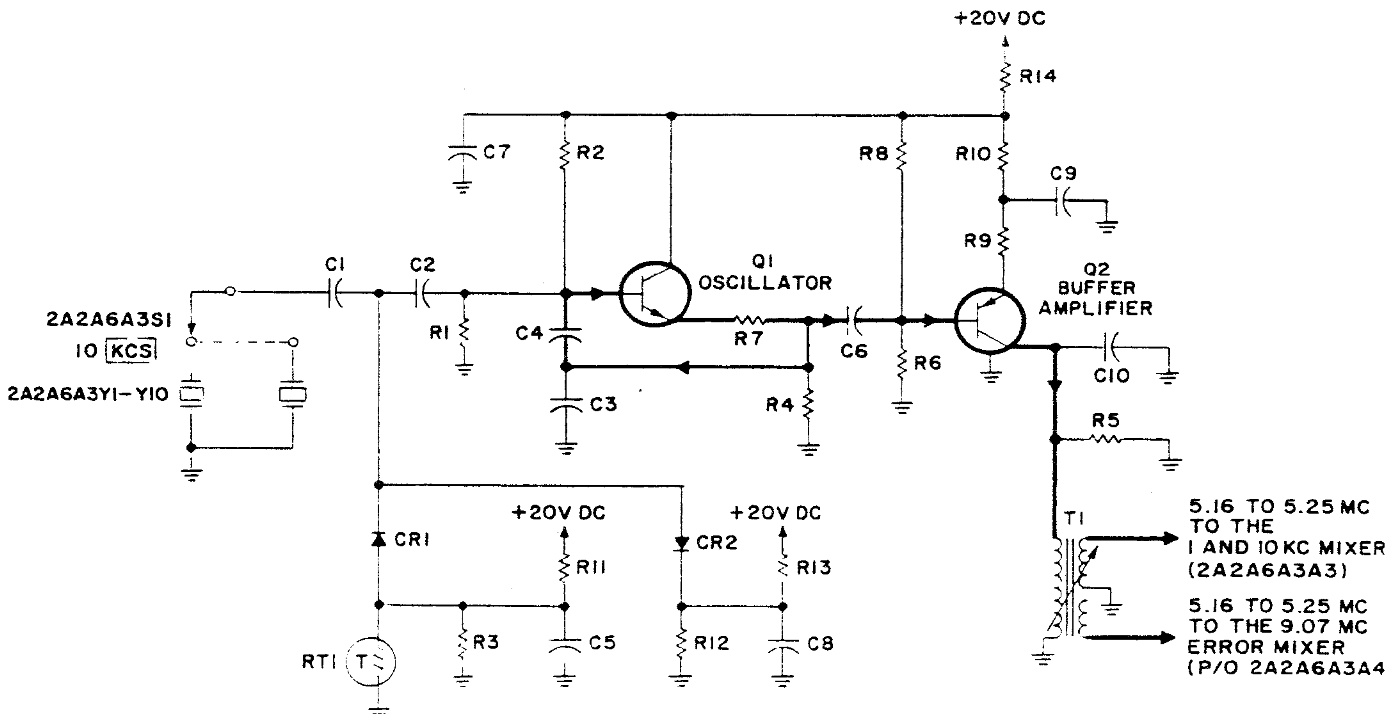
(5) Common Electric Circuits Test Set, TS-2135/WRC-1.

f. 500 KC Amplifiers/Gates and Sidetone Oscillator/Gates, Component and Test Point Location, Figure 5-38.

g. Transmitter Mode Selector Electronic Assembly, Left Side View, Component Location, Figure 5-34.

4-150. 5.16 TO 5.25 MC OSCILLATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 5.16 to 5.25 mc oscillator (figure 4-29) consists of 10 kc (KCS) crystal switch (2A2A6A3S1), a limiter circuit (CR1, CR2), an oscillator (Q1), and a buffer amplifier (Q2). These circuits, which form a part of 1 and 10 KC Synthesizer Electronic Subassembly 2A2A6A3, produce one of ten outputs in 10-kc steps over the frequency range of 5.16 through 5.25 mc for use in 1 and 10 kc output mixer 2A2A6A3A3, and the 9.07-mc error mixer (part of 2A2A6A3A4). These circuits function in all modes of operation. The following paragraphs describe the operation of the 5.16 to 5.25 mc oscillator in detail.

4-151. The operating frequency of the modified crystal-controlled Colpitts (Pierce) oscillator (Q1) is determined by the selection of any one of ten crystals (2A2A6A3Y1 through Y10) by switch 2A2A6A3S1. Selection is accomplished by positioning the 10 kc (KCS) control on the front panel. Operating voltage for the oscillator is derived from main frame power supply 2A2A8. Base bias for oscillator Q1 is developed by voltage divider R1, R2. The output of oscillator Q1 is controlled by diodes CR1 and CR2. The negative-going limit of the signal is established by the anode bias on diode CR1 (developed by voltage divider R3, R11, RT1), minus the drop of diode CR1. The positive-going limit of the signal is established by the cathode bias on diode CR2 (developed by voltage divider R12, R13) plus the drop of diode CR2. Therefore, the peak-to-peak amplitude of the signal is limited by the established dc reference levels. As the temperature of the



NOTE:
UNLESS OTHERWISE NOTED,
REF. DESIG. PREFIX IS 2A2A6A3A1.

Figure 4-29. 5.16 to 5.25 MC Oscillator, Simplified Schematic Diagram circuit varies, the forward drop across diodes CR1 and CR2 varies. This would result in variations in the signal amplitude without temperature compensation. Thermistor RT1 varies the anode bias of CR1 in accordance with temperature changes. Therefore, the negative-going limit of the signal is shifted so that the limiting region is constant. This ensures that the amplitude of the signal does not vary with changes in temperature. Capacitors C5 and C8 are rf bypass capacitors. Capacitor C2 is used for dc blocking and is also used with capacitors C1, C3, and C4 to form the required feedback network. Resistor R7 provides degeneration to increase the stability of oscillator Q1. The output of oscillator Q1 is developed across emitter resistor R4 and is coupled to the base of buffer amplifier Q2 by capacitor C6.

4-152. Voltage divider R6, R8 develops the base bias for buffer amplifier Q2 from the positive 20 vdc. A resonant circuit consisting of the primary of transformer T1 and capacitor C10 provides the collector load for the amplifier. Resistor R5 is used to load the tank circuit to provide uniform gain over the range of frequencies developed by the oscillator. Resistor R9, in the emitter circuit, provides degenerative feedback to stabilize the gain and increase the input impedance of amplifier Q2, thereby preventing loading of oscillator Q1. Resistor R10 is the emitter bias resistor, which is rf bypassed by capacitor C9. Resistor R14 and capacitor C7 provide decoupling for oscillator Q1 and buffer amplifier Q2. The output of amplifier Q2 is coupled to the 1 and 10 kc mixer circuit and to the 9.07 mc error mixer circuit by the secondary of transformer T1.

4-153. 5.16 TO 5.25 MC OSCILLATOR, TEST DATA. Pertinent references and applicable test data for the 5.16 to 5.25 mc oscillator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 and 10 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-78.

c. 1 and 10 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-12.

d. 5.16 to 5.25 MC Oscillator, Component and Test Point Location, Figure 5-91.

e. Required Test Equipment:

(1) Frequency Meter, CAQI-524D.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Multimeter, AN/PSM-4.

(5) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-28 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for alignment for 5.16 to 5.25 M oscillator adjustment procedure.

4-154. 1.850 TO 1.859 MC OSCILLATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 1.850 to 1.859 mc oscillator (figure 4-30) consists of 1 kc (KCS) crystal switch (2A2A6A3S2), a limiter (CR1, CR2), an oscillator (Q1), and a buffer amplifier (Q2). These circuits, which form a part of 1 and 10 KC Synthesizer Electronic Subassembly 2A2A6A3, produce one of ten outputs, in 1-kc steps, over the frequency range of 1.850 through 1.859 mc for use in 1 and 10 kc output mixer 2A2A6A3A3, and the 9.07 mc error mixer (part of 2A2A6A3A4). These circuits function in all modes of operation. The operation of the 1.850 to 1.859 mc oscillator is identical to that of the 5.16 to 5.25 mc oscillator. (Refer to paragraphs 4-149 and 4-150 for details of circuit operation.)

4-155. 1.850 TO 1.859 MC OSCILLATOR, TEST DATA. Pertinent references and applicable test data for the 1.850 to 1.859 mc oscillator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 and 10 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-78.

c. 1 and 10 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-12.

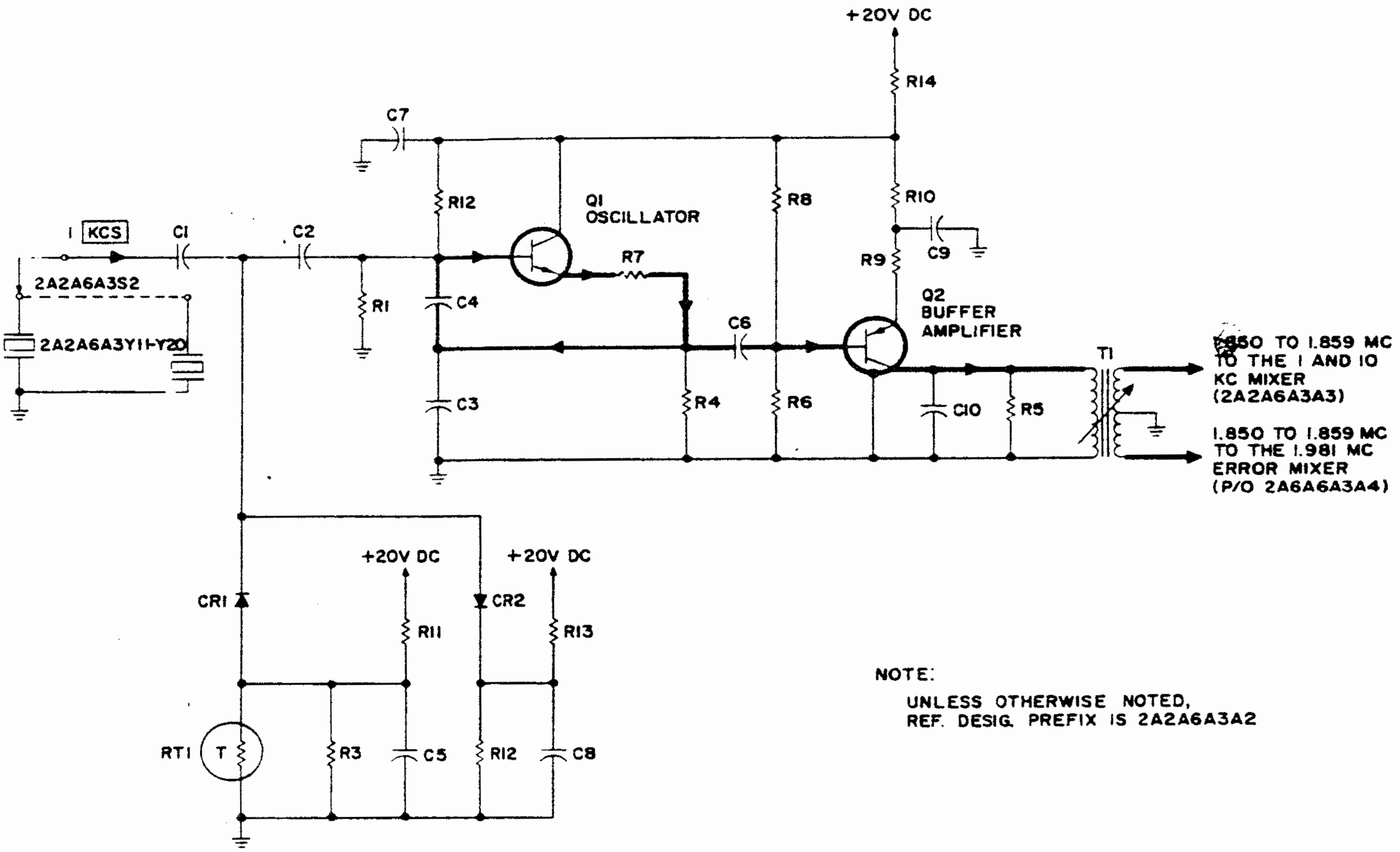


Figure 4-30. 1.850 to 1.859 MC Oscillator, Simplified Schematic Diagram

d. 1.850 to 1.859 MC Oscillator, Component and Test Point Location, Figure 5-92.

e. Required Test Equipment:

(1) Frequency Meter, CAQI-524D.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Multimeter, AN/PSM-4.

(5) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-28 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for alignment for 1.850 to 1.859 MC oscillator adjustment procedures.

4-156. 1 AND 10 KC MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The 1 and 10 kc mixer circuit (figure 4-31) consists of a mixer (Q11) and a four-section filter (C48-L5, C49-L6, C51-L7, and C54 and the primary of transformer T3 with coupling capacitors C56, C50 and C52). A noise blanker control (Q12) is also included, but is not used with the AN/WRC-1 system. These circuits, which form a part of 1 and 10 KC Synthesizer Electronic Subassembly 2A2A6A3, subtractively mix the signal from the 1.850 to 1.859 mc oscillator with the signal from the 5.16 to 5.25 mc oscillator, producing the 1 and 10 kc injection signal (3.301 to 3.400 mc in 1-kc steps) for use in the low frequency mixer. The following paragraphs describe the operation of this circuit in detail.

4-157. The signal from the 1.850 to 1.859 mc oscillator is applied through resistor 2A2A6A3A2R16 to resistor 2A2A6A3A1R16. The signal from the 5.16 to 5.25 mc oscillator is also applied to resistor 2A2A6A3A1R16 through capacitor 2A2A6A3A1C11. This capacitor provides a low impedance to the 5.16-to 5.25-mc signal and a high impedance to the 1.850-to-1.859-mc signal; therefore, the 5.16 to 5.25 mc oscillator will not load the 1.850 to 1.859 mc signal. The two input signals are coupled from resistor 2A2A6A3A1R16 through capacitor C55 to the base of mixer Q11. The base bias is provided by voltage divider R47, R54. Resistor R52 provides a small amount of degeneration to improve the stability of mixer Q11. Resistor R48 is the emitter bias resistor, which is rf bypassed by capacitor C47. Resistor R49 and capacitor C46 provide decoupling for mixer Q11. The output circuit of mixer Q11 is four-section filter. The filter has a bandwidth of 100 kc (3.3 to 3.4 mc) and sufficient selectivity to attenuate any frequency outside this band. Capacitors C56, C50, and C52 are an integral part of the filter and couple the signal between sections of the filter; therefore, the four section filter will pass only the difference of the 1.850-to-1.859-mc and 5.16-to-5.25-mc signals (3.301 to 3.400 mc, in 1 kc steps). The signal from the four-section filter is coupled through transformer T3 and applied to the low frequency mixer.

4-158. If used, noise blanker control Q12 functions as a switch that gates the output of the 1 and 10 kc mixer at a rate and for a duration determined by the pulse received. During the absence of a pulse, diode CR7 references the primary of transformer T3 at a level of about 18.8 vdc. During this time, noise blanker control Q12 is not conducting; therefore, the emitter and collector will be at about 20 vdc and 18.8 vdc, respectively. When a negative pulse arrives at the base of noise blanker control Q12, the transistor is driven into saturation, creating a low impedance from the junction of capacitors C52 and C54 to ac ground for the duration of the pulse. This means that the signal at the junction of capacitors C52 and C54 is essentially shorted to ac ground for the duration of the pulse.

4-159. 1 AND 10 KC MIXER, TEST DATA. Pertinent references and applicable test data for the 1 and 10 kc mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 and 10 KC Synthesizer, Electronic Subassembly, Servicing Block Diagram, Figure 4-78.

c. 1 and 10 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-12.

d. 1 and 10 KC Synthesizer Output, Component and Test Point Location, Figure 5-94.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

(6) Multimeter, AN/PSM-4.

f. Refer to paragraph 3-28 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for alignment of 1 and 10 kc mixer adjustment procedures.

4-160. 4.553 TO 5.453 MC OSCILLATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 4.553 to 5.453 mc oscillator (figure 4-32) consists of 100 kc (KCS) crystal switch (2A2A6A2S1), a limiter (CR1, CR2), an oscillator (Q1), and an emitter follower (Q2). These circuits, which form a part of 100 KC Synthesizer Electronic Subassembly 2A2A6A2, produce one of ten outputs in 100-kc steps over the frequency range of 4.553 through 5.453 mc for use in hi-band/lo-band mixer/amplifier 2A2A6A2A4 and 10.747 mc mixer 2A2A6A2A2. These circuits are used in all modes of operation. The following paragraphs describe the operation of the 4.553 to 5.453 mc oscillator in detail.

4-161. The operating voltage for the 4.553 to 5.453 mc oscillator is derived from main frame power supply 2A2A8. Resistor R12 and capacitor C8 provide decoupling to prevent any interaction with other circuits connected to the 20 vdc supply line. Base bias for oscillator Q1 is developed by voltage divider R5, R7. The output frequency of oscillator Q1 is determined by the setting of the 100 kc (KCS) control (2A2A6A2S1) on the front panel. This switch (2A2A6A2S1) connects the correct crystal (2A2A6A2Y1 through Y10) into the circuit of oscillator Q1 in accordance with the desired 100-kc digit of the operating frequency. The output of oscillator Q1 is controlled by diodes

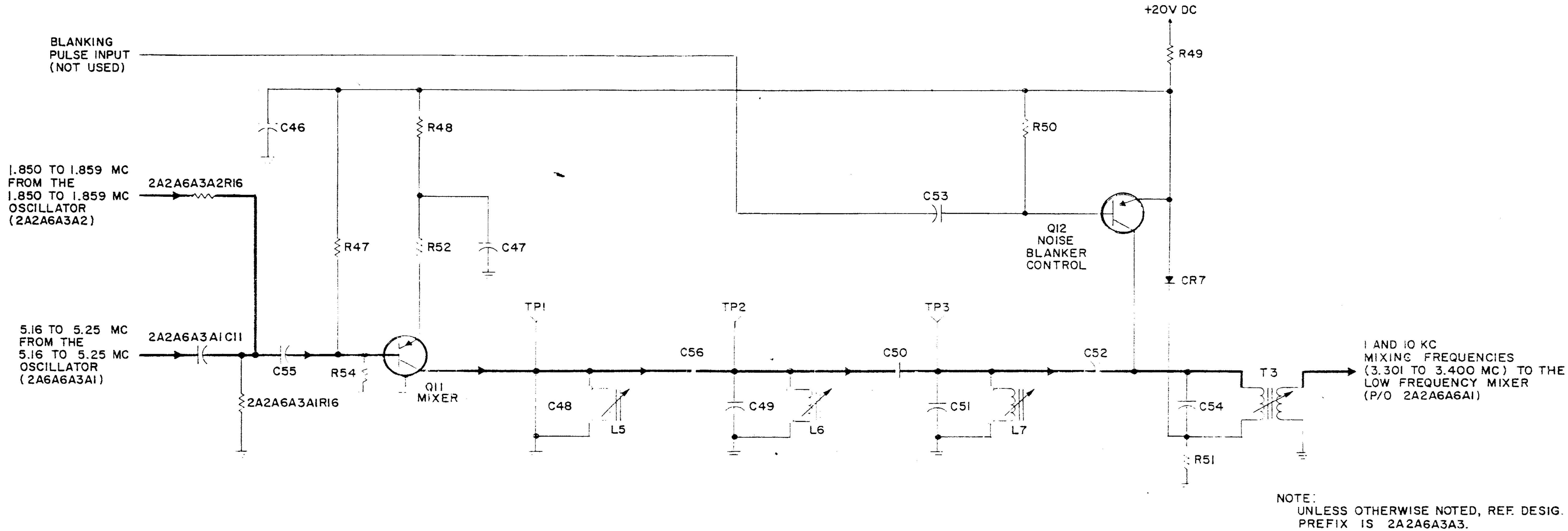


Figure 4-31. 1 and 10 KC Mixer, Simplified Schematic Diagram

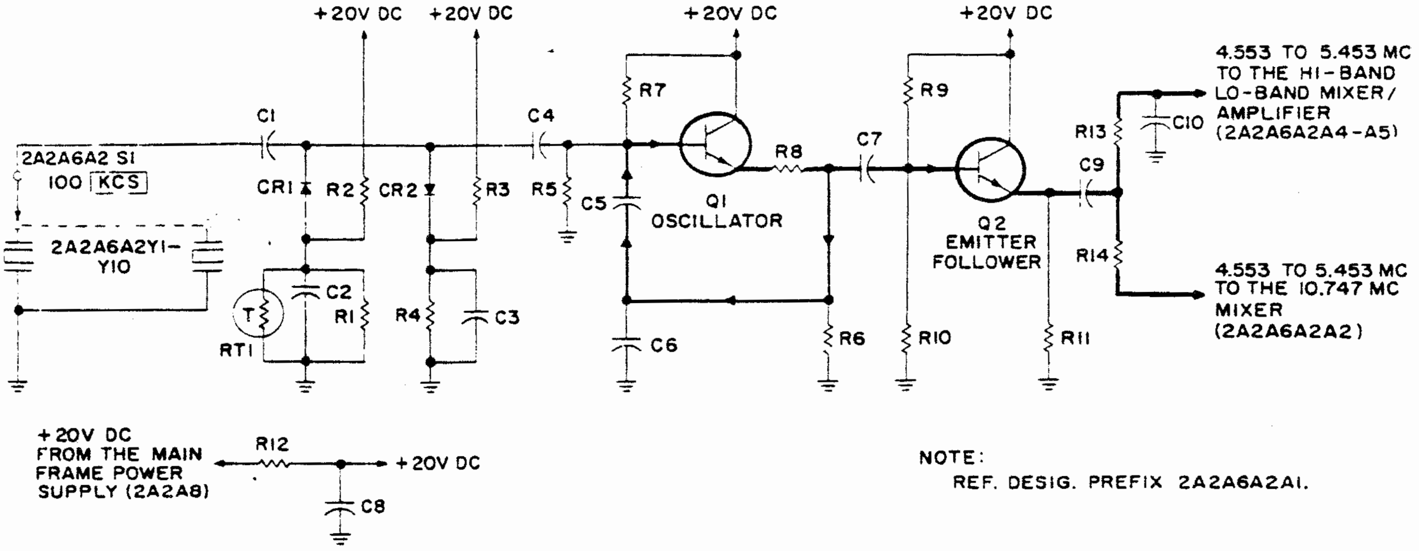


Figure 4-32. 4.553 to 5.453 MC Oscillator, Simplified Schematic Diagram

CR1 and CR2. The negative-going limit of the signal is established by the anode bias on diode CR1 (developed by voltage divider R1, R2, RT1) minus the drop of diode CR1. The positive-going limit of the signal is established by the cathode bias on diode CR2 (developed by voltage divider R3, R4) plus the drop of diode CR2. Therefore, the peak-to-peak amplitude of the signal is limited by the established dc reference levels. As the temperature of the circuit varies, the forward drop of diodes CR1 and CR2 varies. This would result in variations in the signal amplitude without temperature compensation. Thermistor RT1 varies the anode bias of diode CR1 in accordance with temperature changes. Therefore, the negative-going limit of the signal is shifted so that the limiting region is constant. This ensures that the amplitude of the signal does not vary with changes in temperature. Capacitors C2 and C3 are rf bypass capacitors. Capacitor C4 is used for dc blocking and is also used with capacitors C1, C5, and C6 to form the required feedback network. Resistor R8 provides degeneration to increase the stability of oscillator Q1. The output of oscillator Q1 is developed across emitter resistor R6 and is coupled to the base of emitter follower Q2 by capacitor C7.

4-162. The base bias for emitter follower Q2 is developed by voltage divider R9, R10 from the 20 vdc. Emitter follower Q2 is used to isolate the oscillator from the succeeding circuits. The output of emitter follower Q2 is developed across emitter resistor R11 and coupled to the hi-band/lo-band mixer/amplifier and to the 10.747 mc mixer by capacitor C9. Resistors R13 and R14 are isolating resistors. Capacitor C10 provides a low impedance to ground for the other signals used in the hi-band/lo-band mixer/amplifier, preventing these signals from being coupled into the 10.747 mc mixer.

4-163. 4.553 to 5.453 MC OSCILLATOR, TEST DATA. Pertinent references and applicable test data for the 4.553 to 5.453 mc oscillator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 100 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-79.

c. 100 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-11.

d. 4.553 MC to 5.453 MC Oscillator, Component Location, Figure 5-81.

e. Required Test Equipment:

(1) Frequency Meter, CAQI-524D.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

(6) Multimeter AN/PSM-4.

4-164. HI-BAND/LO-BAND MIXER/AMPLIFIER FUNCTIONAL CIRCUIT DESCRIPTION. The hi-band/lo-band mixer/amplifier (figure 4-33) consists of two mixers (A4Q1 and A4Q2), two trap amplifiers (A4Q3 and A4Q4), and an emitter follower (A5Q1). These circuits, which form a part of 100 KC Synthesizer Electronic Subassembly 2A2A6A2, produce either a high (hi) band of injection frequencies (32.4 to 33.3 mc) or a low (lo) band of injection frequencies (22.4 to 23.3 mc), which is used in the mid-frequency mixer of RF Translator Electronic Subassembly 2A2A6A6. The output of these circuits is also used in 10.747 mc mixer agc circuit 2A2A6A2A5 to develop the agc voltage which controls the gain of 10.747 mc mixer 2A2A6A2A2. These circuits are used in all modes of operation. The following paragraphs describe the operation of the hi-band/lo-band mixer/amplifier in detail.

4-165. Only half of the hi-band/lo-band mixer/amplifier circuits are on at any one time, depending on whether the hi (32.4 to 33.3 mc) or lo (22.4 to 23.3 mc) band is required for mixing in RF Translator Electronic Subassembly 2A2A6A6. The hi-band circuits will be discussed first. Unless otherwise noted, all components referenced are located on the A4 assembly.

4-166. The 27.847 mc output from the 17.847/27.847 mc mixer is coupled to the base of mixer Q1 by capacitor C22. The output from the 4.553 to 5.453 mc oscillator is coupled to the emitter of mixer Q1 by capacitor C1. When the hi/lo band control line is at ground potential, base bias will be provided for mixer Q1 and trap amplifier Q3 by voltage divider R4, R6 and voltage divider R13, R14, respectively. Resistor R1 is the emitter resistor. Capacitor C4 is an rf bypass capacitor. At the same time, mixer Q2 and trap amplifier Q4 will be rendered inoperative by the ground potentials applied to the emitters and base bias circuits from the hi/lo band control line. The output of mixer Q1 is a frequency in the 32.4-to-33.3-mc band. All other products of the mixer, except for a small amount of the 27.847-mc component, are eliminated by the triple-tuned filter composed of inductors L1 and L2, transformer T1 and capacitors C7, C10, C11, C14, and C15. From the triple-tuned filter, the signal is coupled through capacitor C18 to the base of amplifier Q3. The emitter circuit of trap amplifier Q3 (capacitor C20 and inductor L3) is parallel-tuned to 27.847 mc. At 27.847 mc, the trap provides degeneration to effectively eliminate the 27.847-mc component from the output signal. Resistor R11 and capacitor C27 provide decoupling for trap amplifier Q3. Resistor R17 is the emitter bias resistor, which is rf bypassed by capacitor C23. The output of trap amplifier Q3 is coupled by capacitor A5C1 to the base of emitter follower A5Q1. The output of emitter follower A5Q1 is also applied to 10.747 mc mixer AGC 2A2A6A2A5.

4-167. The lo-band circuits are identical to the hi-band circuits. When the hi/lo band control line is at 20 vdc, operating voltages are applied to the emitter and bases of mixer Q2 and trap amplifier Q4. At the same time, the 20 vdc is applied to the bases of mixer Q1 and trap amplifier Q3, thereby providing back bias for the transistors, since the emitters are also at 20 vdc. The 17.847-mc output from the 17.847 mc mixer is coupled to the base of mixer Q2 by capacitor C6. The output from the 4.553 to 5.453 mc oscillator is coupled to the emitter of mixer Q2 by capacitor C2. The output of mixer Q2 is a frequency in the 22.4-to-23.3-mc band. All other products of the mixer, except for a small amount of 17.847-mc component, are eliminated by the triple-tuned filter composed of inductors L4 and L5, transformer T2, and capacitors C9, C12, C13 and C16, and C17. From the triple-tuned filter, the signal is coupled by capacitor C19 to the base of trap amplifier Q4. The emitter circuit of trap amplifier Q4 is parallel-tuned to 17.847 mc to eliminate the 17.847-mc signal. The output of trap amplifier Q4 is coupled by capacitor A5C2 to the base of emitter follower A5Q1. The output of emitter follower A5Q1 is applied to 10.747 mc mixer AGC 2A2A6A2A5 and the mid-frequency mixer in the RF Translator Electronic Subassembly 2A2A6A6.

4-168. HI-BAND/LO-BAND MIXER/AMPLIFIER, TEST DATA. Pertinent references and applicable test data for the hi-band/lo-band mixer/amplifier circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Figure 5-5.

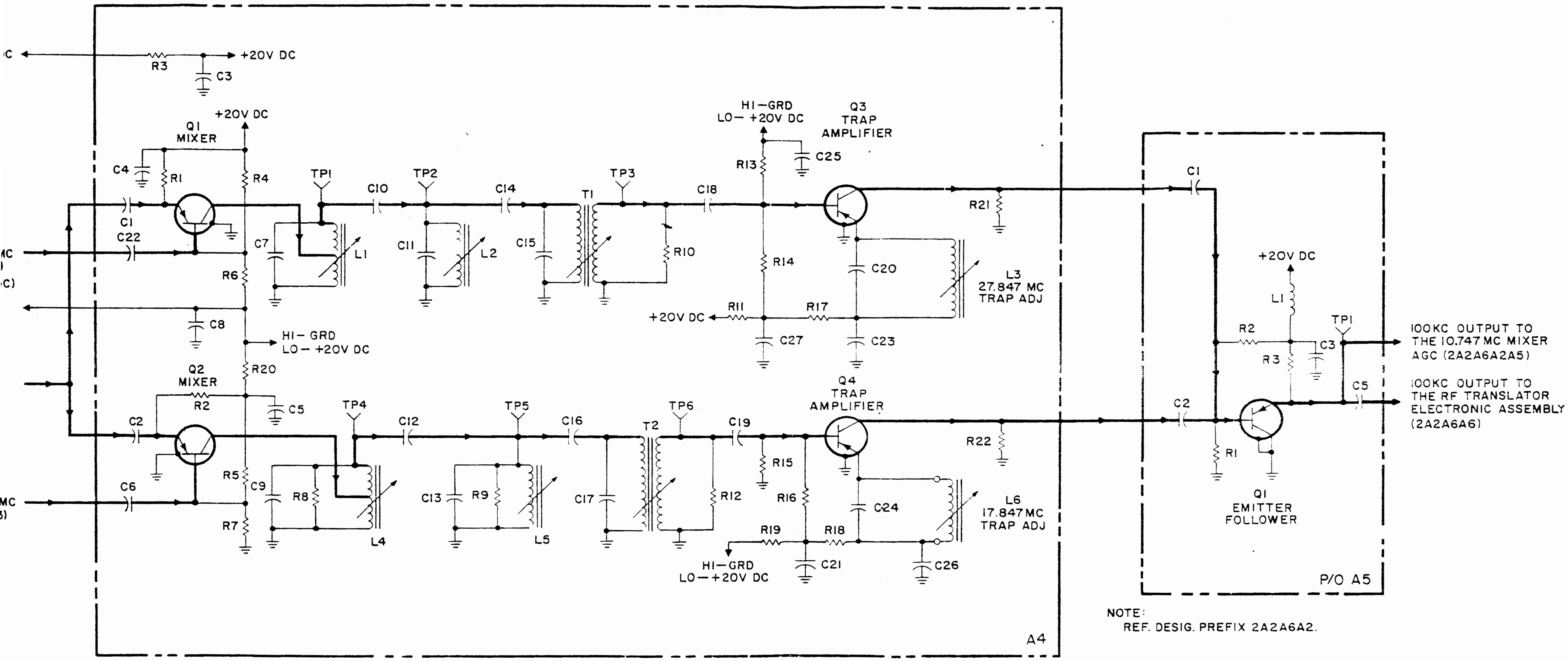
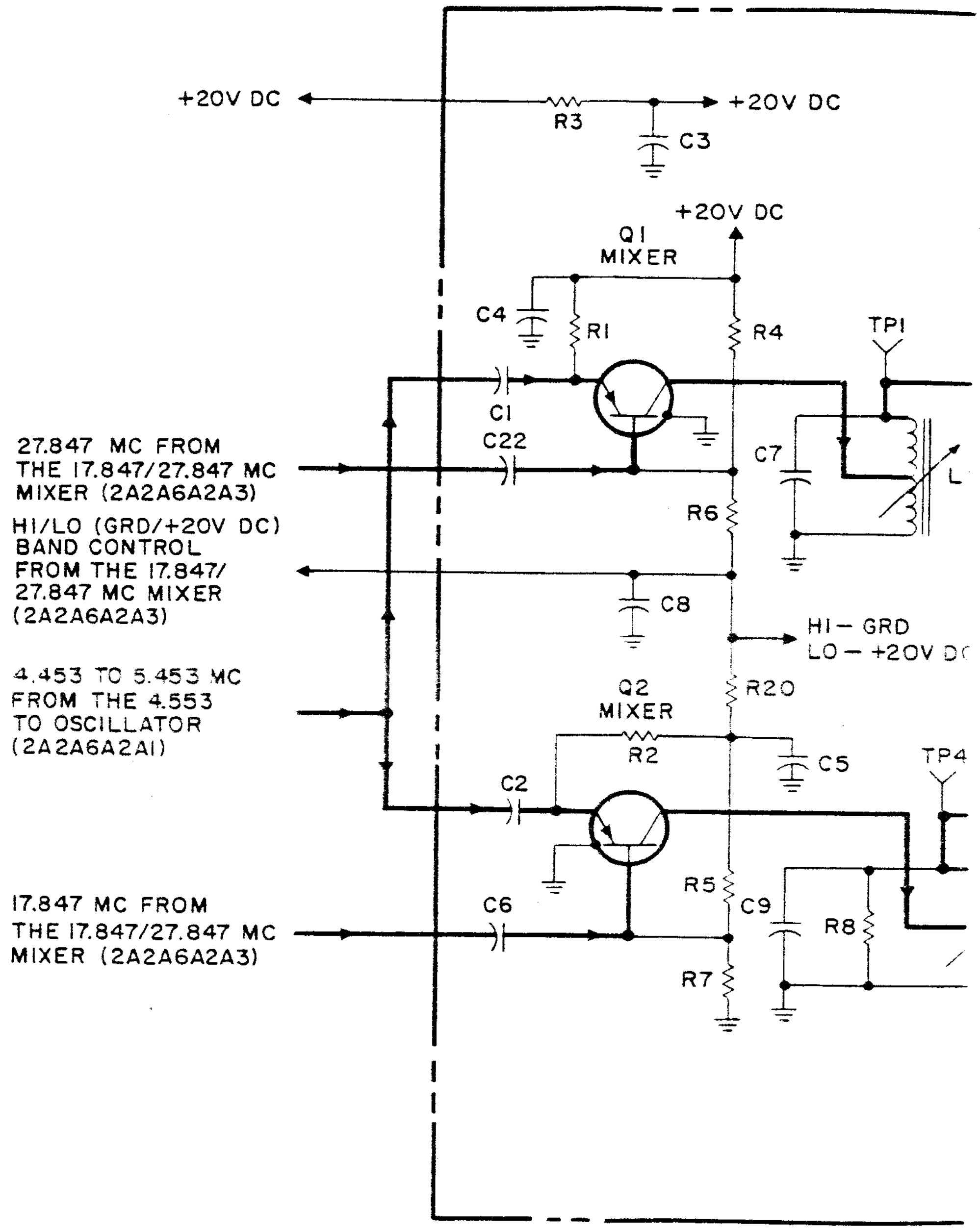


Figure 4-33. Hi-Band/Lo-Band Mixer/Amplifier, Simplified Schematic Diagram


+20V DC
R3
+20V DC
C3
+20V DC
Q1
MIXER
C4
R1
R4
TP1
C1
C22
27.847 MC FROM
THE 17.847/27.847 MC
MIXER (2A2A6A2A3)
C7
L
HI/LO (GRD/+20V DC)
BAND CONTROL
FROM THE 17.847/
27.847 MC MIXER
(2A2A6A2A3)
R6
C8
HI – GRD
LO – +20V DC
4.453 TO 5.453 MC
FROM THE 4.553
TO OSCILLATOR
(2A2A6A2A1)
Q2
MIXER
R20
R2
C5
TP4
C2
R5
C9
R8
17.847 MC FROM
THE 17.847/27.847 MC
MIXER (2A2A6A2A3)
C6
R7

157/158

equency mixer. Capacitor C28 couples the gnal from emitter resistor R16 to the high- equency mixer. Resistors R17 and R18 are olation resistors.

172. MC OSCILLATOR, TEST DATA. Per- ent references and applicable test data for e mc oscillator are as follows:

a. Radio Transmitter T-827/URT, Main ame, Schematic Diagram, Figure 5-5.

b. 1 MC Synthesizer Electronic Subassem- y, Servicing Block Diagram, Figure 4-80.

c. 1 MC Synthesizer Electronic Subassem- y, Schematic Diagram, Figure 5-10.

d. MC Oscillator, Component and Test- int Location, Figure 5-77.

e. Required Test Equipment:

(1) Frequency Meter, CAQI-524D.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Heterodyne Voltmeter, Bruel and er, 2005.

(5) Translator/Synthesizer Test Set, -2133/WRC-1.

(6) Multimeter, AN/PSM-4.

.73. MC SPECTRUM GENERATOR, NCTIONAL CIRCUIT DESCRIPTION. The spectrum generator (figure 4-35) consists hree shaper amplifiers (Q1, Q2, and Q3). ese circuits, which form a part of 1 MC thesizer Electronic Subassembly 2A2A6A1, vide a spectrum of frequencies from 1 to mc in 1-mc steps for use in the mc error ker. The following paragraphs describe the ration of the circuits in detail.

74. These circuits operate from the posi- e 10 vdc derived by Zener diode CR1 and ies resistor R1 from the positive 20 vdc. e 1-mc input is applied to inductor L2 ough resistor R33. Resistor R33 prevents ding of the 5 mc divide-by-five circuit. In- tor L2 functions as an autotransformer, sing the level of the 1-mc signal and apply- ing it to the diode clipper consisting of diode CR3 and resistor R5. Inductor L2 is tuned to 1 mc by capacitor C3. The diode clipper re- moves the positive portion of the 1-mc signal. The remaining negative portion is coupled through capacitor C2 to the base of shaper am- plifier Q1, driving it into saturation. Diode CR2 protects shaper amplifier Q1 against ex- cessive reverse bias on the base-emitter junction. When the base voltage attempts to go more positive than the emitter voltage, diode CR2 will be forward-biased, thereby clamping the base voltage. The emitter voltage is deter- mined by voltage divider R3, R4 and by the average current drawn by shaper amplifier Q1. The output of shaper amplifier Q1 is a positive- going waveform with a fast rise time. This output is developed across collector resistor R6 and applied through capacitor C5 to the base of shaper amplifier Q2. The positive-going waveform drives shaper amplifier Q2 into saturation, producing a negative-going wave- form at the collector of Q2. Capacitor C6 pro- vides emitter peaking, which results in an overshoot on the output waveform. The output of shaper amplifier Q2 is coupled through capacitor C8 to the base of shaper amplifier Q3. The output of shaper amplifier Q2 is dif- ferentiated at the base of shaper amplifier Q3 by the time constant formed by the output im- pedance of shaper amplifier Q2, capacitor C8, and the input impedance of shaper amplifier Q3. The negative-going portion of this signal drives shaper amplifier Q3 into saturation. Diode CR4, like diode CR2, is a protective device which is also used to clamp the positive portions of the input signal. Resistor R15 limits the collector current of shaper amplifier Q3 and minimizes the variations in the satura- tion characteristics of the amplifier. The out- put of shaper amplifier Q3 is developed across an LR differentiating network consisting of resistor R15 and inductor L3. The output of shaper amplifier Q3 is taken across inductor L3. The network consisting of diode CR5, resistor R17 and resistor R22 forms a diode clipper circuit that eliminates the negative portion of the output across inductor L3. Re- sistors R17 and R22 also form an attenuator with the output taken across resistor R22. The output obtained is a positive pulse that pro- vides a uniform spectrum from 1 mc to 25 mc. This output is applied to the mc error mixer.

4-175. MC SPECTRUM GENERATOR, TEST DATA. Pertinent references and applicable

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b. 100 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-79.

c. 100 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-11.

d. Hi-Band/Lo-Band Mixer/Amplifier, Component and Test Point Location, Figure 5-83.

e. 10.747 MC Mixer AGC, Component and Test Point Location, Figure 5-89.

f. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

(6) Multimeter, AN/PSM-4.

g. Refer to paragraph 3-32 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for alignment of hi-band/lo-band mixer/amplifier adjustment procedures.

4-169. MC OSCILLATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The mc oscillator (figure 4-34) consists of an oscillator (Q1), a wideband amplifier (Q2) and two emitter followers (Q3 and Q4). These circuits, which form a part of 1 MC Synthesizer Electronic Subassembly 2A2A6A1, provide 17 discrete frequencies (2.5 to 23.5 mc) for use in the high frequency mixer. The following paragraphs describe the operation of the mc oscillator in detail.

4-170. Oscillator Q1 is a modified, crystal-controlled Colpitts (Pierce) oscillator used with crystals 2A2A6A1Y1 through 2A2A6A1Y17 to cover a frequency range from 2.5 to 23 5 mc in 17 discrete steps. Due to the wide frequency range required, it is necessary to select a capacitor (2A2A6A1C1 through 2A2A6A1C17) in the feedback network for each crystal and thus provide a uniform output level. The oscillator feedback network consists of capacitors C21, C24, and 2A2A6A1C1 through 2A2A6A1C17, voltage-variable capacitor CR3 and a crysta (2A2A6A1Y1 through 2A2A6A1Y17). Voltage variable capacitor CR3 provides the necessa control for correcting any error in the frequ cy of oscillator Q1. Resistor R2 references voltage variable capacitor CR3 to 20 vdc. T error voltage from the error detector/ampli fier passes through resistor R1 to voltage variable capacitor CR3, where it changes the capacity and the resonant frequency of the ci cuit until the circuit resonates at the correct frequency. Capacitor C21 compensates for variations in the oscillator frequency caused temperature changes. Since capacitor C21 i in the oscillator feedback path, the temperatu coefficient of C24 will affect the output ampl tude of oscillator Q1. To compensate for thi a temperature-compensating capacitor is use as capacitor C24. Base bias for oscillator Q is developed by voltage divider L2, R7, R8. The output of oscillator Q1 is controlled by diodes CR1 and CR2. The positive-going lim of the signal is established by the cathode bia on diode CR1 (developed by voltage divider R R4) plus the drop of diode CR1. The negative going limit of the signal is established by the anode bias on diode CR2 (developed by voltag divider R5, R6, RT1) minus the drop of diod CR2; therefore, the peak-to-peak amplitude the signal is limited by the established dc reference levels. As the temperature of the circuit varies, the forward drop of diodes CI and CR2 varies. This would result in variations in the signal amplitude without temperature compensation. Thermistor RT1 varies the anode bias of diode CR2 in accordance wi the temperature changes and the negative-goi limit for the signal is shifted so that the limi ing region is constant. This action ensures that the amplitude of the signal does not vary with changes in temperature. Capacitors C1 and C23 are rf bypass capacitors. Resistor R10 provides degeneration to improve the stability of oscillator Q1. The output of osci lator Q1 is developed across emitter resisto R10 and inductor L3. The output of oscillato Q1 is coupled to the base of wideband amplifi Q2 by capacitor C26.

4-171. The base bias for wideband amplifie Q2 is developed by voltage divider R11, R13, from the 20 vdc. Emitter resistor R14 is un bypassed to provide the necessary degeneration, producing wide bandwidth, and uniform gain for this stage. Stages Q3 and Q4 are cascaded, direct-coupled emitter followers that provide the required low source impedance for driving the error loop and the high-

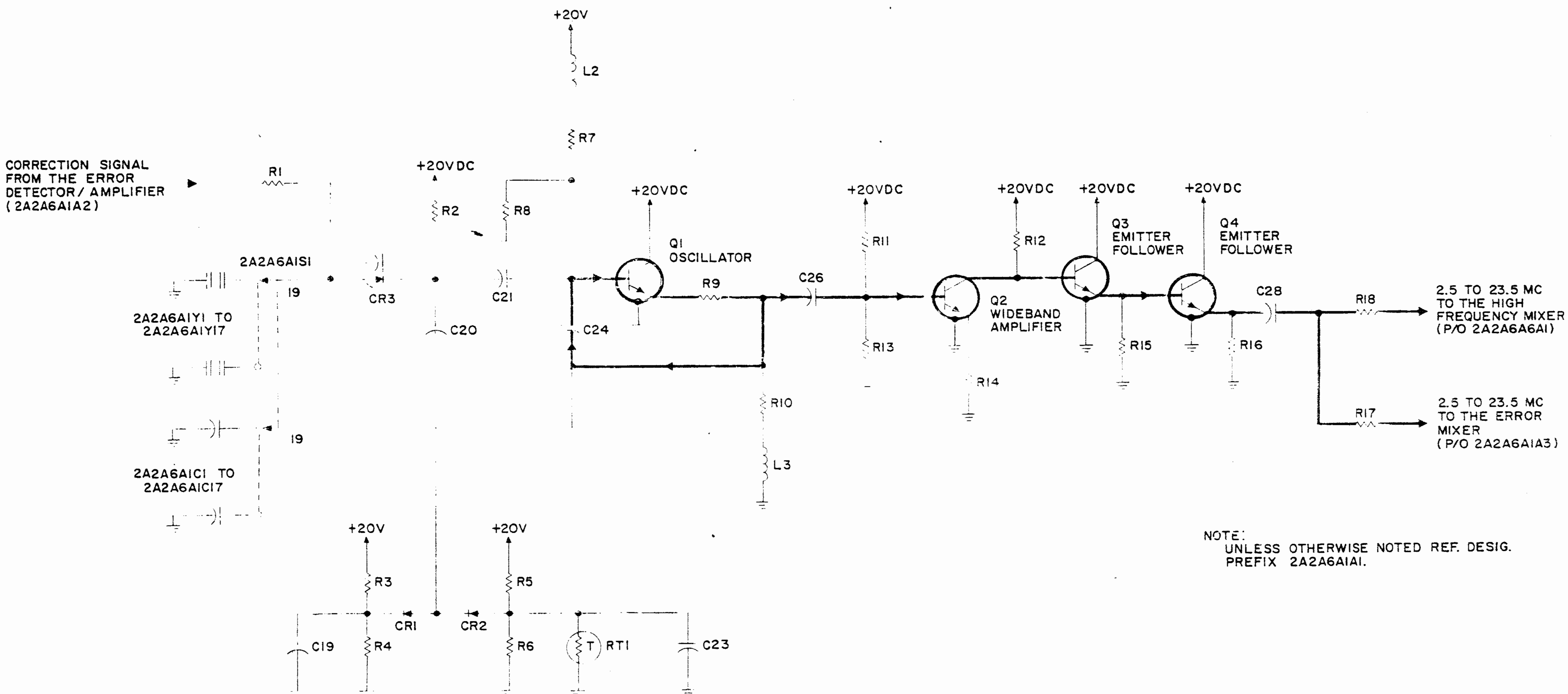

Figure 4-34. MC Oscillator, Simplified Schematic Diagram

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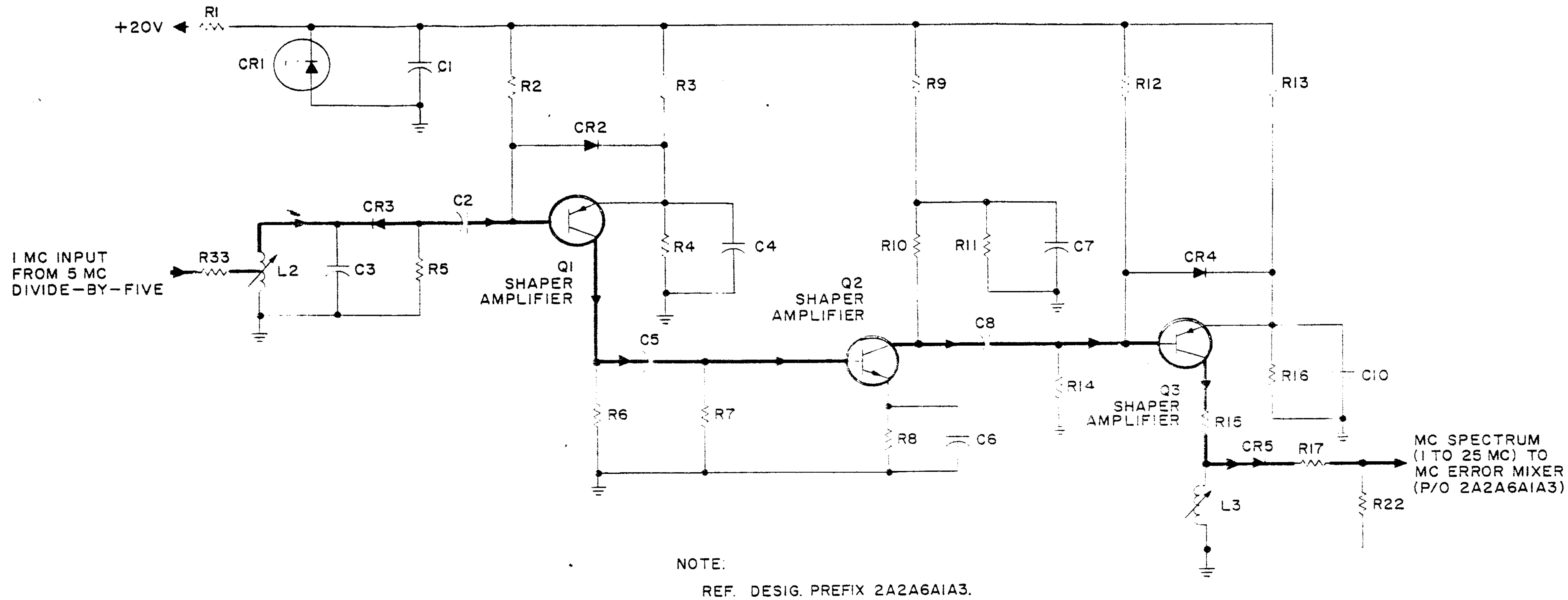

Figure 4-35. MC Spectrum Generator, Simplified Schematic Diagram

test data for the mc spectrum generator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 MC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-80.

c. 1 MC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-10.

d. Spectrum Generator/Mixer, Component and Test Point Location, Figure 5-79.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Multimeter, AN/PSM-4.

(5) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-34 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for alignment for mc spectrum generator adjustment procedures.

4-176. MC ERROR MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The mc error mixer (figure 4-36) consists of an isolation amplifier (Q5), an emitter follower (Q6) and a mixer (Q4). These circuits, which form a part of 1 MC Synthesizer Electronic Subassembly 2A2A6A1, mix the signal from the mc oscillator with the signal from the mc spectrum generator. An error signal is produced that, in the locked condition, is proportional to the phase relationship between the spectrum and the oscillator output. The following paragraphs describe the operation of the circuits in detail.

4-177. The input from the mc oscillator is coupled through capacitor C18 to the emitter of isolation amplifier Q5. Isolation amplifier Q5 is used in a grounded-base amplifier configuration, which provides high reverse attenuation to the output products of mixer Q4, preventing them from appearing in the output from the mc oscillator. Base bias for isolation amplifier Q5 is provided by voltage divider R27, R28. Resistor R30 and capacitor C20 are used for decoupling. The output of isolation amplifier Q5 is taken across collector resistor R29 and is coupled through capacitor C14 to the base of emitter follower Q6. Base bias for emitter follower Q6 is provided by voltage divider R23, R24. Resistor R31 and capacitor C12 are used for decoupling. Emitter follower Q6 provides a low source impedance to mixer Q4 and prevents loading of isolation amplifier Q5. The output of emitter follower Q6 is coupled through capacitor C13 to the emitter of mixer Q4. The signal from the mc spectrum generator is coupled through capacitor C9 to the base of mixer Q4. Base bias for mixer Q4 is provided by voltage divider R18, R21. Resistor R20 provides a small amount of degeneration to stabilize mixer Q4. The output circuit of mixer Q4 is a double-tuned circuit consisting of inductor L4, capacitors C16, C15 and C17, resistor R32, and transformer T1, which is tuned to 1.5 mc. When there is a frequency error, the signal from the mc oscillator is mixed with the two spectrum points that are within approximately ±1.5 mc of the oscillator frequency. The output of mixer Q4 includes two frequencies (one less than 1.5 mc and one more than 1.5 mc) if the mc oscillator has an error. When the mc oscillator is locked, only one frequency is present, since the frequency of the oscillator, ± the spectrum points, is 1.5 mc. For example, assume that the mc oscillator frequency is 11.499 mc; therefore, the two closest spectrum points will be 10 and 13 mc. These frequencies, when mixed, produce difference frequencies of 1.499 and 1.501 mc. It can be seen that when the mc oscillator is exactly 11.5 mc, the two difference frequencies will be identical (1.5 mc). The double-tuned circuit attenuates all mixer products except the difference frequencies. The output of the double-tuned filter is coupled through transformer T1 to the error detector/amplifier.

4-178. MC ERROR MIXER, TEST DATA. Pertinent references and applicable test data for the mc error mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 MC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-80.

c. 1 MC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-10.

d. Spectrum Generator/Mixer, Component and Test Point Location, Figure 5-79.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Multimeter, AN/PSM-4.

(5) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-34 in Technical Manual for Repair of Radio Set AN/WRC-1 and Radio Receiver R-1051/URR 2N Modules, NAVSHIPS 95700 for alignment for mc error mixer adjustment procedure.

4-179. ERROR DETECTOR/AMPLIFIER, FUNCTIONAL CIRCUIT DESCRIPTION. The error detector/amplifier (figure 4-37) consists of two if. amplifiers (Q1 and Q2) and a dc amplifier (Q3). These circuits, which form a part of 1 MC Synthesizer Electronic Subassembly 2A2A6A1, amplify and detect the mc error signal, producing a correction signal for subsequent application to the mc oscillator. The following paragraphs describe the operation of the error detector/amplifier circuit in detail.

4-180. The signal from the error mixer is coupled through capacitor C1 to the base of if. amplifier Q1. The base bias for amplifier Q1 is provided by voltage divider R1, R2. Resistor R22 and capacitor C14 are used for decoupling. Resistor R4 provides a small amount of degeneration to add to the stability of if. amplifier Q1. The output load of if. amplifier Q1 is a 1.5-mc tuned circuit consisting of capacitor C3 and transformer T1. Resistor R5 loads the tank circuit sufficiently to insure uniformity. The output signal of if. amplifier Q1 is coupled through transformer T1 to potentiometer R6, which is used to adjust the gain of the phase lock loop. The output from the wiper of this potentiometer is coupled through capacitor C12 to the base of if. amplifier Q2. The base bias for if. amplifier Q2 is provided by voltage divider R7, R8. Resistor R10 provides a small amount of degeneration to add to the stability of if. amplifier Q2. The output load of if. amplifier Q2 is a 1.5-mc tuned circuit consisting of capacitor C6 and transformer T2. Resistor R11 loads the tank circuit sufficiently to insure uniformity. The output signal of if. amplifier Q2 is coupled through transformer T2 and applied to a diode detector circuit. The diode detector circuit consists of diode CR1, resistor R12, and capacitor C13. The output of the diode detector is filtered by a network consisting of a composite of a constant-k section and an m-derived section. The constant-k section consists of capacitor C7, inductor L1, and a portion of inductor L2. The m-derived section consists of inductors L3 and L4, capacitor C8, and the remaining portion of inductor L2. Variable inductor L4 compensates for the tolerance of the components used in the m-derived section. Resistor R13 and capacitor C9 form the termination of the filter. The output of this filter is applied to the emitter of dc amplifier Q3. Resistor R14 provides a small amount of degeneration to add to the stability of dc amplifier Q3. Base bias for dc amplifier Q3 is provided by voltage divider R17, R18, R19, R20, RT1. Thermistor RT1 varies the bias with temperature to compensate for changes in the base-to-emitter voltage of dc amplifier Q3 which result from temperature changes. The network consisting of resistors R15 and R16, and capacitor C10 serves as the collector load for dc amplifier Q3 and is used as a lag network for the phase-locked loop, which decreases the noise output and increases the stability. Resistor R21 prevents the collector voltage of dc amplifier Q3 from rising above 19 vdc and forward-biasing voltage-variable capacitor 2A2A6A1A1CR3. The error voltage taken from the collector of dc amplifier Q3 is applied to the mc oscillator.

4-181. ERROR DETECTOR/AMPLIFIER, TEST DATA. Pertinent references and applicable test data for the error detector/amplifier are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 MC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-10.

c. 1 MC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-80.

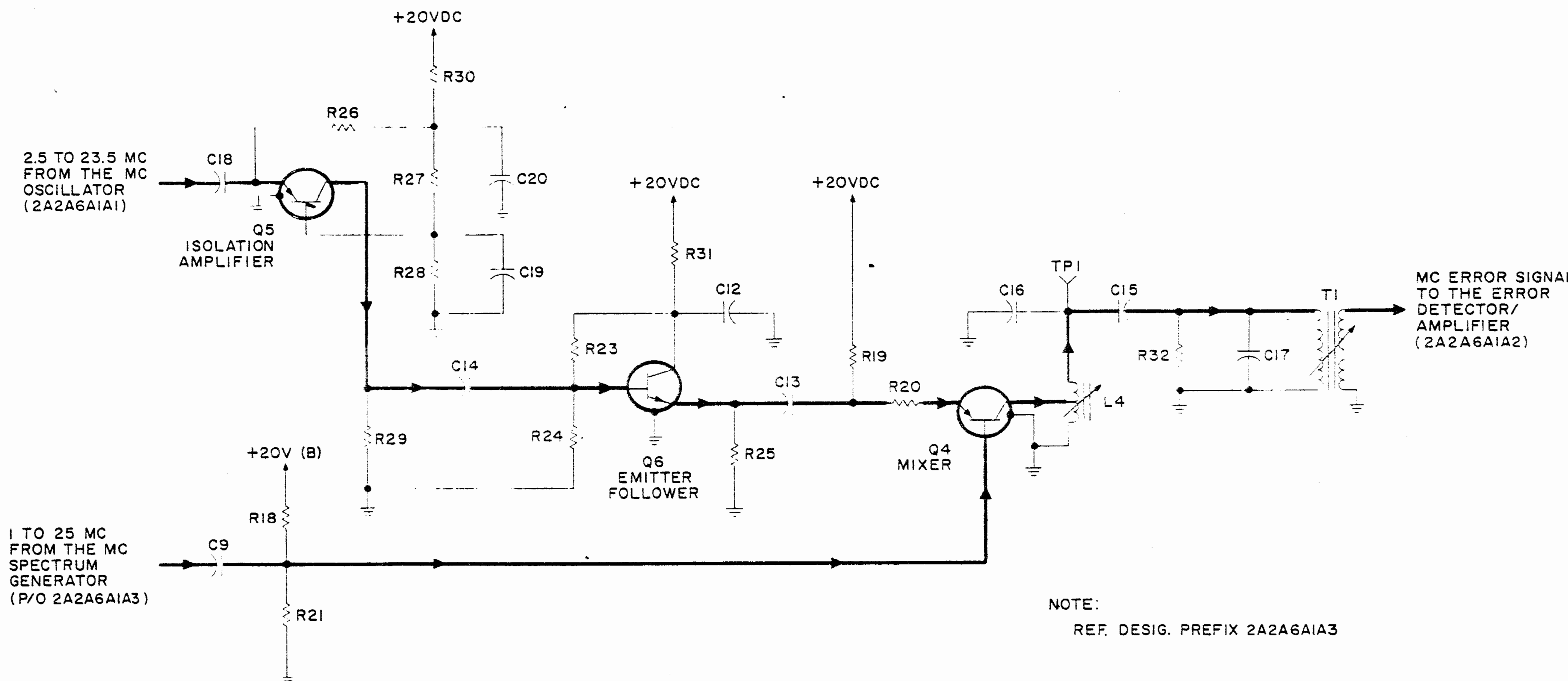

Figure 4-36. MC Error Mixer, Simplified Schematic Diagram

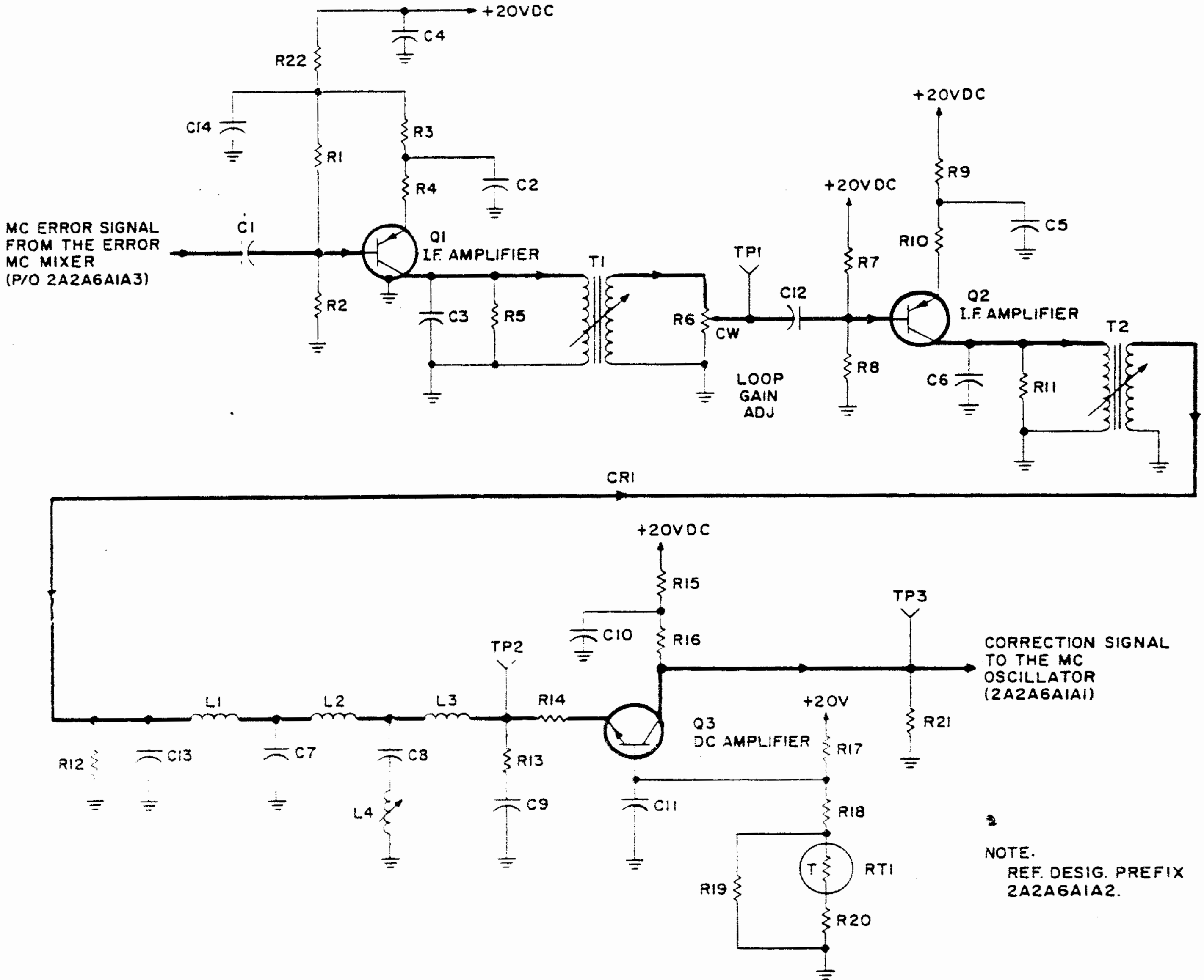

Figure 4-37. Error Detector/Amplifier, Simplified Schematic Diagram

d. MC Oscillator AGC, Component and Test Point Location, Figure 5-78.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Multimeter, AN/PSM-4.

(5) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-34 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700, for alignment for error detector/amplifier adjustment procedure.

4-182. 100 KC SPECTRUM GENERATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 100 kc spectrum generator (figure 4-38) consists of a trigger amplifier (Q1), a divide-by-five multivibrator (Q2 and Q3), a gate amplifier (Q4), a keyed oscillator (Q5), an amplifier

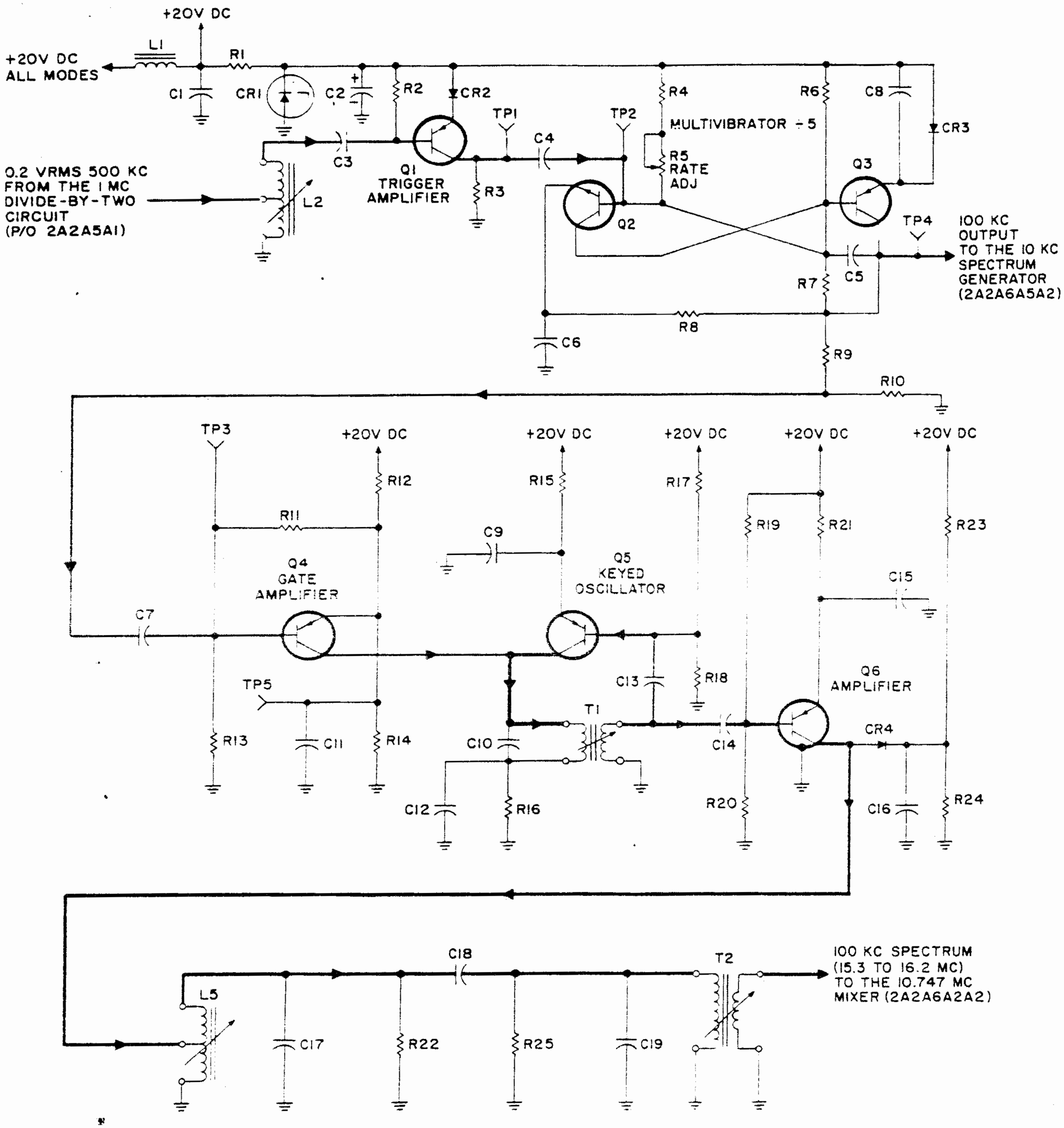

Figure 4-38. 100 KC Spectrum Generator, Simplified Schematic Diagram

(Q6), and a double-tuned filter (L5 and T2). This circuit, which forms a part of Spectrum Generator Electronic Subassembly 2A2A6A5, produces a spectrum of frequencies between 15.3 and 16.2 mc. This spectrum is applied to 10.747 mc mixer A2A6A2A2 to produce the 10.747 mc reference frequency used for error cancellation in the 100 kc mixing frequency scheme. This circuit also provides the 100 kc trigger pulses to 10 kc spectrum generator A2A6A5A2. The 100 kc spectrum generator is used in all modes of operation. The following paragraphs describe the operation of the 100 kc spectrum generator in detail.

4-183. The input to the 100 kc spectrum generator is the 500-kc sinusoidal output from 1 mc divide-by-two circuit A2A5A1. This signal is applied to autotransformer L2, where it is stepped up and in turn coupled to the base of trigger amplifier Q1 by capacitor C3. A positive 20 vdc is applied to the 100 kc spectrum generator in all modes of operation from power supply 2A2A8 (located on the main frame). The positive 20 vdc is regulated to 10 vdc by Zener diode CR1, which draws enough current in addition to the current drawn by the load to maintain a 10 vdc drop across R1. This regulated 10 vdc is used to provide a stable supply for trigger amplifier Q1 and multivibrator Q2, Q3. The negative halves of the 500 kc signal, applied to the base of trigger amplifier Q1, are of sufficient magnitude to drive it into saturation. This results in the collector of trigger amplifier Q1 being switched between zero (non-conducting) and 9.0 vdc (saturated). The small drop (1 volt) is caused by the small forward resistance of the diode and the collector-to-emitter resistance of the transistor. Diode CR2 provides temperature compensation for trigger amplifier Q1 and aids in the shaping of the positive output triggers. Resistor R2 is the base-return resistor, providing capacitor C3 with a discharge path. The output pulses of trigger amplifier Q1 are developed across resistor R3 and are differentiated by capacitor C4 and the input impedance of divide-by-five multivibrator Q2, Q3. This results in a series of 500-kc positive and negative triggers to multivibrator Q2, Q3.

4-184. Divide-by-five multivibrator Q2, Q3 is an astable multivibrator, which is locked at a 500-kc rate. Refer to timing diagram, figure 4-39, for the following detailed discussion of multivibrator Q2, Q3. Multivibrator Q2, Q3 is free-running until locked by the 500-kc input trigger pulses from trigger amplifier Q1. Assume that a positive trigger pulse is applied to the base of transistor Q2 and that transistors Q2 and Q3 are cutoff. The collector of transistor Q2 and the base of transistor Q3 are at the voltage supply level (10 vdc) at this time. When the input pulse causes transistor Q2 to conduct, a voltage drop is developed across resistor R6, decreasing the voltage on the base of transistor Q3. Since the emitter of transistor Q3 is essentially at the supply voltage level (when it is cutoff), it becomes forward-biased and conducts. This causes the collector of transistor Q3 to go from 0 volts (no conduction) to approximately 9 volts. The 1 volt drop from the 10 vdc supply voltage level is caused by the small forward drop of diode CR3 and the collector-to-emitter drop of transistor Q3. The base-voltage divider for transistor Q2 (R4, R5, R7) now has the 9 vdc (collector voltage of transistor Q3) on one end and the 10 vdc supply voltage on the other end. This causes transistor Q2 to become saturated. Therefore, transistors Q2 and Q3 are both conducting and are in saturation. Capacitor C6 now charges through two paths. One path is through tran-

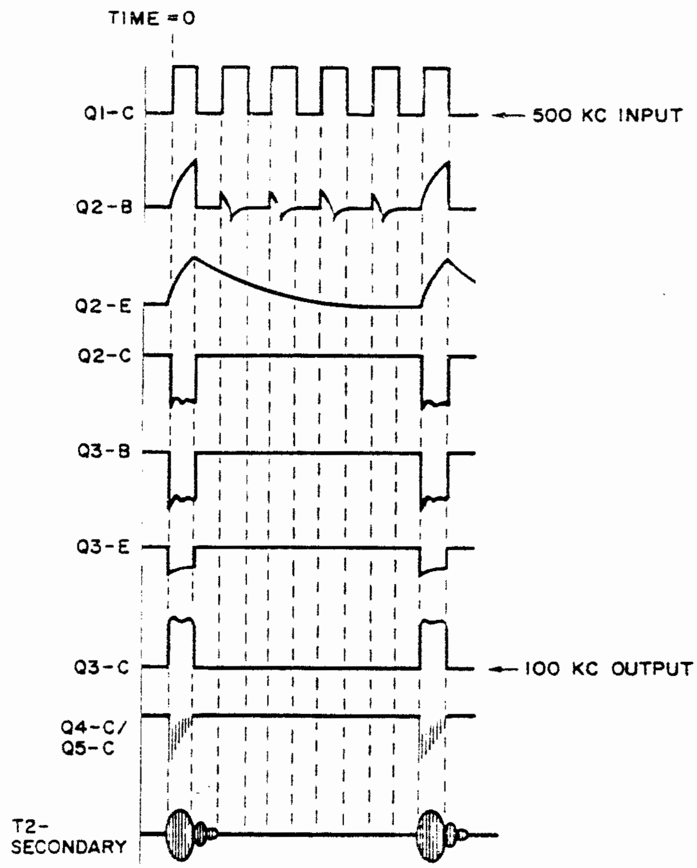

Figure 4-39. Divide-by-Five Multivibrator, Timing Diagram

sistor Q2 and resistors R4, R5, and R6. The other path is through resistor R8, transistor Q3, and diode CR3. As capacitor C6 charges, the emitter voltage of transistor Q2 increases, resulting in a decrease of forward bias on transistor Q2. This reduces the collector current of transistor Q2, resulting in a decreased drop across resistor R6. Therefore, the base voltage on transistor Q3 will start to go positive, resulting in a decrease of its forward bias. The collector current of transistor Q3 then begins to decrease as the forward bias decreases. Therefore, the collector voltage of transistor Q3 begins to decrease, increasing the voltage across the base voltage divider of transistor Q2. This reduces the forward bias of transistor Q2 even more. This regeneration brings transistors Q2 and Q3 out of saturation and continues until they are both cut off. Capacitor C6 now starts to discharge through resistors R10, R9, and R8. During this discharge period, the positive and negative trigger pulses are still applied to the base of transistor Q2, but are not of sufficient amplitude to forward-bias and turn on transistor Q2. When transistors Q2 and Q3 are cut off, the base bias of transistor Q2 is determined by voltage divider R4, R5, R7, R9, R10. The emitter voltage of transistor Q2 is the charge on capacitor C6. Therefore, capacitor C6 has to discharge to such a level that when a positive trigger pulse is applied to the base of transistor Q2, it starts conducting. The time constant of the RC network consisting of C6, R8, R9, and R10 is fixed such that resistor R5 can be used to adjust the bias on transistor Q2, allowing every sixth positive trigger pulse, after the initial trigger pulse, to turn transistor Q2 on. When this occurs, the collector voltage on transistor Q2 will again drop, and the regeneration process described above will be repeated. Thus, the process of regeneration occurs before the natural period has been completed as the result of every sixth positive trigger pulse on the base of transistor Q2. This results in an output (collector of transistor Q3) that is exactly one-fifth of the input trigger pulse rate. The 100-kc signal present on the collector of transistor Q3 is applied to the 10 kc spectrum generator. Capacitor C8 prevents any degeneration in the circuit as a result of the small forward resistance of diode CR3. Capacitor C5 speeds up the application of the pulses from the collector of transistor Q3 to the base of transistor Q2. The 100-kc output signal of multivibrator Q2, Q3, which is developed across voltage divider R9, R10, is coupled to the base of gate amplifier Q4 by capacitor C7.

4-185. During the off time of multivibrator Q2, Q3, gate amplifier Q4 is forward-biased and in saturation. Forward-bias voltage for gate amplifier Q4 is developed by voltage dividers R12, R14 and R12, R11, R13 from the positive 20 vdc applied from main frame power supply 2A2A8. Capacitor C11 is the emitter bypass capacitor. When gate amplifier Q4 conducts, the base is at approximately 10.1 vdc and the emitter is at approximately 10.3 vdc, the drop being caused by the small emitter-to-base resistance. With gate amplifier Q4 in saturation, the tank circuit (capacitor C10 and the primary of transformer T1) of keyed oscillator Q5 will be heavily loaded by the small collector-to-emitter resistance of gate amplifier Q4, preventing regeneration. When a positive pulse is coupled to the base of gate amplifier Q4, it is reversed-biased and cut off for the duration of the pulse. This removes the load from the tank circuit of keyed oscillator Q5, permitting it to oscillate at its natural frequency. Resistor R16 limits the current flow through gate amplifier Q4 when it is in saturation.

4-186. Voltage divider R17, R18 and emitter resistor R15 develop bias voltage for oscillator Q5 from the positive 20 vdc applied from the power supply on the main frame. Capacitor C9 is the emitter bypass capacitor. When the load created by the conduction of gate amplifier Q4 is removed from the tank circuit of keyed oscillator Q5, the tank circuit will produce an 0.8-microsecond sinusoidal burst of frequencies. This results in a spectrum of frequencies centered around the free-running frequency of keyed oscillator Q5. The desired spectrum consists of ten spectrum points, which are below the free-running (center) frequency of keyed oscillator Q5, separated by the 100-kc keying rate. The secondary of transformer T1 and capacitor C13 provide the required feedback path for keyed oscillator Q5, so that the necessary loop gain can be developed to sustain oscillations. Capacitor C12 is an rf bypass for resistor R16 at the output frequency of keyed oscillator Q5.

4-187. The spectrum output of the tank circuit is coupled to the base of amplifier Q6 by capacitor C14. Operating voltage for amplifier Q6 is developed by voltage divider R19, R20 and emitter resistor R21 from the positive 20 vdc applied from the power supply on the main frame. The output of amplifier Q6 is limited by diode CR4. The amount of limiting is adjusted by selecting the value of resistor R24.

Resistors R23 and R24 form a voltage divider for developing the cathode bias on limiter CR4. Capacitors C15 and C16 are bypass capacitors. The output of amplifier Q6 is developed across a tuned circuit consisting of capacitor C17 and inductor L5. Resistor R22 increases the bandwidth of the tuned circuit and ensures uniformity. The output of tuned circuit L5, C17 is coupled by capacitor C18 to another tuned circuit consisting of capacitor C19 and the primary of transformer T2. Resistor R25 increases the bandwidth of this tuned circuit. The passband of these two tuned filters is sufficient to pass the desired 15.3-to-16.2-mc spectrum, but has sufficient selectivity to eliminate all the undesired harmonics and products produced by keyed oscillator Q5. The output of the 100 kc spectrum generator is coupled to 10.747 mc mixer 2A2A6A2A2.

4-188. 100 KC SPECTRUM GENERATOR, TEST DATA. Pertinent references and applicable test data for the 100 kc spectrum generator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Spectrum Generator Electronic Subassembly, Servicing Block Diagram, Figure 4-81.

c. Spectrum Generator Electronic Subassembly, Schematic Diagram, Figure 5-14.

d. 100 KC Spectrum Generator, Component and Test Point Location, Figure 5-10.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Oscilloscope, AN/USM-105A.

(3) Electronic Multimeter, CCVO-91CA.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-26 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700, for 100 kc spectrum generator adjustment procedure.

4-189. 10.747 MC MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The 10.747 mc mixer (figure 4-40) consists of an isolation amplifier (Q2), a mixer (Q1), and a 10.747 mc crystal filter (FL1). These circuits, which form a part of 100 KC Synthesizer Electronic Subassembly 2A2A6A2, produce a 10.747-mc output at a level suitable for use in 17.847/27.847 mc mixer 2A2A6A2A3. These circuits are used in all modes of operation. The following paragraphs describe the operation of the 10.747 mc mixer in detail.

4-190. The 4.553-to-5.453-mc output from the 4.553 to 5.453 mc oscillator is coupled to the emitter of isolation amplifier Q2 by capacitor C7. Voltage divider R4, R5 and emitter resistor R7 derive operating voltage for isolation amplifier Q2 from the positive 20-vdc supply line. Resistor R6 and capacitor C6 provide decoupling to prevent any interaction with other circuits connected to the positive 20-vdc supply line. Capacitor C3 is an rf bypass capacitor. Isolation amplifier Q2 is a grounded-base amplifier, which prevents the spectrum frequencies and mixer products in mixer Q1 from being fed back into the hi-band/lo-band mixer/amplifier circuits via the 4.553 to 5.453 mc oscillator circuits. The output of isolation amplifier Q2 is developed across the primary of transformer T1. Resistor R9 ensures the uniformity of the signal developed across transformer T1.

4-191. The 4.553-to-5.453-mc output of isolation amplifier Q2 is coupled to the emitter of mixer Q1 by capacitor C1. The 100-kc spectrum (15.3 to 16.2 mc) from the 100 kc spectrum generator is coupled to the base of mixer Q1 by capacitor C2. Voltage divider R1, R2 derives base bias for mixer Q1 from the positive 20-vdc supply line. Resistor R3 and capacitor C4 provide decoupling to prevent any interaction with the other circuits connected to the positive 20-vdc supply line. The emitter bias for mixer Q1 is developed from the output of the 10.747 mc mixer agc circuit by emitter resistor R8. The agc voltage is a variable voltage that controls the amount of forward-biasing, and thereby, the gain of mixer Q1. The frequency from the 4.553 to 5.453 mc oscillator is mixed with each of the ten spectrum points applied by the 100 kc spectrum generator. The resulting mixing products are developed across a tuned circuit consisting of capacitor C5 and the primary of transformer T2. This circuit is tuned to 10.747 mc, the desired mixer product. Transformer T2 couples the output of mixer Q1 to filter FL1. Filter FL1 is a 10.747 mc crystal lattice filter which eliminates all other mixing products. The 10.747 mc output of filter FL1 is developed

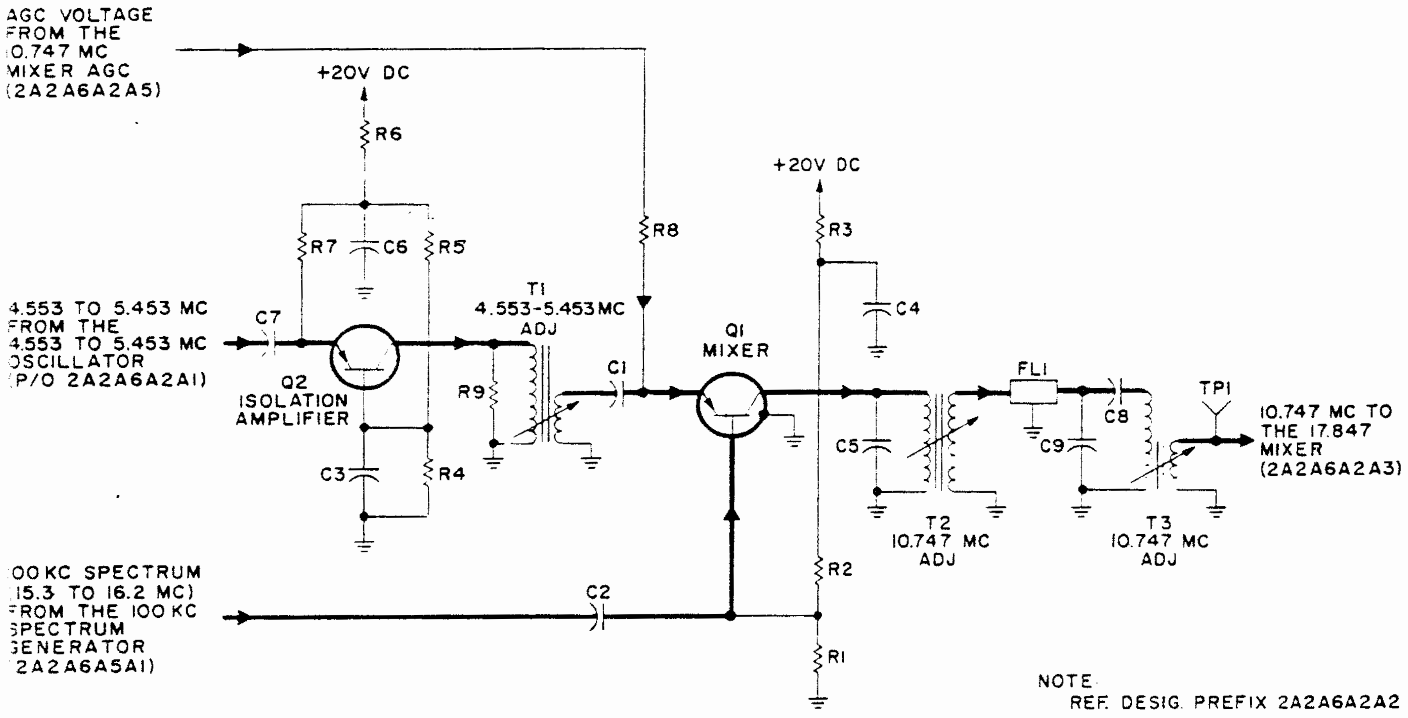

Figure 4-40. 10.747 MC Mixer, Simplified Schematic Diagram

across the tuned circuit consisting of capacitors C8 and C9 and the primary of transformer T3. The output of the 10.747 mc mixer circuit is coupled to 17.847/27.847 mc mixer 2A2A6A2A3 by transformer T3.

4-192. 10.747 MC MIXER, TEST DATA. Pertinent references and applicable test data for the 10.747 mc mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 100 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-79.

c. 100 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-11.

d. 10.747 MC Mixer, Component and Test Point Location, Figure 5-83.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-32 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700, for 10.747 mc mixer adjustment procedure.

4-193. 10.747 MC MIXER AGC, FUNCTIONAL CIRCUIT DESCRIPTION. The 10.747 mc mixer AGC (figure 4-41) consists of two agc amplifiers (Q2 and Q3) and a detector (Q4). These circuits, which form a part of 100 KC Synthesizer Electronic Subassembly 2A2A6A2, produce an agc voltage which is used to control the gain of mixer Q1 in the 10.747 mc mixer (2A2A6A2A2). These circuits are used in all modes of operation. The following paragraphs describe the operation of the 10.747 mc mixer agc circuit in detail.

4-194. The 22.4-to-23.3-mc or 32.4-to-33.3-mc output from the hi-band/lo-band mixer/amplifier is coupled to the base of agc amplifier Q2 by capacitor C4. Voltage divider R4, R5 derives bias voltage for agc amplifier Q2 from the positive 20-vdc supply line. Inductor L2 is a peaking coil which compensates for high frequency roll-off, and provides for uniform output for both the hi-band and lo-band mixing frequencies. Resistor R7 develops enough

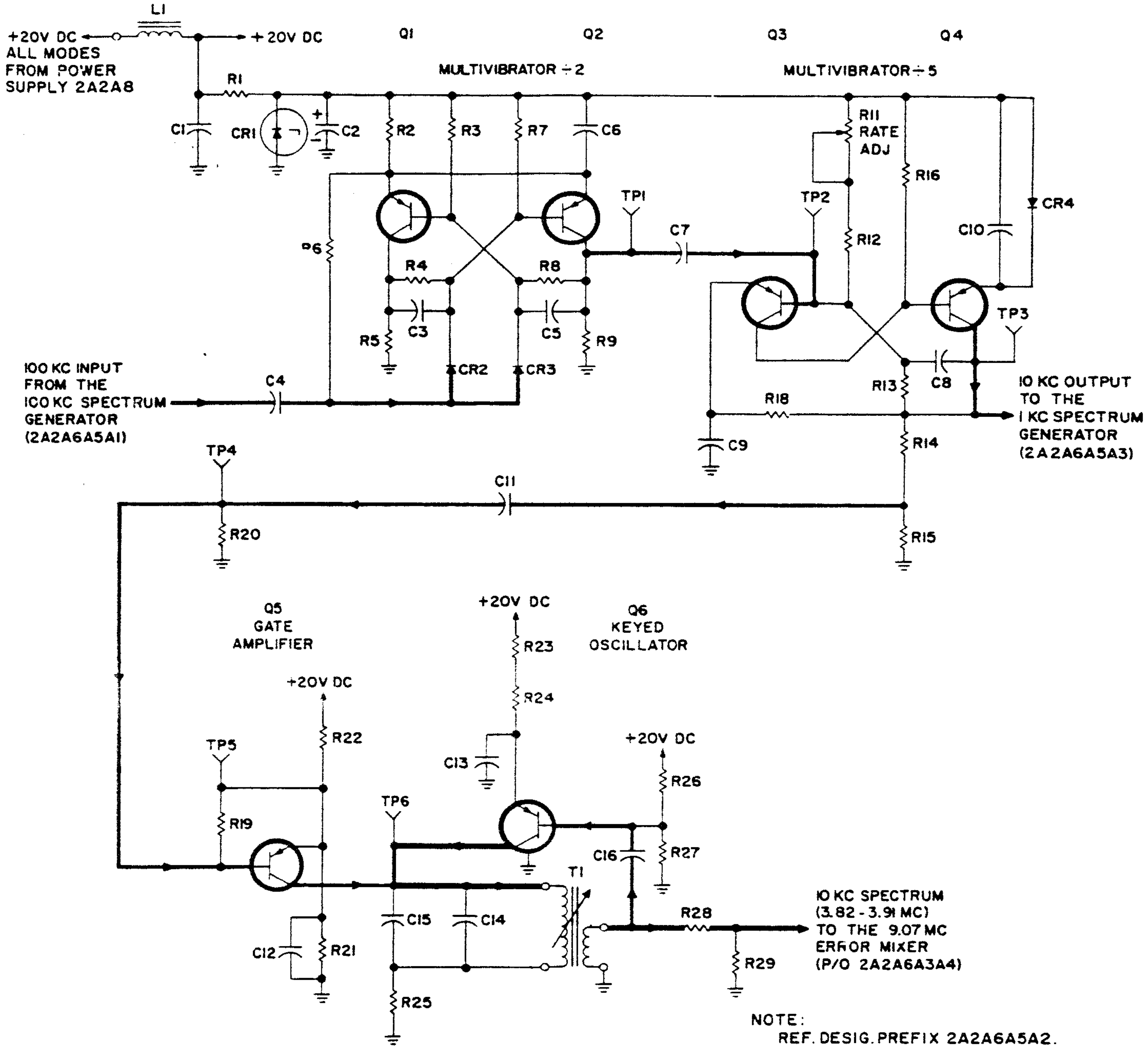

Figure 4-44. 10 KC Spectrum Generator, Simplified Schematic Diagram

results in a 3.82-to-3.91-mc frequency spectrum with a 10-kc separation between spectrum points. The output of keyed oscillator Q6 is divided by resistors R28 and R29 and applied to the 9.07 mc error mixer (part of 2A2A6A3A4).

4-212. 10 KC SPECTRUM GENERATOR, TEST DATA. Pertinent references and applicable test data for the 10 kc spectrum generator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Spectrum Generator Electronic Subassembly, Servicing Block Diagram, Figure 4-81.

c. Spectrum Generator Electronic Subassembly, Schematic Diagram, Figure 5-14.

d. 10 KC Spectrum Generator, Component and Test Point Location, Figure 5-106.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Frequency Meter, CAQI-524D.

(5) Multimeter, AN/PSM-4.

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-276 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 10 kc spectrum generator adjustment procedure.

4-213. 1 KC SPECTRUM GENERATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 1 kc spectrum generator (figure 4-45) consists of a divide-by-two multivibrator (Q1, Q2), a divide-by-five multivibrator (Q3, Q4), a gate amplifier (Q5), and a keyed oscillator (Q6). These circuits, which form a part of Spectrum Generator Electronic Subassembly 2A2A6A5, produce a spectrum of frequencies between 0.122 and 0.131 mc. This frequency spectrum is applied to the 1.981 mc error mixer (part of 2A2A6A3A4) to produce the reference frequencies used in the error cancellation scheme. These circuits also provide the 5-kc trigger frequency to the 5 kc spectrum generator for producing the 5-kc spectrum. The 1 kc spectrum generator is used in all modes of operation. The following paragraphs describe the operation of the 1 kc spectrum generator in detail.

4-214. The input to the 1 kc spectrum generator is the 10-kc pulse output of the 10 kc spectrum generator. This input signal is differentiated by capacitor C4 and the input impedance of divide-by-two multivibrator Q1, Q2. The resulting positive pulses are used to trigger divide-by-two multivibrator Q1, Q2. Divide-by-two multivibrator Q1, Q2 is identical to divide-by-two multivibrator Q1, Q2 in the 10 kc spectrum generator (refer to paragraph 4-210), except for the additional output. The 5-kc pulsed output of the divide-by-two multivibrator is divided by voltage divider R9, R10 and applied to the 5 kc spectrum generator as trigger pulses. The 5-kc pulse output of divide-by-two multivibrator Q1, Q2 is differentiated by capacitor C7 and the input impedance of divide-by-five multivibrator Q3, Q4. Diode CR4 provides a fast turn-on time for transistor Q3 and holds transistor Q3 in saturation during its conduction period. Divide-by-five multivibrator Q3, Q4 is identical to divide-by-five multivibrator Q3, Q4 in the 100 kc spectrum generator (refer to paragraph 4-184), except for circuit time constants. The 1-kc pulse output of divide-by-five multivibrator Q3, Q4 is coupled to the base of gate amplifier Q5. Gate amplifier Q5 is identical to gate amplifier Q4 in the 100 kc spectrum generator (refer to paragraph 4-185). Gate amplifier Q5 turns keyed oscillator Q6 on and off at a 1-kc repetition rate. Keyed oscillator Q6 is identical to keyed oscillator Q5 in the 100 kc spectrum generator (refer to paragraph 4-186). The output of keyed oscillator Q6 is a 10-microsecond sinusoidal burst of frequencies with a 1-kc repetition rate. This results in a 0.122-to-0.131-mc frequency spectrum with a 1-kc separation between spectrum points.

4-215. 1 KC SPECTRUM GENERATOR, TEST DATA. Pertinent references and applicable test data for the 1 kc spectrum generator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Spectrum Generator Electronic Subassembly, Servicing Block Diagram, Figure 4-81.

c. Spectrum Generator Electronic Subassembly, Schematic Diagram, Figure 5-14.

d. 1 KC Spectrum Generator, Component and Test Point Location, Figure 5-107.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Frequency Meter, CAQI-524D.

(5) Multimeter, AN/PSM-4.

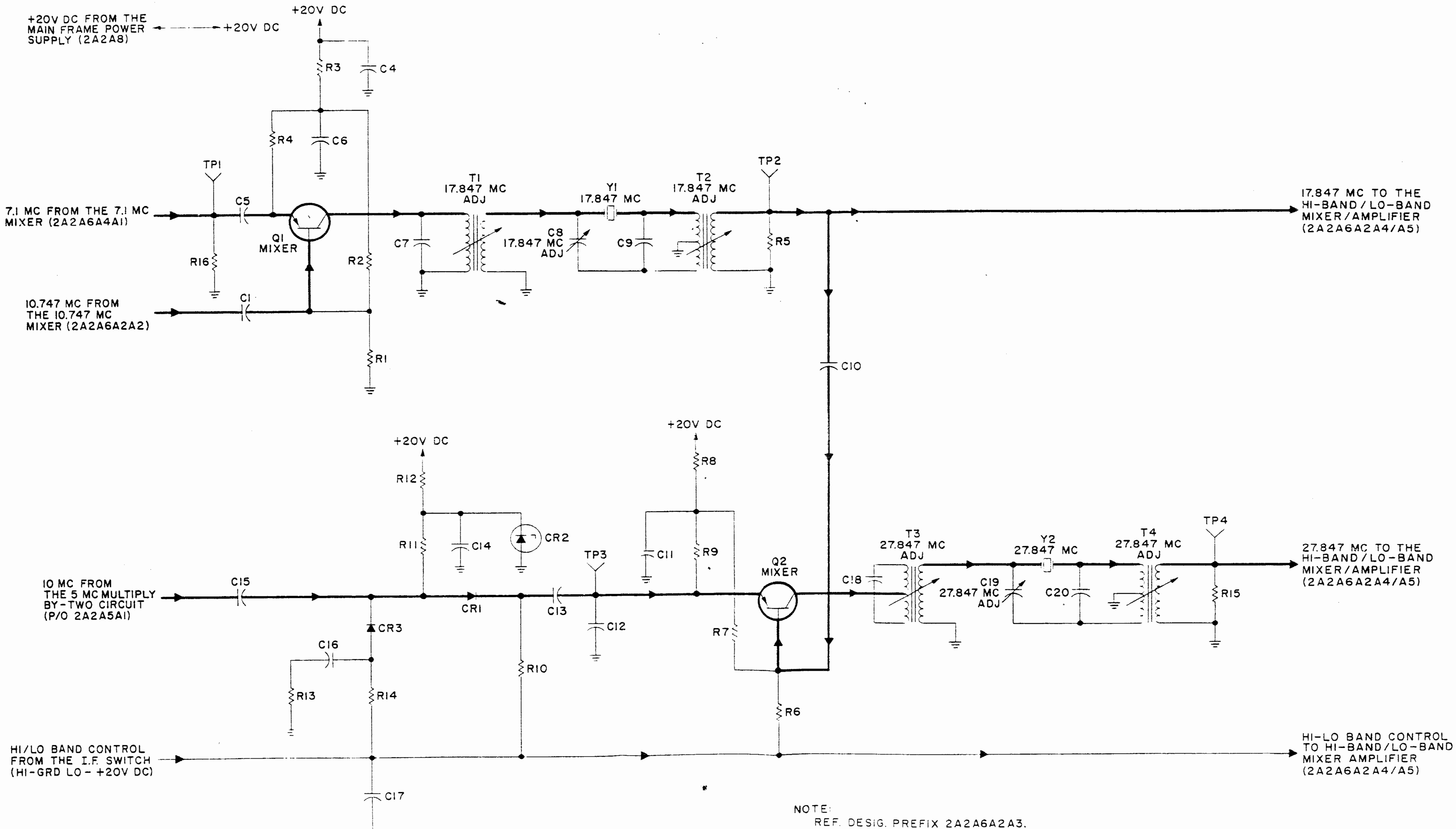

Figure 4-43. 17.847/27.847MC Mixer, Simplified Schematic Diagram

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4-201. 17.847/27.847 MC MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The 17.847/27.847 mc mixer (figure 4-43) consists of two mixers (Q1 and Q2), a gating circuit (CR1, CR3), a 17.847 mc filter (Y1), and a 27.847 mc filter (Y2). These circuits, which form a part of 100 KC Synthesizer Electronic Subassembly 2A2A6A2, produce either a 17.847-mc or 27.847-mc frequency for use in the mixing circuits of the hi-band/lo-band mixer/amplifier. These circuits are used in all modes of operation. The following paragraphs describe the operation of the 17.847/27.847 mc mixer in detail.

4-202. The 7.1-mc output from the 7.1 mc mixer is coupled to the emitter of mixer Q1 by capacitor C5. The 10.747-mc output from 10.747 mc mixer 2A2A6A4A1 is coupled to the base of mixer Q1 by capacitor C1. Voltage divider R1, R2 and emitter resistor R4 derive operating voltage for mixer Q1 from the positive 20-vdc supply line. Resistor R3 and capacitor C6 provide decoupling to prevent interaction with the other circuits connected to the 20 vdc supply line. Resistor R16 is the terminating resistor for the 7.1-mc input signal. Mixer Q1 mixes the two input signals and develops the resulting mixing products across the tuned circuit consisting of capacitor C7 and the primary of transformer T1. The circuit is tuned to 17.747 mc, the desired additive product.

4-203. The output of mixer Q1 is coupled to a crystal filter consisting of transformers T1 and T2, capacitors C8 and C9, and crystal Y1. Crystal Y1, series-resonant at 17.847 mc, passes the desired additive mixing product. Since the crystal can also be parallel resonated with its own shunt capacitance, capacitor C8 and the bottom half of the primary of transformer T2 are adjusted to cancel the effect of this shunt capacitance. The output of the filter is coupled to the hi-band/lo-band mixer/amplifier (when the lo-band of mixing frequencies is required) and to the base of mixer Q2 (when the hi-band of mixing frequencies is required) by transformer T2. Resistor R5 terminates the crystal filter.

4-204. The 10-mc signal from the 5 mc multiply-by-two circuit (part of 2A2A5A1) is coupled to the anode of diode CR1 by capacitor C15. Zener diode CR2 regulates the positive 20 vdc to 10 vdc by drawing enough current in addition to the load current to maintain a 10-vdc drop across resistor R12. This 10 vdc is applied to the cathode of diode CR3 and to the anode of diode CR1 through isolating resistor R11. When the lo-band output from the hi-band/lo-band mixer/amplifier is required, 20 vdc is applied to resistors R6, R10 and R14. Voltage divider R6, R7, which produces the base bias, on mixer Q2, then has 20 vdc applied to both ends. Thus, mixer Q2 is biased off when the lo-band of frequencies is being used. The lo-band positive 20 vdc is also applied through resistor R10 to the cathode of diode CR1. Therefore, when the lo-band of frequencies is being used, diode CR1 is back-biased, preventing the 10-mc signal from passing. The lo-band positive 20 vdc is also applied to the anode of diode CR3 through resistor R14. Consequently, diode CR3 is forward-biased and conducts. The 10-mc signal is then allowed to pass through capacitor C16 to 51-ohm load resistor R13. Therefore, resistor R13 loads the 10-mc signal when the lo-band mixing frequencies are required.

4-205. When the hi-band mixing frequencies are required, a ground is applied to resistors R14, R10, and R6. The ground is applied through isolating resistors R14 and R10 to diodes CR3, and CR1, respectively. This back-biases diode CR3 and forward-biases diode CR1. When diode CR1 is forward-biased, it conducts, allowing the 10-mc signal to pass. The 10-mc signal is coupled to the emitter of mixer Q2 by capacitor C13.

4-206. Voltage divider R6, R7 and emitter resistor R9 derive operating voltage for mixer Q2 from the positive 20-vdc supply line. Resistor R8 and capacitor C11 provide decoupling to prevent interaction with other circuits connected to the positive 20-vdc supply line. Capacitor C12 is the emitter bypass capacitor. The 17.847-mc output of the crystal filter is coupled to the base of mixer Q2 by capacitor C10. The 17.847-mc and 10-mc signals are mixed, and the resulting products are developed across the tuned circuit consisting of capacitor C18 and the primary of transformer T3. This circuit is tuned to 27.847 mc, which is the desired additive mixer product. Transformer T3 couples the output of mixer Q2 to a crystal filter, consisting of crystal Y2, transformers T3 and T4, and capacitors C19 and C20. Each of these components has the same function as its corresponding component in the 17.847 mc crystal filter. Resistor R15 is the termination for the crystal filter. The output of this crystal filter is coupled to the hi-band/lo-band mixer/amplifier by transformer T4.

4-207. 17.847/27.847 MC MIXER, TEST DATA. Pertinent references and applicable test data for the 17.847/27.847 mc mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 100 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-79.

c. 100 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-11.

d. 17.847/27.847 MC Mixer Component and Test Point Location, Figure 5-85.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Frequency Meter, CAQI-524D.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-32 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 17.847/27.847 mc adjustment procedures.

4-208. 10 KC SPECTRUM GENERATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 10 kc spectrum generator (figure 4-44) consists of a divide-by-two multivibrator (Q1, Q2), a divide-by-five multivibrator (Q3, Q4), a gate amplifier (Q5), and a keyed oscillator (Q6). These circuits, which form a part of Spectrum Generator Electronic Subassembly 2A2A6A5, produce a spectrum of frequencies between 3.82 and 3.91 mc. This frequency spectrum is applied to the 9.07 mc error mixer (part of 2A2A6A3A4) to produce the reference frequencies used in the error cancelling scheme. These circuits also provide the 10-kc trigger pulses to the 1 kc spectrum generator. The 10 kc spectrum generator is used in all modes of operation. The following paragraphs describe the operation of the 10 kc spectrum generator in detail.

4-209. The input to the 10 kc spectrum generator is the 100-kc pulsed output of the 100 kc spectrum generator. Positive 20 vdc from main frame power supply 2A2A8 is applied to the 10 kc spectrum generator in all modes of operation. The positive 20 vdc is regulated to 10 vdc by Zener diode CR1, which draws enough current in addition to the current drawn by the load to maintain a 10-vdc drop across resistor R1. This 10 vdc is used to provide a stable supply voltage for divide-by-two multivibrator Q1, Q2 and divide-by-five multivibrator Q3, Q4.

4-210. Divide-by-two multivibrator Q1, Q2 is a conventional bistable multivibrator that produces one output pulse for every two input pulses. The 100-kc input pulses are differentiated by capacitor C4 and the input impedance of multivibrator Q1, Q2. The resulting positive triggers are directed to the saturated transistor of divide-by-two multivibrator Q1, Q2 by steering diodes CR2 and CR3. This cuts off the saturated transistor and starts the process of regeneration. Resistor R6 references the anodes of steering diodes CR2 and CR3 at the same potential as the emitters of transistors Q1 and Q2 and provides the return path for capacitor C4.

4-211. The output of divide-by-two multivibrator Q1, Q2 is a 50-kc square wave. This signal is differentiated by capacitor C7 and the input impedance of divide-by-five multivibrator Q3, Q4. The resulting positive pulses are used to trigger divide-by-five multivibrator Q3, Q4. Divide-by-five multivibrator Q3, Q4 is identical to divide-by-five multivibrator Q2, Q3 in the 100 kc spectrum generator (refer to paragraph 4-184), except for circuit time constants. The 10-kc output signal of divide-by-five multivibrator Q3, Q4 is applied directly to the 1 kc spectrum generator. The 10-kc output signal of divide-by-five multivibrator Q3, Q4 is divided by resistors R14 and R15 and coupled to the base of gate amplifier Q5 by capacitor C11. Gate Amplifier Q5 is identical to the gate amplifier in the 100 kc spectrum generator (refer to paragraph 4-185). Gate amplifier Q5 turns keyed oscillator Q6 on and off at a 10-kc repetition rate. Keyed oscillator Q6 is identical to keyed oscillator Q5 in the 100 kc spectrum generator (refer to paragraph 4-186). The output of keyed oscillator Q6 is a 0.7-microsecond sinusoidal burst of frequencies with a 10-kc repetition rate. This

d. 10.747 MC Mixer AGC, Component and est Point Location, Figure 5-89.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Oscilloscope, AN/USM-105A.

(3) Multimeter, AN/PSM-4.

(4) Translator/Synthesizer Test Set, -2133/WRC-1.

f. Refer to paragraph 3-32 in Technical anual for Repair of AN/WRC-1 and R-1051/ RR 2N Modules, NAVSHIPS 95700, for .747 mc mixer agc adjustment procedures.

198. 5 MC MULTIPLY-BY-TWO, FUNC- ONAL CIRCUIT DESCRIPTION. The 5 mc ltiply-by-two circuit (figure 4-42) doubles e frequency of the 5-mc input signal obtained om switch A2A5S1 in the comparator circuit subsequent use in 17.847/27.847 mc mixer 2A6A2A3. This circuit consists of a 10 mc plifier (Q4), which forms a part of Frequen- Standard Electronic Assembly 2A2A5. The lowing paragraph describes the operation of e circuit in detail.

199. The 5-mc input signal from the com- rator circuit is coupled to the base of 10 mc plifier Q4 by capacitor C17. Bias for the se of amplifier Q4 is provided by voltage ider R15, R16. Resistor R14 is the emit- resistor, which is rf bypassed by capaci- C15. The output tuned circuit consisting of e primary of transformer T4 and capacitor 6, is tuned to 10 mc. Since this stage is biased to produce non-linear amplification, the second harmonic (10 mc) of the 5-mc signal is produced and amplified. The 10-mc signal is coupled through transformer T4 and applied to the 17.847/27.847 mc mixer.

4-200. 5 MC MULTIPLY-BY-TWO, TEST DATA. Pertinent references and applicable test data for the 5 mc multiply-by-two circuit are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. RF Translator Electronic Subassembly, Servicing Block Diagram, Figure 4-74.

c. Frequency Standard Electronic Assembly, Schematic Diagram, Figure 5-9.

d. Refer to paragraph 2-25 in Technical Manual for Repair of AN/WRC-1 and R-1051/ URR 2N Modules, NAVSHIPS 95700, for 5 mc multiply-by-two adjustment procedures.

e. Required Test Equipment:

(1) Electronic Multimeter, CCVO-91CA.

(2) Multimeter, AN/PSM-4.

(3) RF Signal Generator, CAQI-606A.

(4) Frequency Standard Test Set, TS-2134/WRC-1.

f. 5 MC Multiplier, Divider, and Comparator, Component and Test Point Location, Figure 5-71.

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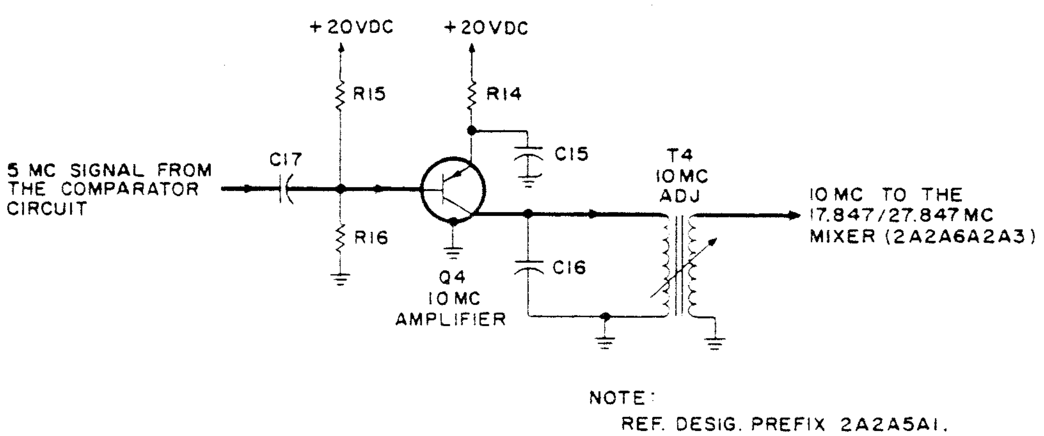


Figure 4-42. 5 MC Multiply-by-Two, Simplified Schematic Diagram

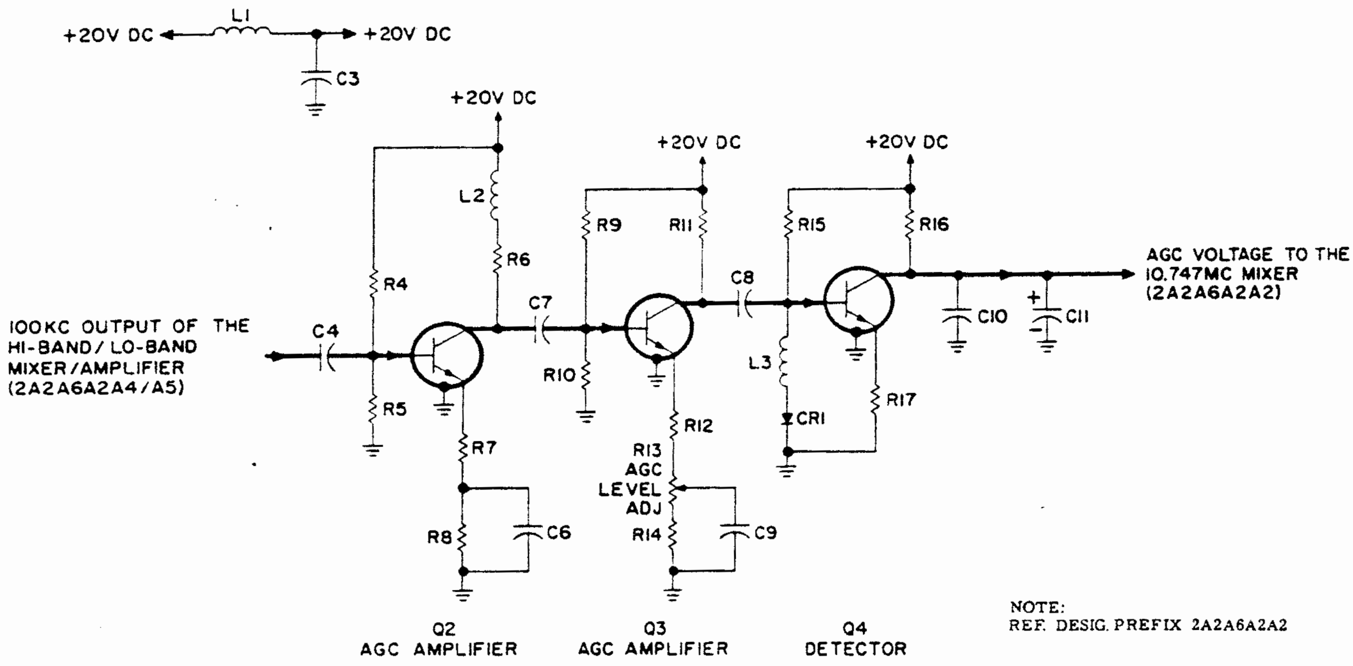


Figure 4-41. 10.747 MC Mixer AGC, Simplified Schematic Diagram

degeneration to flatten the frequency response and provide stability. Resistor R8 is the emitter resistor, which is rf bypassed by capacitor C6. The output of agc amplifier Q2 is developed across resistor R6 and inductor L2 and is coupled to the base of agc amplifier Q3 by capacitor C7.

4-195. Voltage divider R9, R10 derives bias voltage for agc amplifier Q3 from the positive 20-vdc supply line. Resistors R12 and R13 develop degeneration for increasing stability and controlling the agc loop gain. The gain of agc amplifier Q3 is set by adjusting potentiometer R13. Resistor R14 is the emitter resistor, which is rf bypassed by capacitor C9. The output of agc amplifier Q3 is developed across resistor R11 and is coupled to the base of detector Q4 by capacitor C8.

4-196. Resistor R15, inductor L3, and diode CR1 derive bias voltage for detector Q4 from the positive 20-vdc supply line. Inductor L3 provides a high ac input impedance and a low dc resistance. This prevents any output loading of agc amplifier Q3. Diode CR1 compensates for temperature variations in the base-to-emitter circuit of detector Q4. Resistor R17 provides a small amount of degeneration to improve the stability of detector Q4. With no signal applied, detector Q4 is non-conducting. The positive portions of the applied signal forward-bias the base-to-emitter diode of detector Q4, causing current to flow. Capacitor C11 starts to charge to the 20 vdc when there is no collector current in detector Q4. When collector current starts to flow, the collector voltage drops, causing capacitors C10 and C11 to discharge through transistor Q4. Once the output of agc amplifier Q3 reaches a steady-state condition, each input cycle sustains the charge on capacitors C10 and C11, preventing fluctuations in the dc output voltage. Since this circuit forms a closed loop with all the other circuits of the 100 KC Synthesizer Electronic Subassembly, the gain of all circuits will reach a steady state condition, thus maintaining constant outputs from detector Q4, and hi-band/lo-band mixer/amplifier 2A2A6A2A4/A5, respectively.

4-197. 10.747 MC MIXER AGC, TEST DATA. Pertinent references and applicable test data for the 10.747 mc mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 100 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-79.

c. 100 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-11.

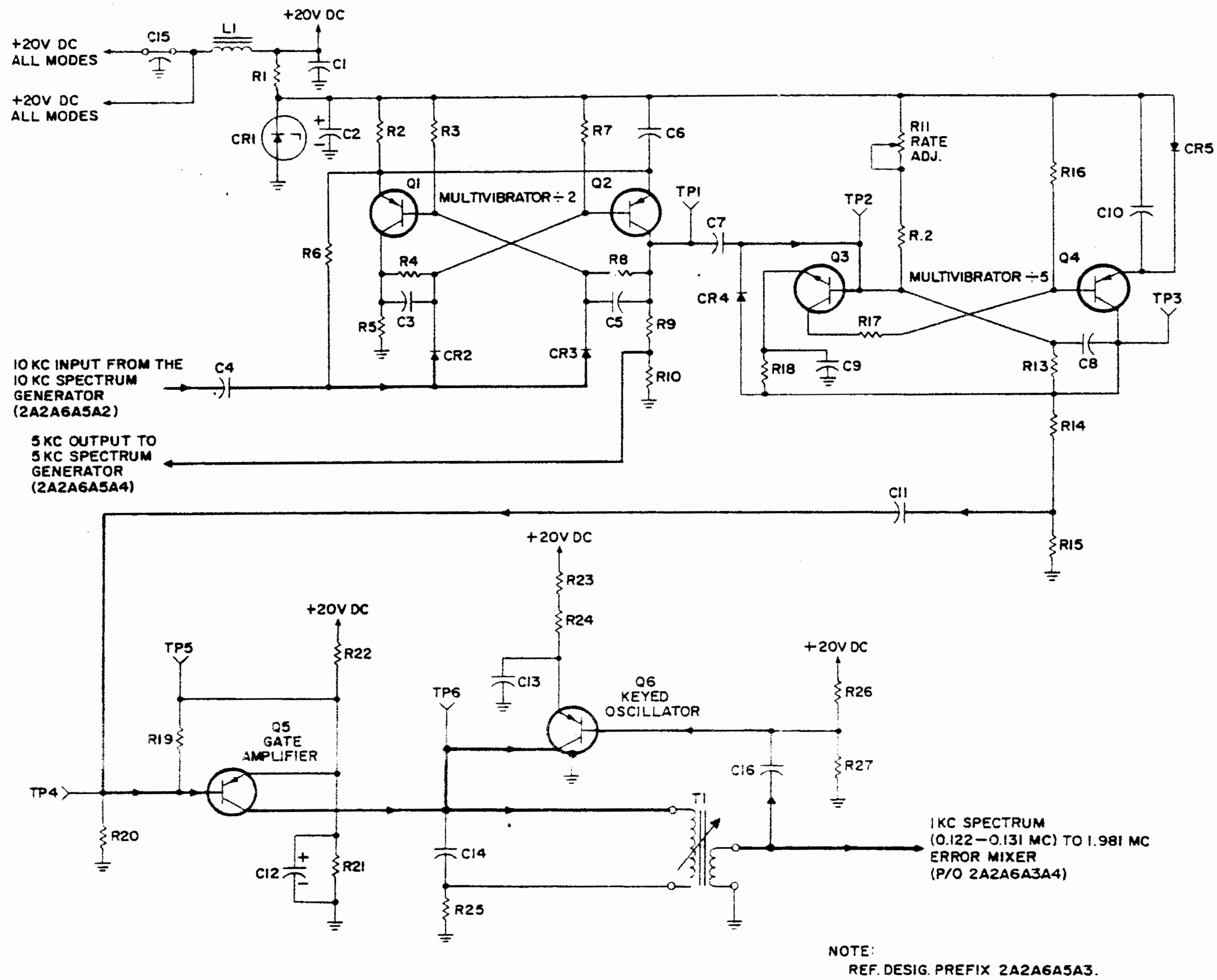


Figure 4-45. 1KC Spectrum Generator, Simplified Schematic Diagram

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-27c in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 1 kc spectrum generator adjustment procedures.

d. 1 KC Spectrum Generator, Component and Test-Point Location, Figure 5-103.

4-216. 1.981 MC ERROR MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The 1.981 mc error mixer (figure 4-46) consists of an isolation amplifier (Q7), a mixer (Q10), and a 1.981 mc filter (FL2). These circuits, which form a part of the 1 and 10 KC Synthesizer Electronic Subassembly 2A2A6A3, mix the output signal from the 1.850 to 1.859 mc oscillator with one of the 1-kc spectrum points to produce the 1.981-mc product signal for use in the 7.089 mc mixer. The following paragraphs describe the operation of the circuits in detail.

4-217. The signal from the 1.850 to 1.859 mc oscillator is coupled through capacitor C30 to the emitter of isolation amplifier Q7. The grounded base configuration of isolation amplifier Q7 provides high reverse attenuation to the spectrum and mixer products present in mixer Q10. Base bias is provided by voltage divider R29, R27. Resistor R12 and capacitor C13 provide decoupling for isolation amplifier Q7. Capacitor C29 provides ac ground to the

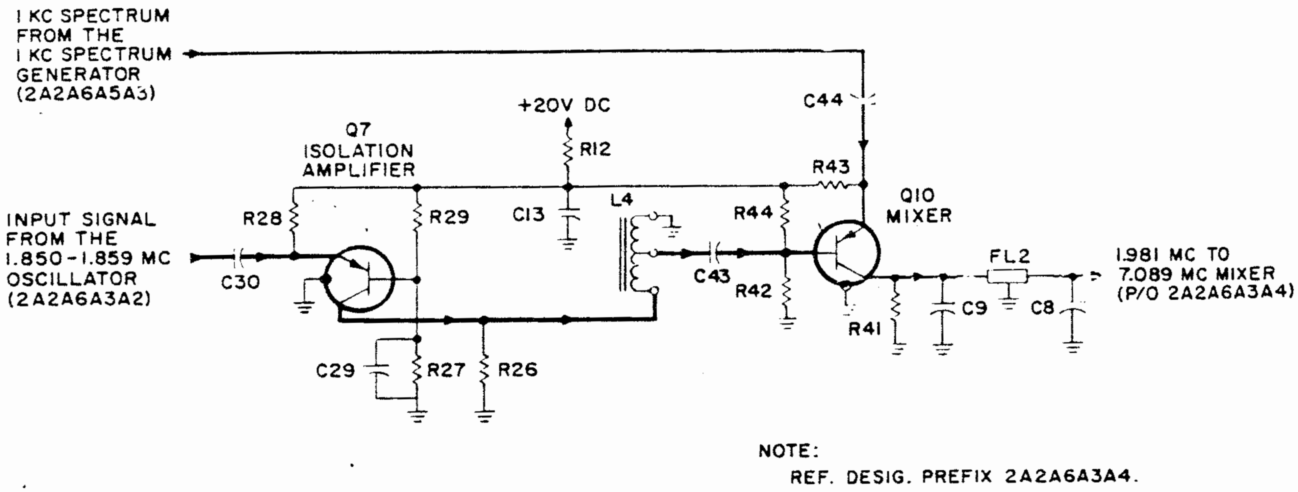


Figure 4-46. 1.981 MC Error Mixer, Simplified Schematic Diagram

base of isolation amplifier Q7. The output of isolation amplifier Q7 is applied to inductor L4. Inductor L4 provides the impedance transformation necessary to drive mixer Q10. The output of inductor L4 is coupled through capacitor C43 to the base of mixer Q10. Resistor R26 is used to ensure uniformity of the signal developed across inductor L4. Base bias is provided by voltage divider R44, R42. Resistor R12 and capacitor C13 also provide decoupling for mixer Q10. The 1-kc spectrum is coupled through capacitor C44 to the emitter of mixer Q10. The mixing products on the collector of mixer Q10 are applied to crystal filter FL2 where all products except the sum (1.981 mc) are attenuated. Resistor R41 and capacitor C9 form the input termination of crystal filter FL2 while capacitor C8 forms a part of the filter output termination. The output of rystal filter FL2 is applied to the 7.089 mc mixer.

4-218. 1.981 MC ERROR MIXER, TEST DATA. Pertinent references and applicable test data for the 1.981 mc error mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 and 10 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-78.

c. 1 and 10 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-12.

d. 7.089 MC Mixer, Component and Test Point Location, Figure 5-96.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-41CA.

(3) Frequency Meter, CAQI-524D.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

4-219. 9.07 MC ERROR MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The 9.07 mc error mixer (figure 4-47) consists of an isolation amplifier (Q6), a mixer (Q8), and a 9.07 mc filter (FL1). These circuits, which form a part of 1 and 10 KC Synthesizer Electronic Subassembly 2A2A6A3, mix the output signal from the 5.16 to 5.25 mc oscillator with one of the 10-kc spectrum points to produce the 9.07-mc product signal for use in the 7.089 mc mixer. This circuit is identical (except for a few component values) to the 1.981 mc error mixer. Refer to paragraph 4-217 for details of circuit operation.

4-220. 9.07 MC ERROR MIXER, TEST DATA. Pertinent references and applicable test data for the 9.07 mc error mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

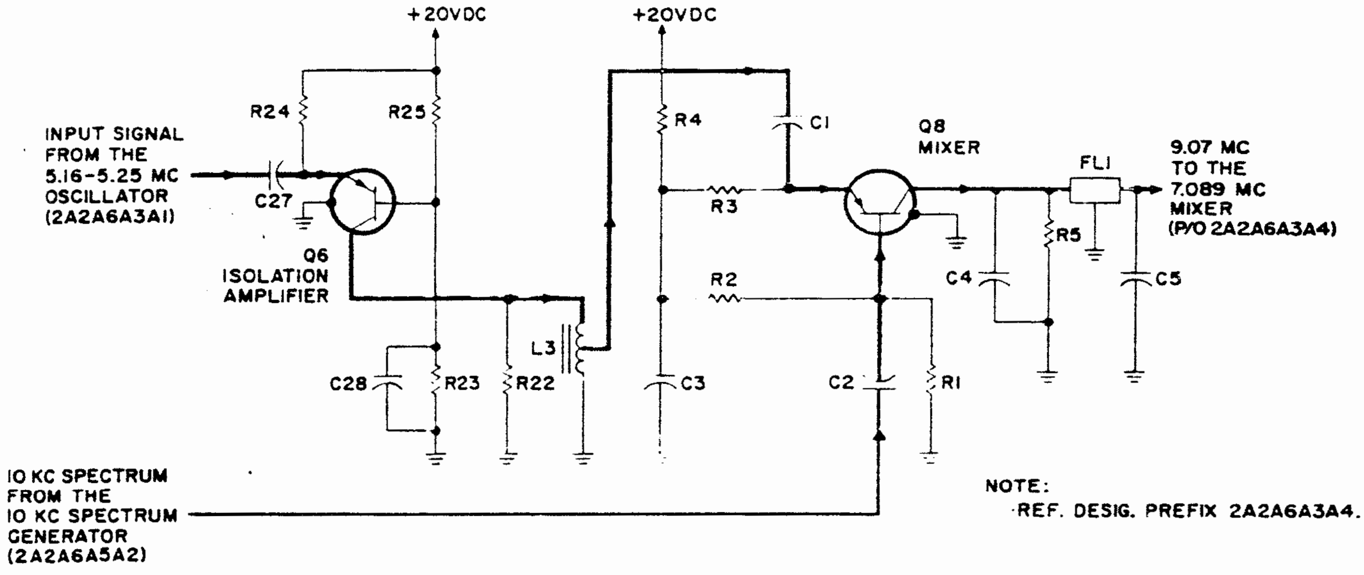


Figure 4-47. 9.07 MC Error Mixer, Simplified Schematic Diagram

b. 1 and 10 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-78.

c. 1 and 10 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-12.

d. 7.089 MC Mixer, Component and Test Point Location, Figure 5-96.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Frequency Meter, CAQI-524D.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

4-221. 7.089 MC MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. Mixer Q9 circuit (figure 4-48), which forms a part of 1 and 10

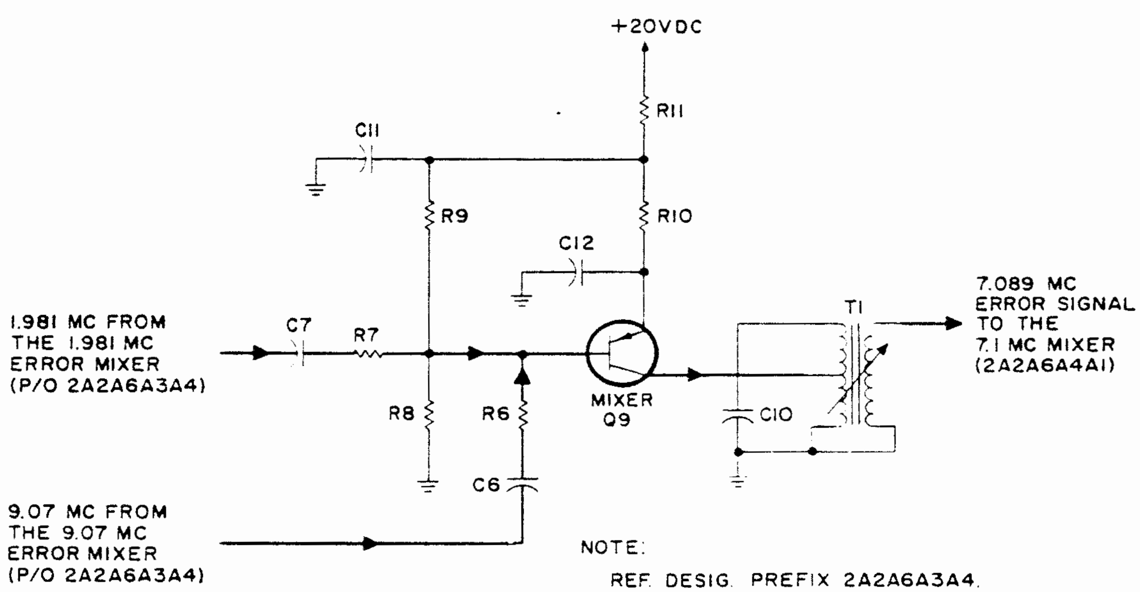


Figure 4-48. 7.089 MC Mixer, Simplified Schematic Diagram

KC Synthesizer Electronic Subassembly 2A2A6A3, mixes the 1.981-mc signal from the 1.981 mc error mixer with the 9.07-mc signal from the 9.07 mc error mixer to produce the 7.089 mc error signal for use in the 7.1 mc mixer of 500 CPS Synthesizer Electronic Subassembly 2A2A6A4. The following paragraphs describe the operation of the circuit in detail.

4-222. The 1.981-mc signal is coupled through capacitor C7 and isolating resistor R7 to the base of mixer Q9. The 9.07-mc signal is coupled through capacitor C6 and isolating resistor R6 to the base of mixer Q9. Since the outputs of the 1.981 mc error mixer and the 9.07 mc error mixer are combined at the base of mixer Q9, the output termination for the corresponding mixer filters is located in the 7.089 mc mixer. This termination consists of resistors R6 and R7, capacitors C5 (figure 4-47), C6, C7, and C8 (figure 4-46), and the input impedance of mixer Q9, and the output impedance of the respective filters. Voltage divider R9, R8 provides base bias for mixer Q9. Resistor R11 and capacitor C11 provide decoupling for mixer Q9. The output circuit of mixer Q9 is a 7.089-mc tuned circuit consisting of capacitor C10 and transformer T1. All mixing products except the difference frequency (7.089 mc) are attenuated by the output circuit of mixer Q9. The 7.089-mc signal is coupled through transformer T1 to the 7.1 mc mixer circuit in 500 CPS Synthesizer Electronic Subassembly 2A2A6A4.

4-223. 7.089 MC MIXER, TEST DATA. Pertinent references and applicable test data for the 7.089 mc mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 1 and 10 KC Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-78.

c. 1 and 10 KC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-12.

d. 7.089 MC Mixer Components and Test-Point Location, Figure 5-96.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Frequency Meter, CAQI-524D.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-28 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 7.089 mc error mixer adjustment procedures.

4-224. 5 KC SPECTRUM GENERATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 5 kc spectrum generator (figure 4-49) consists of an emitter follower (Q1), a gate amplifier (Q2), and a keyed oscillator (Q3). These circuits, which form a part of Spectrum Generator Electronic Subassembly 2A2A6A5, produce a 0.110-to-0.115-mc frequency spectrum which is supplied to 500 cps oscillator 2A2A6A4A3 for use in the automatic phase-lock Loop. The 5 kc spectrum generator is used in all modes of operation. The following paragraphs describe the operation of the 5 kc spectrum generator in detail.

4-225. The input to the 5 kc spectrum generator is the 5-kc pulsed output of the 1 kc spectrum generator. The 5-kc input signal is coupled to the base of emitter follower Q1. Voltage divider R1, R2 and emitter resistors R4 and R6 develop bias voltage for emitter follower Q1 from the positive 20 vdc obtained from main frame power supply 2A2A8. Emitter Follower Q1 prevents loading on the multivibrator in 1 kc spectrum generator assembly 2A2A6A5A3 and provides a low-impedance source for gate amplifier Q2. The output of emitter follower Q1 is coupled to the base of gate amplifier Q2 by capacitor C3. Gate amplifier Q2 is identical to gate amplifier Q4 in the 100 kc spectrum generator (refer to paragraph 4-185). Gate amplifier Q2 turns keyed oscillator Q3 on and off at a 5-kc repetition rate. Keyed oscillator Q3 is identical to keyed oscillator Q5 in the 100 kc spectrum generator (refer to paragraph 4-186). The output of keyed oscillator Q3 is a 100-microsecond sinusoidal burst of frequencies with a 5-kc repetition rate. This results in a 0.110-to-0.115-mc frequency spectrum. The output of keyed oscillator Q3 is applied to 500 CPS Synthesizer Electronic Subassembly 2A2A6A4.

4-226. 5 KC SPECTRUM GENERATOR, TEST DATA. Pertinent References and applicable test data for the 5 kc spectrum generator are as follows:

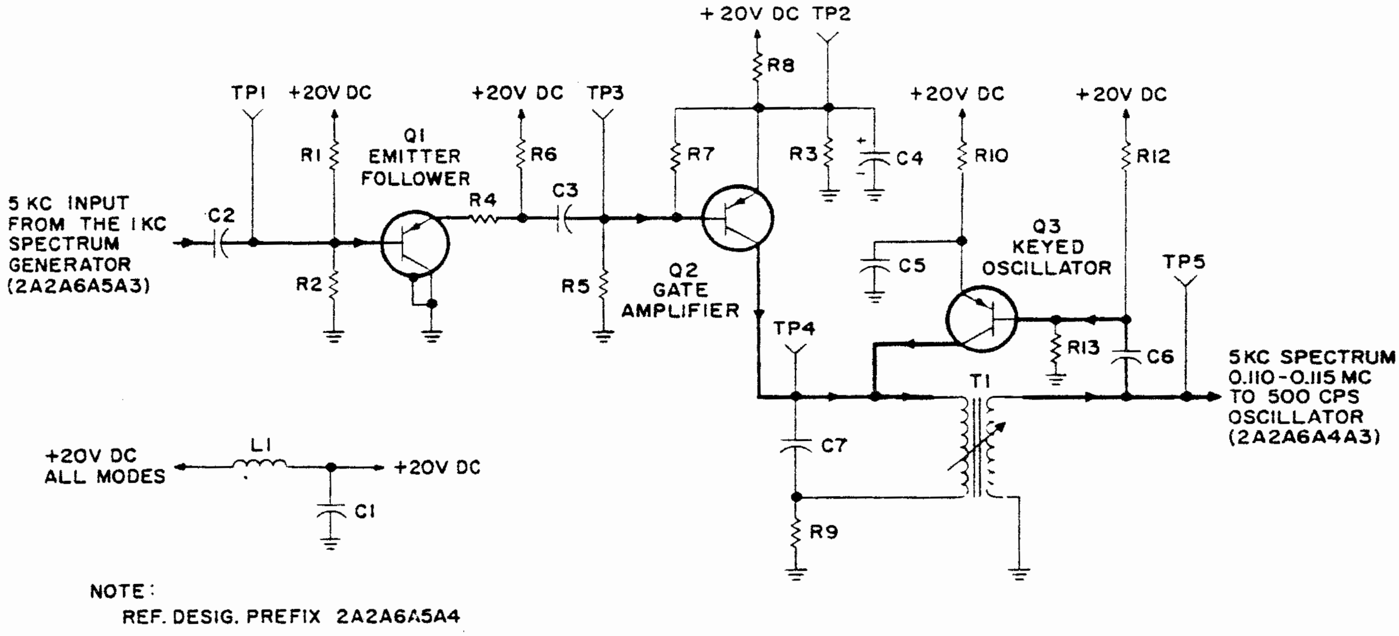


Figure 4-49. 5 KC Spectrum Generator, Simplified Schematic Diagram

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Spectrum Generator Electronic Subassembly, Servicing Block Diagram, Figure 4-81.

c. Spectrum Generator Electronic Subassembly, Schematic Diagram, Figure 5-14.

d. 5 KC Spectrum Generator, Component and Test Point Location, Figure 5-108.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Oscilloscope, AN/USM-105A.

(4) Frequency Meter, CAQI-524D.

(5) Multimeter, AN/PSM-4.

(6) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-27d in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 5 kc spectrum generator adjustment procedures.

4-227. 500 CPS OSCILLATOR, FUNCTIONAL CIRCUIT DESCRIPTION. The 500 cps oscillator (figure 4-50) consists of a Clapp oscillator (Q1, Q2), three emitter followers (Q3, Q5 and Q6), two amplifiers (Q4 and Q7), and a phase detector (CR8, CR9 and T1). The 500 cps oscillator, which forms a part of 500 CPS Synthesizer Electronic Subassembly 2A2A6A4, produces either a locked 110-kc or a locked 115-kc signal for driving the divide-by-ten multivibrators (2A2A6A4A2). These circuits are used in all modes of operation. The following paragraphs describe the operation of the 500 cps oscillator in detail.

4-228. The positive 20-vdc supply voltage for all circuits of the 500 cps oscillator is obtained from main frame power supply 2A2A8. Zener diode CR1 regulates this 20 vdc to 15 vdc for use in the circuit by drawing enough current in addition to the load current to maintain a 5 vdc drop across resistor R1. Capacitors C2 and C3 filter the regulated 15-vdc output of Zener diode CR1.

4-229. The tank circuit of Clapp oscillator Q1, Q2 consists of capacitors C4, C5, and C7 through C11, inductor L4, and voltage-variable capacitors CR2, CR3, and CR4. Voltage-variable capacitors (VVC) CR2 and CR3 are the main tuning elements of oscillator Q1, Q2. Capacitor C10 is selected to adjust the initial frequency of oscillator Q1, Q2. VVC CR4 provides the required pulling range for the phase-lock loop. Capacitor C9 compensates or the non-linear tuning characteristics of /VC CR4. Capacitor C11 has a negative tem-)erature coefficient to compensate for tempera- ure changes in oscillator Q1, Q2. The parallel ınd series combination of the aforementioned :apacitances results in a single variable capac- ty, which is designated C'. A simplified ac quivalent circuit of oscillator Q1, Q2 is in- luded in figure 4-51 as an aid in analyzing the scillator tank circuit. Figure 4-51 makes it eadily evident that capacitors C4, C5, C7, C8, ınd C' and inductor L4 form the parallel- esonant tank circuit of oscillator Q1, Q2.

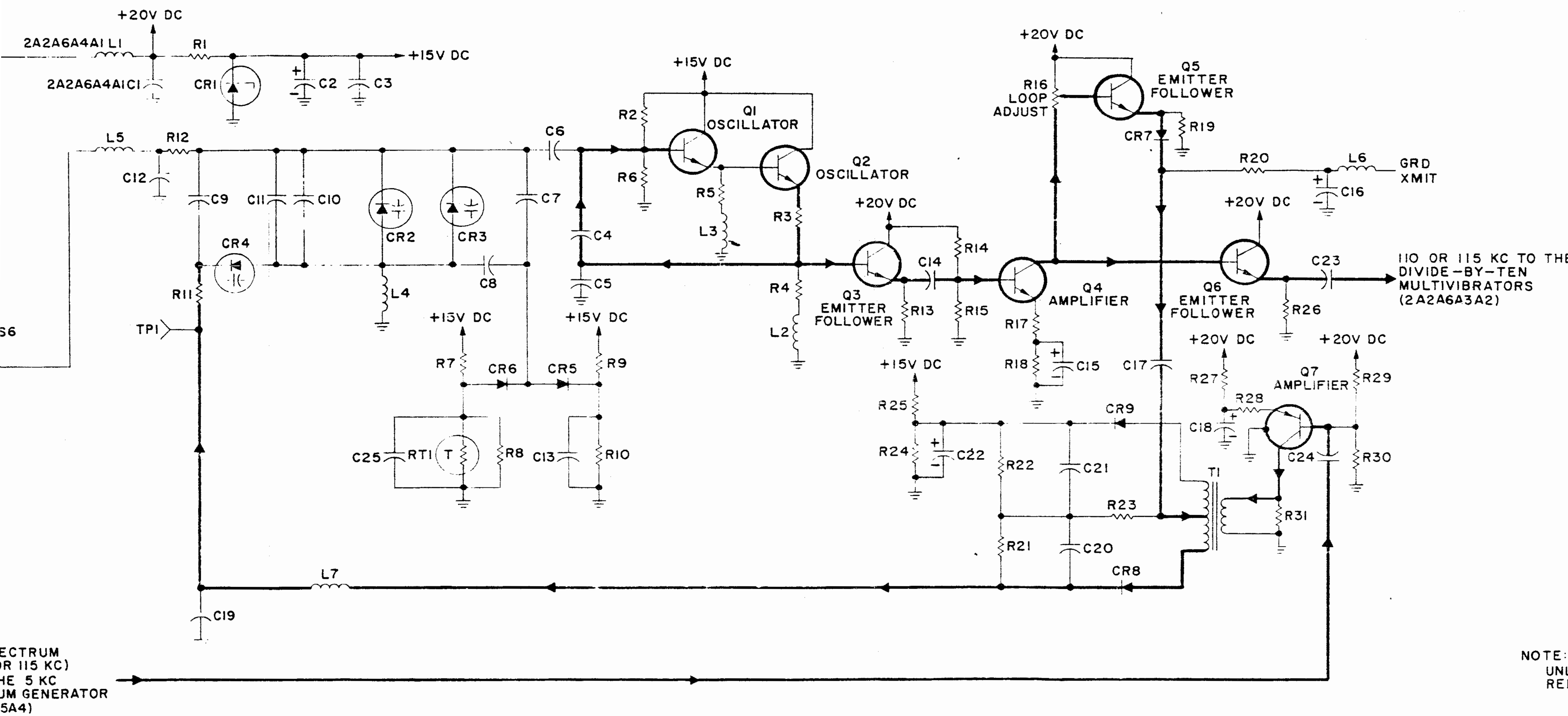
-230. The regulated 15 vdc present at Zener iode CR1 is filtered by 2A2A6A4A1 L1, A2A6A4A1 C1 and applied to a voltage divider 2A2A16R1, 2A2A16R2, 2A2A16R3) located on ıe main frame. The voltage developed across ıis voltage divider is tapped on one of two laces, depending on the setting of CPS switch 2A2S6). When the CPS switch is in the 000)sition, the voltage applied through isolating esistor R12 sets the capacitance of VVC CR2 ıd VVC CR3 to a value which tunes the output : oscillator Q1, Q2 to approximately 110 kc vhen the phase-lock loop is open) or to exactly .0 kc (when the phase-lock loop is closed). hen the CPS switch is in the 500 position, the ltage applied through isolating resistor R12 ts the capacitance of VVC CR2 and VVC CR3 a value which tunes the output of oscillator l, Q2 to 115 kc. Filter L5, C12, removes ıy spurious ac signals present on the 15-vdc ne.

-231. When operating voltage is applied to cillator Q1, Q2, the oscillator produces an tput of approximately 110 kc or 115 kc, de- nding on the setting of the CPS switch. These tput frequencies will only approximate the sired operating frequencies until the phase- ck loop is closed. Resistors R2 and R6 form voltage divider which develops the base bias r transistor Q1. Resistors R5, R3, R4 are e emitter resistors for transistors Q1 and 2, respectively. Inductors L2 and L3 pro- le a ground path for dc voltages and a high pedance for ac voltages. Capacitor C6 is a blocking capacitor. The output of oscil- or Q1, Q2 is limited by diodes CR5 and CR6. e negative-going limit of the signal is es-)lished by the anode bias (developed by volt- e divider R7, R8, RT1) minus the forward)p across diode CR6. The positive-going nit of the signal is established by the cathode ıs (developed by voltage divider R9, R10) ıs the forward drop across diode CR5. Therefore, the peak-to-peak amplitude of the signal is limited by the two established dc reference levels. The bias on diodes CR5 and CR6 is nearly equal at room temperature. As the temperature of the circuit varies, the for- ward drop of diodes CR5 and CR6 varies. This would result in variations in the output signal amplitude without temperature compensation. Thermistor RT1 varies the anode bias of diode CR6 in accordance with temperature changes. Therefore, the negative-going limit of the sig- nal is shifted so that the difference between the two dc references remains constant. This ensures that the amplitude of the signal does not vary with changes in temperature. Ca- pacitors C13 and C25 are rf bypass capacitors.

4-232. The output of oscillator Q1, Q2 is ap- plied directly to the base of emitter follower Q3, which in turn develops the signal across resistor R13. Emitter follower Q3 provides isolation for oscillator Q1, Q2, preventing succeeding stages from adversely loading the oscillator. The output of emitter follower Q3 is coupled to the base of amplifier Q4 by ca- pacitor C14. Bias voltage for amplifier Q4 is developed by voltage divider R14, R15. A small amount of degeneration is developed by unbypassed emitter resistor R17 to increase the stability of amplifier Q4. The output of amplifier Q4 is applied directly to the base of emitter follower Q6 which develops the signal across resistor R26. Emitter follower Q6 provides a low-impedance source for the divide-by-ten multivibrators. The output of emitter follower Q6 is coupled to the divide- by-ten multivibrators by capacitor C23.

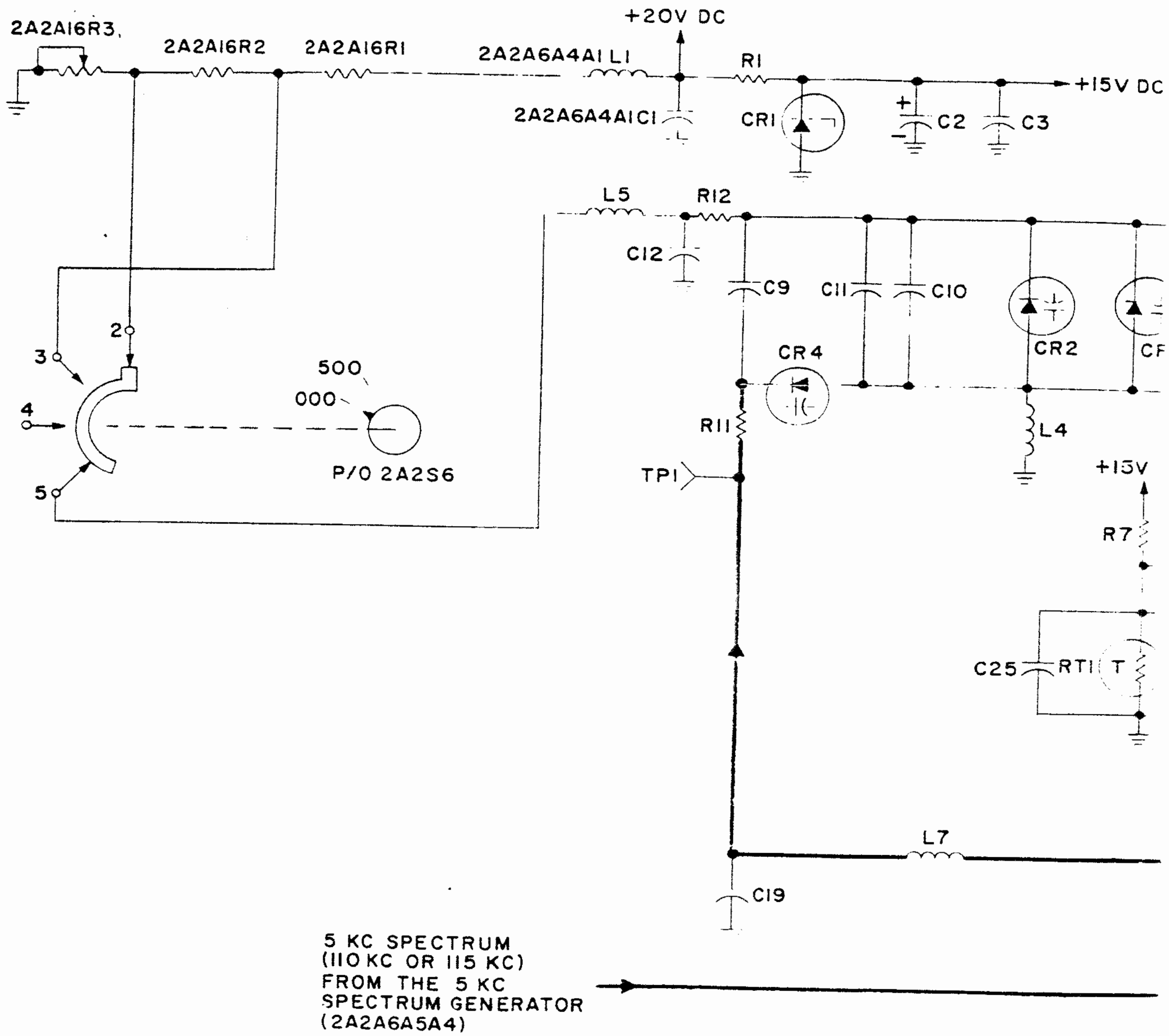
4-233. The output of amplifier Q4 is also ap- plied to the base of emitter follower Q5. Potentiometer R16 establishes the signal level at the base of emitter follower Q5 and also serves as a voltage divider for developing the base bias, thereby setting the gain of the phase- lock loop. Emitter follower Q5 provides a low-impedance source for phase-detector cir- cuit CR8, CR9, and T1. During transmit operation, a ground potential is applied through filter L6, C16 to resistor R20. Therefore, diode CR7 is forward-biased, allowing the signals developed across resistor R19 by emit- ter follower Q5 to pass. This signal is coupled to the center-tapped secondary of transformer T1 by capacitor C17.

4-234. The 5-kc spectrum output of the 5 kc spectrum generator is coupled to the base of



NOTE:
UNLESS OTHERWISE NOTED
REF. DESIG. PREFIX IS 2A2A6A4A3

Figure 4-50. 500 CPS Oscillator, Simplified Schematic Diagram


2A2A16R3
2A2A16R2
2A2A16R1
+20V DC
2A2A6A4A1 L1
R1
+15V DC
2A2A6A4A1C1
CR1
C2
C3
L5
R12
C12
C9
C11
C10
CR2
CR4
2
3
4
5
500
000
P/O 2A2S6
R11
L4
TP1
+15V
R7
C25
RT1
T
L7
C19
5 KC SPECTRUM
(110 KC OR 115 KC)
FROM THE 5 KC
SPECTRUM GENERATOR
(2A2A6A5A4)

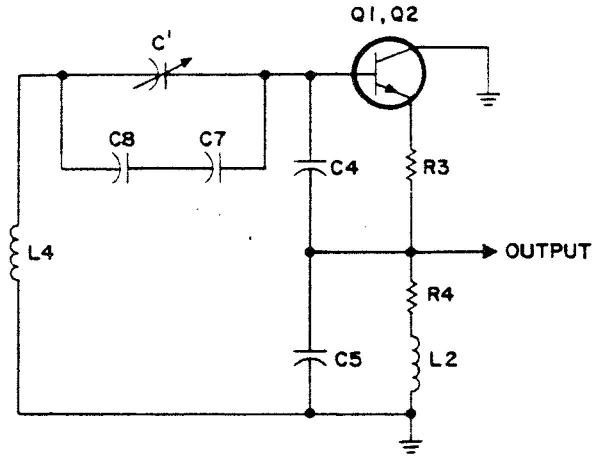


Figure 4-51. 500 CPS Oscillator, AC Equivalent Circuit, Schematic Diagram

amplifier Q7 by capacitor C24. Voltage Divider R29, R30 and emitter resistors R27, R28 develop operating voltages for amplifier Q7 from the positive 20-vdc supply. A small amount of degeneration is developed by resistor R28 to increase the stability of amplifier Q7. The output of amplifier Q7 is developed across the primary of transformer T1. Resistor R31 ensures that a uniform signal is developed across the primary of transformer T1.

4-235. The phase detector circuit compares the output of oscillator Q1, Q2 with the 5-kc spectrum generator is coupled to the base of amplifier Q7 by capacitor C24. Voltage divider R29, R30 and emitter resistors R27, R28 develop that varies about the circuit dc reference. This ac function varies the capacitance of VVC CR4, causing the oscillator frequency to This a-c function varies the capacitance of VVC CR4, causing the oscillator frequency to sweep. As the oscillator output sweeps through the reference frequency, the output frequency of the phase detector decreases with each sweep and eventually diminishes to zero. The output of the phase detector is then a dc level which locks the output of the oscillator to the frequency standard. Whenever the oscillator begins to drift. the phase difference is detected by the phase detector and the dc potential applied to VVC CR4 is shifted accordingly to hold the oscillator on frequency.

4-236. The phase detector circuit is referenced at a dc potential which is developed by voltage divider R25, R24. This dc reference (voltage across resistor R24) is applied to the cathode of diode CR9. Since there is no other dc path in the phase detector circuit, this level references the output at the cathode of diode CR8 to the same dc potential. Capacitor C22 serves as a bypass for resistor R24. The oscillator output signal is developed across resistor R23. The 5-kc spectrum output of amplifier Q7 is induced into the secondary of transformer T1. The secondary of transformer T1 provides a balanced output from amplifier Q7 and also forms part of the phase-detector circuit. Each half of the balanced output is composed of a diode (CR8 or CR9), a resistor (R21 or R22), and a capacitor (C21 or C20) with a common path through resistor R23. The center-tapped secondary of transformer T1 is the common path for the signals in the circuit. Since the output of transformer T1 is balanced, the net dc current through resistor R23 is zero. In the absence of an oscillator signal, the net voltage from the cathode of diode CR8 to the cathode of diode CR9 is also zero. With an oscillator signal present, this net voltage remains at approximately zero, unless the oscillator frequency is nearly coincident with the 5-kc spectrum reference frequency. When the oscillator and 5 kc spectrum frequencies are nearly coincident, the net output voltage across resistors R21 and R22 becomes a time-varying function with a frequency equal to the difference between the oscillator frequency and the 5-kc spectrum frequency. In order for oscillator Q1, Q2 to be locked, the difference between the oscillator frequency and the 5-kc spectrum reference frequency must be zero.

4-237. Assume that the output of the oscillator is 110.4 kc. The desired oscillator output is 110 kc. The 5-kc spectrum contains the two spectrum points, 110 kc and 115 kc. The 110.4 kc and 115 kc are not coincident enough to materially change the net voltage between diodes CR8 and CR9. However, the 110.4 kc is in close coincidence with the 110-kc spectrum point. This causes a 400-cps ac output from the phase detector circuit. The ac output of the phase detector varies the capacity of VVC CR4 by varying the applied voltage above and below the dc reference, thus sweeping the oscillator accordingly. Since the loop is closed, this frequency decreases with time due to the decrease of the oscillator output frequency as it is being swept. After this sweep frequency has been decreased to a frequency within the pull-in range of the oscillator, the oscillator pulls in and locks at the desired 110 kc. At this time the output of phase detector CR8 and CR9 is the dc reference level. If the phase of the oscillator begins to drift, the phase difference is detected by the phase detector circuit and the dc output is shifted accordingly to correct the oscillator frequency. The network composed of inductor L7 and capacitor C19 serves as a filter for the output of the phase-detector circuit.

4-238. A vector diagram of the operation of the phase detector circuit is shown in figure 4-52. Consider first the series circuit composed of R23, C21, and C22, across which oscillator Q1, Q2 develops its output (see figure 4-52a). At frequencies near 110 kc, the reactance of capacitor C21 is approximately 145 ohms and the reactance of capacitor C22 is approximately 0.65 ohms. Therefore, nearly all the signal from oscillator Q1, Q2 is developed across resistor R23. Next, consider the situation when the oscillator frequency equals the 110-kc spectrum point. Potentials E_{ao} and E_{bo} then have amplitudes and phases

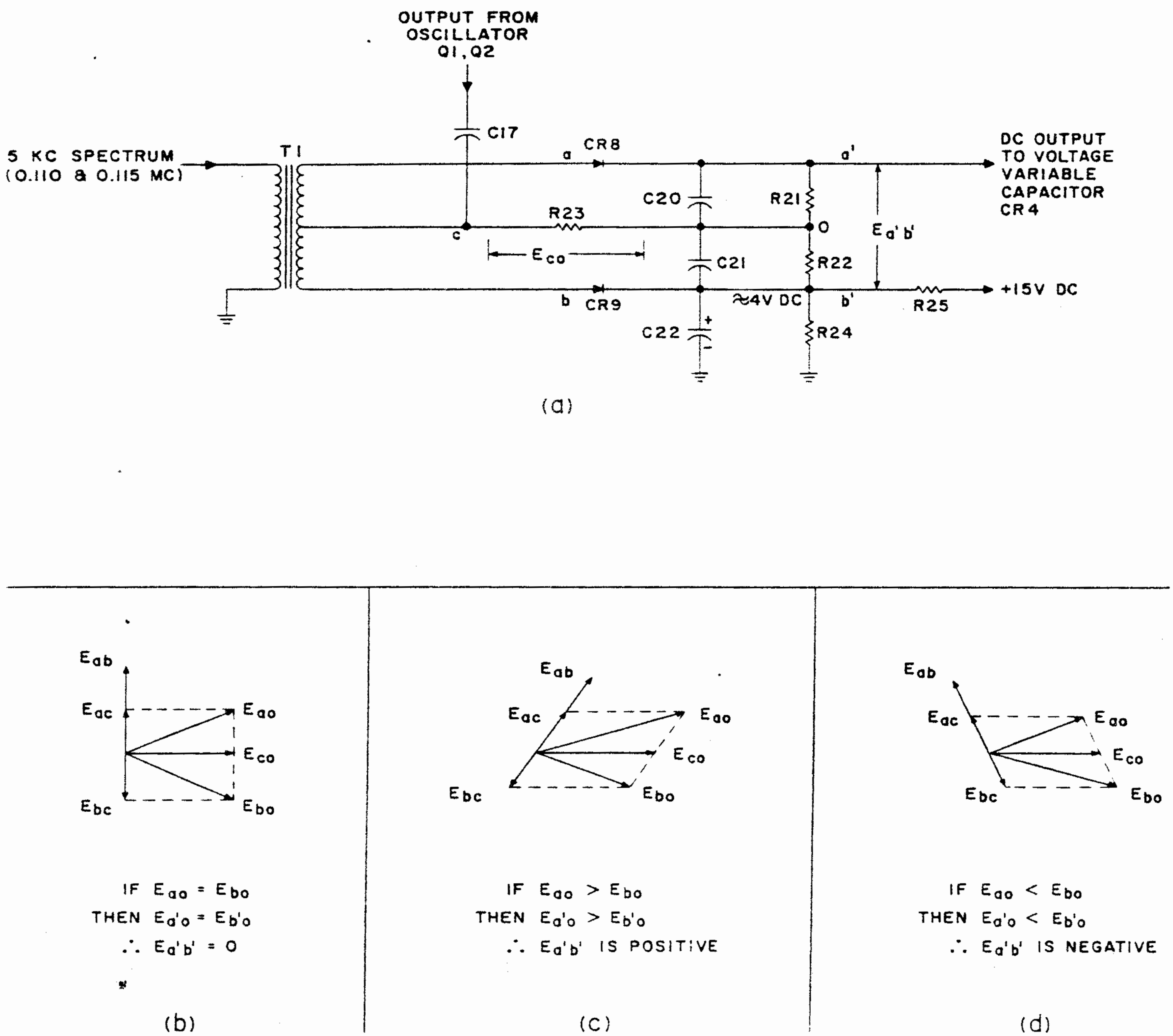


Figure 4-52. Phase Detector, Vector Diagram

similar to those illustrated in figure 4-52b. Since $E_{ao} = E_{bo}$, then $E_{a'o} = E_{b'o}$. Therefore, $E_{a'b'} = O$. When the phase difference between the oscillator and the 110-kc spectrum points is positive, (oscillator output greater than the spectrum point), E_{ao} and E_{bo} have amplitudes and phases as illustrated in figure 4-52c. Since $E_{ao} > E_{bo}$, then $E_{a'o} > E_{b'o}$. Therefore, $E_{a'b'}$ is positive. When the phase difference between the oscillator and the 110-kc spectrum point is negative (oscillator output less than the spectrum point), E_{ao} and E_{bo} have amplitudes and phases as illustrated in figure 4-52d. Since $E_{ao} < E_{bo}$, then $E_{a'o} < E_{b'o}$. Therefore, $E_{a'b'}$ is negative. The preceeding discussion also holds true if the desired oscillator output is 115 kc.

4-239. 500 CPS OSCILLATOR, TEST DATA. Pertinent references and applicable test data for the 500 cps oscillator are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 500 CPS Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-82.

c. 500 CPS Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-13.

d. 500 CPS Oscillator, Component and Test Point Location, Figure 5-103.

e. Transmitter 500 Cycle Control, Component Location, Figure 5-32.

f. Required Test Equipment:

(1) Frequency Meter, CAQI-524D.

(2) Oscilloscope, AN/USM-105A.

(3) Heterodyne Voltmeter, Bruel and Kjaer, 2005.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

g. Refer to paragraph 3-30 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 500 cps oscillator adjustment procedures.

4-240. DIVIDE-BY-TEN MULTIVIBRATORS, FUNCTIONAL CIRCUIT DESCRIPTION. The divide-by-ten multivibrators circuit (figure 4-53) consists of a shaping amplifier (Q9), a divide-by-five circuit (Q1, Q2, Q3, Q4, Q5, and Q6), and a divide-by-two circuit (Q7 and Q8). These circuits, which form a part of 500 CPS Synthesizer Electronic Subassembly 2A2A6A4, divide the 110-kc or 115-kc output from 500 cps oscillator 2A2A6A4A3 by ten to provide the 11-kc or 11.5-kc signal required for mixing in 7.1 mc mixer 2A2A6A4A1. These curcuits are used in all modes of operation. The following paragraphs describe the operation of the divide-by-ten multivibrators in detail.

4-241. The operating voltage for the divide-by-ten multivibrators is the positive 10-vdc output from Zener diode CR1. Zener diode CR1 regulates the positive 20-vdc output from main frame power supply 2A2A8 to 10 vdc by drawing enough current in addition to the load current to maintain a 10-vdc drop across resistor R1. Capacitor C1 and inductor L1 filter the 20-vdc input to Zener diode CR1 and capacitor C2 filters the positive 10-vdc output from Zener diode CR1.

4-242. The locked 110-kc or 115-kc sinusoidal output from the 500 cps oscillator is the input signal for the divide-by-ten multivibrators. This signal is coupled to the base of shaping amplifier Q9 by capacitor C3. Resistors R3, R4, and R6 comprise a resistive network for developing the required operating voltages for shaping amplifier Q9. With no signal input, diode CR2 holds amplifier Q9 at cutoff. As a result, a small input signal overdrives shaping amplifier Q9. Diode CR2 clamps the positive portions of the input signal. Resistor R2 provides isolation for the input signal and capacitor C4 reduces the transistor storage time, thus, increasing the switching speed. Due to the clamping action of diode CR2, the negative portions of the input signal will drive shaper amplifier Q9 into saturation. The resulting negative-going pulses are inverted by shaping amplifier Q9, and are developed across resistor R5. These positive pulses are coupled to steering diodes CR3 and CR4 by capacitor C6.

4-243. Transistors Q1, Q2, Q3, Q4, Q5, and Q6 comprise three sta[illegible]ard bistable multivibrators, which are c[illegible]ected in a configuration

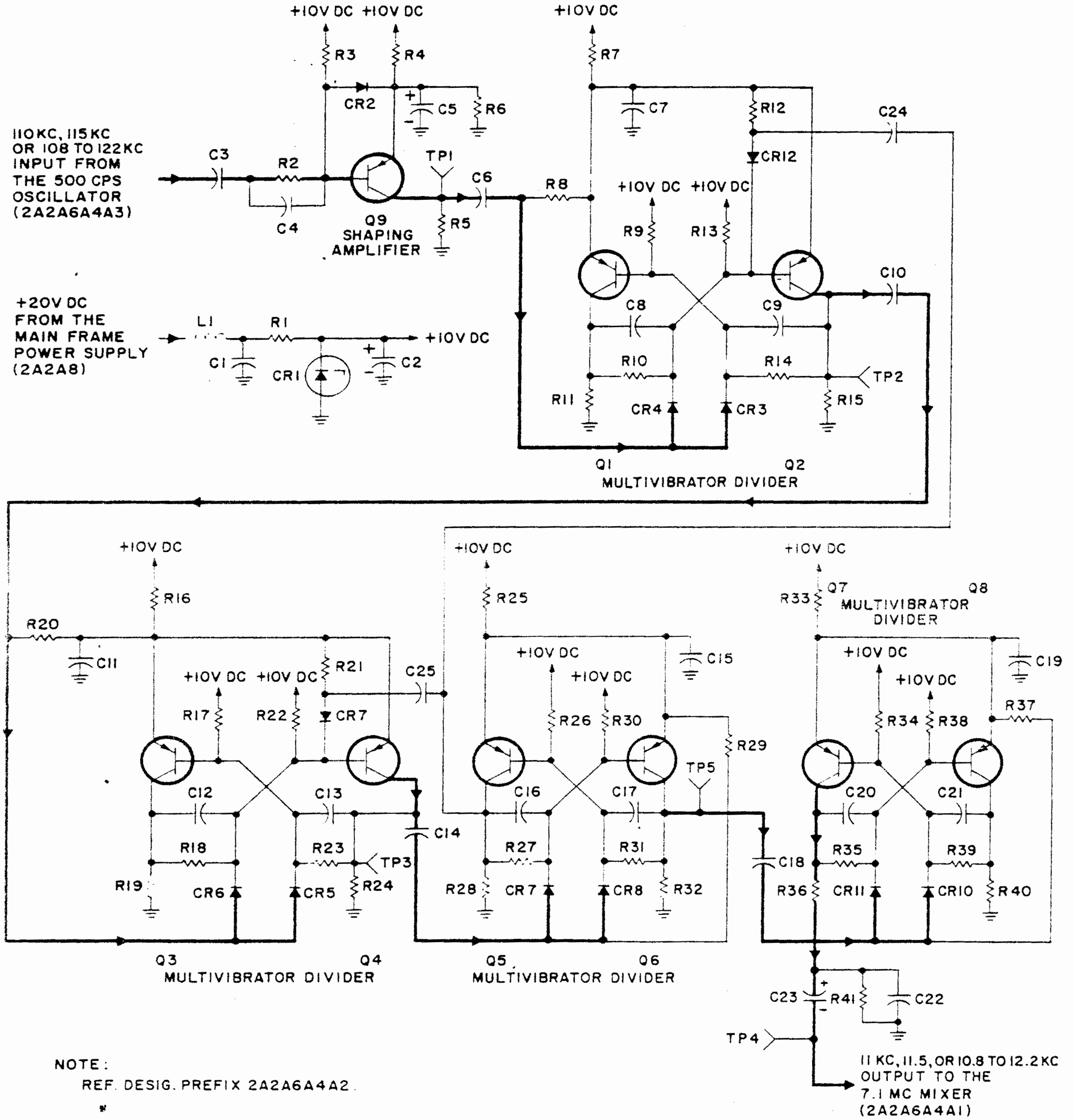


Figure 4-53. Divide-By-Ten Multivibrator, Timing Diagram

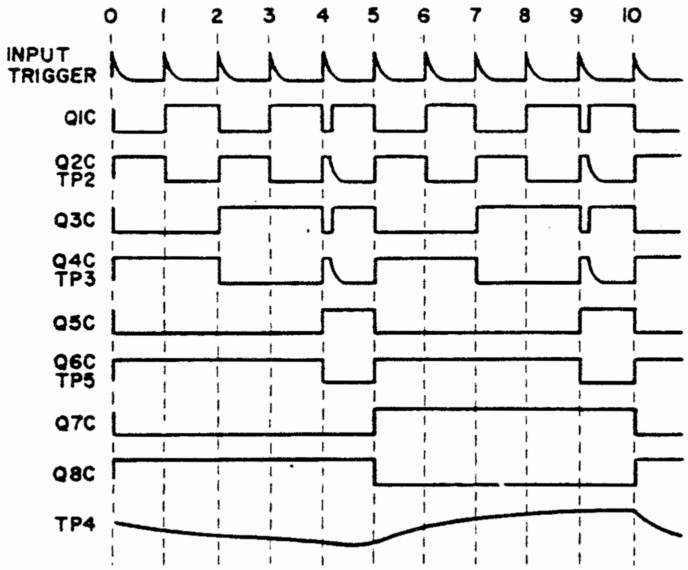


Figure 4-54. Divide-by-Ten Multivibrator, Timing Diagram

employing a feedback loop, to divide the input signal by five. Bistable multivibrator Q7, Q8 divides the output from this circuit by two. See figure 4-54 and table 4-1 during the following discussion.

4-244. Assume that transistors Q1 through Q8 are in the condition shown in the start condition line of table 4-1. The first input pulse from shaping amplifier Q9 is differentiated by capacitor C6 and the input impedance of multivibrator Q1, Q2. The resulting positive trigger pulse switches transistor Q2 to cutoff and transistor Q1 to saturation, producing a negative pulse on the collector of transistor Q2. This pulse is differentiated by capacitor C10 and the input impedance of multivibrator Q3, Q4. This back-biases steering diodes CR5 and CR6, preventing any input to multivibrator Q3, Q4. Therefore, the remaining transistors of the divide-by-ten multivibrators circuit do not change condition (pulse 1 line of table 4-1). The second input pulse to multivibrator Q1, Q2 is differentiated, and the resulting positive trigger pulse switches transistor Q1 to cutoff and transistor Q2 back into saturation, producing a positive pulse on the collector of transistor Q2. This pulse is differentiated, producing a positive trigger pulse, which switches transistor Q4 to cutoff and transistor Q3 to saturation. The negative pulse on the collector of transistor Q4 is differentiated by capacitor C14 and the input impedance of multivibrator Q5, Q6. This back-biases steering diodes CR8 and CR9. Therefore, the remaining transistors of the divide-by-ten multivibrators do not change condition (pulse 2 line of table 4-1). The third input pulse to multivibrator Q1, Q2 switches transistor Q2 to cutoff and transistor Q1 to saturation, producing another negative pulse on the collector of transistor Q2. Therefore, there is no further change in the remaining transistors of the divide-by-ten multivibrators (pulse 3 line of table 4-1). The fourth input pulse to multivibrator Q1, Q2 switches transistor Q1 to cutoff and transistor Q2 to saturation. The positive pulse on the collector of transistor Q2 is differentiated, and the resulting positive trigger pulse switches transistor Q3 to cutoff and transistor Q4 to saturation. The positive pulse on the collector of transistor Q4 is differentiated, and the resulting positive trigger pulse switches transistor Q6 to cutoff and transistor Q5 to saturation. The negative pulse on the collector of transistor Q6 is differentiated by capacitor C18 and the input impedance of multivibrator Q7, Q8. This back-biases steering diodes CR10 and CR11. Therefore, transistors Q7 and Q8 do not change condition (pulse 4 line of table 4-1). When the fourth input pulse is applied to the multivibrator Q1, Q2, transistor, Q5 is switched to saturation. The positive pulse on the collector of transistor Q5 is differentiated by capacitor C25 and the input impedance of multivibrator Q3, Q4. The resulting positive trigger pulse is applied through diode CR7 to the base of transistor Q4, switching transistor Q4 to cutoff and transistor Q3 to saturation. The positive-going pulse on the collector of transistor Q5 is also differentiated by capacitor C24 and the input impedance of multivibrator Q1, Q2. The resulting positive trigger pulse is applied through diode CR12 to the base of transistor Q2, switching transistor Q2 to cutoff and transistor Q1 to saturation. Transistors Q1 through Q8 are now in the conditions shown in the feedback line of table 4-1. The fifth pulse applied to multivibrator Q1, Q2 causes changes in all four of the multivibrators as shown in the fifth line of table 4-1. Transistors Q1 through Q6 are now in the same condition they were in prior to the application of the input pulses. Thus, the input signal is divided by five by transistors Q1 through Q6. The sixth, seventh, eighth, and ninth input pulses to multivibrator Q1, Q2 causes the same changes in circuit conditions for transistors Q1 through Q6 as previously explained for input pulses 1 through 4, respectively (lines 6, 7, 8, 9, and feedback of table 4-1). The tenth input pulse to multivibrator Q1, Q2 (like the fifth input pulse) switches transistors Q1 through

TABLE 4-1. DIVIDE-BY-TEN MULTIVIBRATORS, TIMING CHART

PULSE NUMBER	TRANSISTOR							
	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
START CONDITION	OFF	ON	OFF	ON	OFF	ON	OFF	ON
1	ON	OFF	OFF	ON	OFF	ON	OFF	ON
2	OFF	ON	ON	OFF	OFF	ON	OFF	ON
3	ON	OFF	ON	OFF	OFF	ON	OFF	ON
4	OFF	ON	OFF	ON	ON	OFF	OFF	ON
FEEDBACK	ON	OFF	ON	OFF	ON	OFF	OFF	ON
5	OFF	ON	OFF	ON	OFF	ON	ON	OFF
6	ON	OFF	OFF	ON	OFF	ON	ON	OFF
7	OFF	ON	ON	OFF	OFF	ON	ON	OFF
8	ON	OFF	ON	OFF	OFF	ON	ON	OFF
9	OFF	ON	OFF	ON	ON	OFF	ON	OFF
FEEDBACK	ON	OFF	ON	OFF	ON	OFF	ON	OFF
10	OFF	ON	OFF	ON	OFF	ON	OFF	ON

ON indicates saturation

OFF indicates cutoff

Q6 back to the starting position. The positive pulse on the collector of transistor Q6 is differentiated; the resulting positive trigger pulse switches transistor Q7 to cutoff and transistor Q8 to saturation. Therefore, for each ten input pulses applied to multivibrator Q1, Q2, transistors Q7 and Q8 produce one complete output cycle.

4-245. Resistors R36 and R41 and capacitor C22 serve as the collector load and also form an integrating network to integrate the square-wave output at the collector of transistor Q7. The resulting sawtooth output from multivibrator Q7, Q8 is coupled to the 7.1 mc mixer by capacitor C23. Resistor R41 provides a d-c conduction path to ground for transistor Q7.

4-246. DIVIDE-BY-TEN MULTIVIBRATORS, TEST DATA. Pertinent references and applicable test data for the divide-by-ten multivibrators are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 500 CPS Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-82.

c. 500 CPS Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-13.

d. Divide-by-Ten Multivibrators, Component and Test Point Location, Figure 5-101.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Frequency Meter, CAQI-524D.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

4-247. 7.1 MC MIXER, FUNCTIONAL CIRCUIT DESCRIPTION. The 7.1 mixer (figure 4-55) consists of two amplifiers (Q3 and Q5), a mixer (Q1), two emitter followers (Q2 and Q4), and a 7.1 mc crystal filter (FL1). These circuits, which form a part of 500 CPS Synthesizer Electronic Subassembly 2A2A6A4, mix the 11-kc or 11.5-kc output from divide-by-ten multivibrators 2A2A6A4A2 with the 7.089-mc output from 7.089 mc mixer 2A2A6A3A4 to produce a nominal 7.1-mc output with the level suitable for use in 17.847/27.847 mixer 2A2A6A2A3. These circuits are used in all of the modes of operation. The following paragraphs describe the operation of the 7.1 mc mixer in detail.

4-248. The 11-kc or 11.5-kc output from the divide-by-ten multivibrators is coupled to the base of amplifier Q5 by capacitor C20. The operating voltage for amplifier Q5 is developed by voltage divider R25, R26 and emitter resistors R23 and R24 from the positive 20 vdc supply line. Decoupling is provided by capacitor C19 and resistor R21 to prevent interaction with the other circuits connected to the positive 20 vdc supply line. Capacitor C18 is the emitter bypass capacitor of amplifier Q5. The amplified output signals from amplifier Q5 are developed across a tuned circuit consisting of capacitor C17 and the primary of transformer T2. Resistor R22 increases the bandwidth of transformer T2.

4-249. The sinusoidal output from amplifier Q5 is coupled to the base of emitter follower Q4 by capacitor C16. The operating voltage for emitter follower Q4 is developed by voltage divider R19, R20. Resistor R18 and capacitor C15 provide decoupling to prevent interaction with the other circuits connected to the positive 20 vdc supply line. Emitter follower Q4 provides a low impedance source for mixer Q1. The output from emitter follower Q4 is developed across resistor R17 and coupled to the emitter of mixer Q1 by capacitor C14.

4-250. The operating voltage for mixer Q1 is developed from the positive 20 vdc supply line by emitter resistor R4 and voltage divider R1, R2. Resistor R3 and capacitor C3 provide decoupling to prevent interaction with the other circuits connected to the positive 20 vdc supply line. Capacitator C4 is the emitter bypass capacitor. Due to the large difference in frequency between the two inputs, resistor R5 develops a small amount of degeneration to increase the stability of mixer Q1. The 7.089-mc output from 7.089 mc mixer 2A2A6A3A4 is coupled to the base of mixer Q1 by capacitor C2. Transistor Q1 mixes the 11-kc or 11.5-kc signal with the 7.089-mc signal, providing one of two outputs. If the 11 kc is used, the mixing products are 11 kc, 7.089 mc, 7.078 mc, and 7.1 mc. If the 11.5 kc is used, the mixing products are 11.5 kc, 7.089 mc, 7.0775 mc, and 7.1005 mc. One of these two groups of mixing products is developed across resistor R6. The signals developed across resistor R6 are applied to filter FL1. Filter FL1 is very selective, allowing only the 7.1 mc, or the 7.1005 mc to pass. Capacitor C5 and resistor R6, and capacitor C6 and resistor R7 form the input and output terminations, respectively, for crystal filter FL1. The output from filter FL1 is coupled to the base of emitter follower Q2 by capacitor C7.

4-251. The operating voltage for emitter follower Q2 is developed from the positive 20 vdc supply line by voltage divider R8, R9 and emitter resistor R11. Resistor R10 and capacitor C8 provide decoupling to prevent interaction with the other circuits connected to the positive 20 vdc supply line. Emitter follower Q2 isolates filter FL1 to prevent it from being adversely loaded by amplifier Q3. The output from emitter follower Q2 is developed across resistor R11 and is coupled to the base of amplifier Q3 by capacitor C10.

4-252. The operating voltage for amplifier Q3 is developed by voltage divider R14, R15 and emitter resistor R13. Resistor R12 and capacitor C9 provide decoupling to prevent inter interaction with the other circuits connected to the positive 20 vdc supply line. Capacitor C12 is the emitter bypass capacitor. The amount of gain provided by amplifier Q3 is controlled by adjusting the amount of degeneration developed by potentiometer R16. The amplified out-

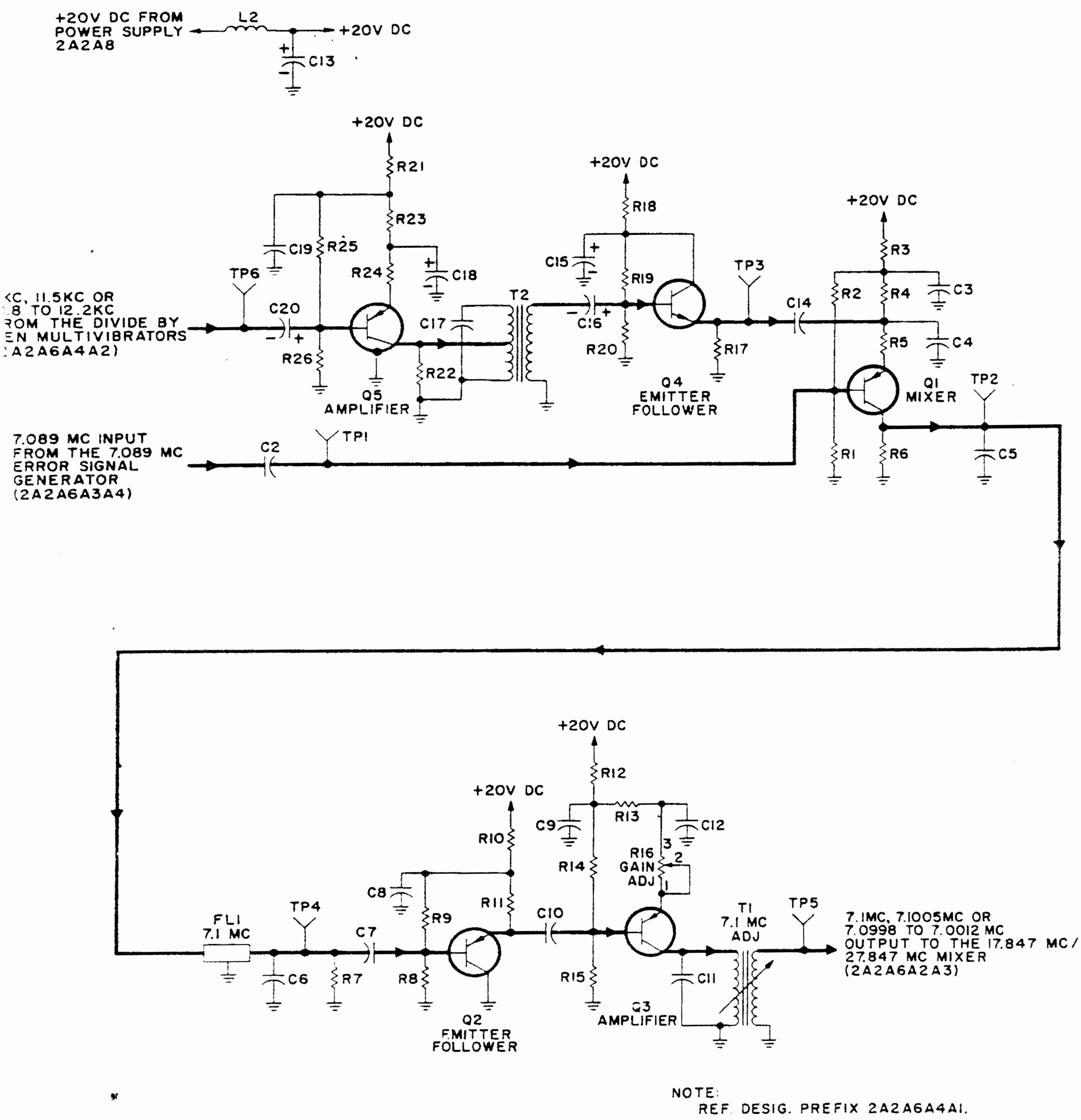


Figure 4-55. 7.1 MC Mixer, Simplified Schematic Diagram

put from amplifier Q3 is developed across the tuned circuit consisting of capacitor C11 and the primary of transformer T1 and is applied to 17.847/27.847 mixer 2A2A6A2A3.

4-253. 7.1 MC MIXER, TEST DATA. Pertinent references and applicable test data for the 7.1 mc mixer are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. 500 CPS Synthesizer Electronic Subassembly, Servicing Block Diagram, Figure 4-82.

c. 500 CPS Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-13.

d. 7.1 MC Mixer, Components and Test Panel Location, Figure 5-99.

e. Required Test Equipment:

(1) RF Signal Generator, CAQI-606A.

(2) Electronic Multimeter, CCVO-91CA.

(3) Frequency Meter, CAQI-524D.

(4) Multimeter, AN/PSM-4.

(5) Translator/Synthesizer Test Set, TS-2133/WRC-1.

f. Refer to paragraph 3-30 in Technical Manual for Repair of AN/WRC-1 and R-1051/URR 2N Modules, NAVSHIPS 95700 for 7.1 mc mixer adjustment procedures.

4-254. POWER SUPPLY, FUNCTIONAL CIRCUIT DESCRIPTION. The power supply (figure 4-56) consists of the +110 vdc supply, the +28 vdc supply, and the regulated +20 vdc supply. These circuits, which form a part of the Transmitter Main Frame 2A2, supply operating power to all the circuits in the T-827/URT. The following paragraphs describe the operation of the power supply in detail.

4-255. All power is derived from the nominal 115 vac line, which is applied through switches 2A2S7, 2A2S8, 2A2S2 and fuses 2A2F1, 2A2F2 to the primary of power transformer 2A2T1. Indicator lamps 2A2DS1 and 2A2DS2 will light if respective fuses, 2A2F1 and 2A2F2, open. The primary of transformer 2A2T1 is tapped so that in locations where line voltages differ slightly from the normal 115 vac on a reasonably permanent basis, the difference can be compensated by reconnecting to a new tap. The 6.3 vac from terminals 13 and 14 on the secondary of transformer 2A2T1 powers the filaments of rf amplifiers V1 and V2 in RF Amplifier Electronic Assembly 2A2A4. The output from terminals 7 and 8 of 2A2T1 is applied to a bridge rectifier consisting of diodes CR1 through CR4. The rectifier output is applied to a choke input filter consisting of choke 2A2L1 and capacitor 2A2C1. The output from the choke input filter (+110 vdc) is used as the plate and screen voltage supply in the RF Amplifier Electronic Assembly 2A2A4. Resistor 2A2R1 is a bleeder load for the +110 vdc. The output from terminals 9 and 10 of transformer 2A2T1 is applied to a bridge rectifier consisting of diodes CR5 through CR8. The rectifier output is applied to a choke input filter consisting of choke 2A2L2 and capacitors C1 and C2. The output from the choke input filter (+28 vdc) is used in the RF Amplifier Frequency Standard, LSB and USB Audio Amplifiers, and Translator/Synthesizer Electronic Assemblies. The regulated +20-vdc supply is derived from the +28-volt source. Resistor 2A2R2 is the bleeder load for the +28 vdc.

4-256. The regulated +20 vdc supply (figure 4-56) consists of series regulator 2A2Q1, dc amplifiers Q1 and Q2, comparators Q3 and Q4, 12 vdc Zener diode CR12 and 4.7 vdc Zener diode CR13. This circuit provides a constant +20 vdc regardless of the load. The input voltage of +28 vdc is applied to the collector of series regulator 2A2Q1 through contacts 7 and 6 on front of section C of switch 2A2S2 (set to any position other than OFF or STANDBY) and contacts 8 and 6 of relay 2A2K1. If the MCS controls are set to the 00 or 01 position, a ground is applied to relay 2A2K1. The relay is energized and thereby inhibits the output of the regulated 20 vdc supply unless the operating frequency is 2.0 to 30.0 mc. The collector-to-emitter resistance is inversely proportional to the amount of base-to-emitter current. The +20 vdc output voltage is selected by adjusting Output Voltage Control R10, which controls the bias voltage on comparator Q4. The bias voltage determines the amount of emitter current flow, thereby determining the voltage across the emitter resistor R8. Since the bias voltage on the base of comparator Q3 is held constant by Zener diode CR13, the collector current flow will be determined by the emitter voltage. The emitter of comparator Q3 is connected to the emitter of comparator Q4; therefore, the collector current of comparator Q3 will be controlled by the bias voltage on comparator Q4. The collector current flow of dc amplifier Q2 is controlled by the collector voltage on comparator Q3 since the base voltage is held constant by Zener diode CR12. The collector current of dc amplifier Q1 is controlled by the collector current of dc amplifier Q2. The collector current through resistor R2 determines the bias voltage on the base of series regulator A2Q1 which determines the emitter-to-collector resistance.

4-257. To understand fully the operation of the regulated +20 vdc supply, assume that some of the load on the +20 vdc has been removed. This condition causes the +20 vdc to rise. This rise increases the base-bias voltage of comparator Q4, thereby increasing the voltage across resistor R8. This increase results in a decrease in the base-to-emitter voltage of comparator Q3, thereby causing an increase in collector voltage. Since the emitter of dc amplifier Q3 is connected to the collector of comparator Q3 and the base voltage is held constant by Zener diode CR12, the increase in collector voltage in comparator Q3 causes the collector current to decrease in dc amplifier Q2. Since the collector of dc amplifier Q2 is connected to the base of dc amplifier Q1, the decrease in collector current in dc amplifier Q2 causes a decrease in collector current in dc amplifier Q1. Since the collector of dc amplifier Q1 is connected to the base of series regulator 2A2Q1 through resistor R2, a decrease in collector current in dc amplifier Q1 causes the collector-to-emitter resistance to increase, thereby causing the voltage to fall back to +20 vdc. Resistor R2 acts as a parasitic suppressor. Diode CR11 provides circuit protection in the event the +20 vdc line becomes grounded. Normally, diode CR11 is back-biased due to the +20 vdc on its anode and +12 vdc on its cathode. If the +20 vdc line becomes grounded, the diode will become forward-biased, dropping the base of dc amplifier Q2 to ground potential and preventing damaging current flow in dc amplifiers Q1 and Q2.

4-258. POWER SUPPLY, TEST DATA. Pertinent references and applicable test data for the power supply are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. Required Test Equipment:

(1) Multimeter, AN/PSM-4.

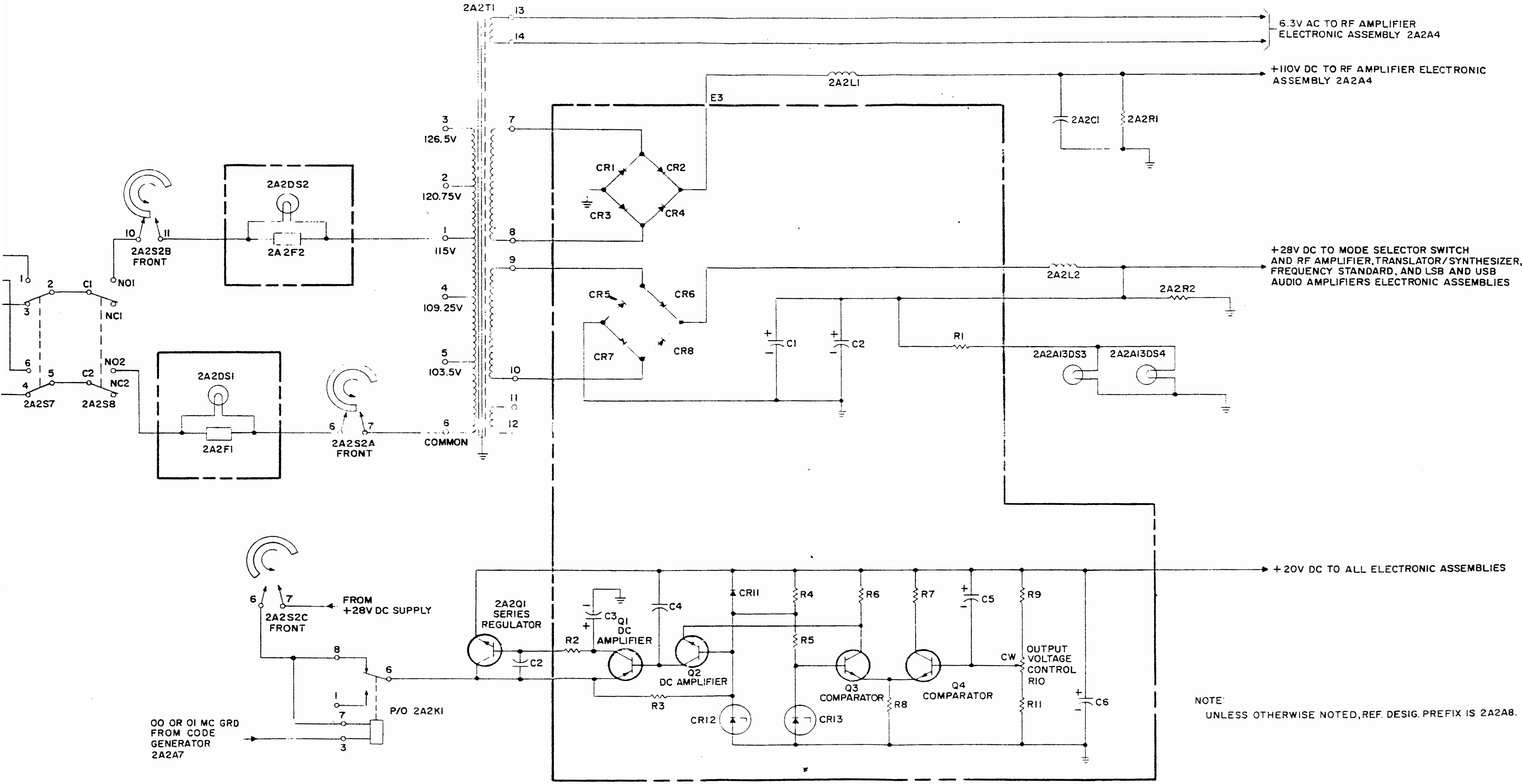
(2) Oscilloscope, AN/USM-105A.

c. Transmitter Power Supply Electronic Assembly, Component and Test Point Location, Figure 5-29.

d. 20-Volt Regulator Circuit adjustment, paragraph 5-6.

4-259. TUNING, FUNCTIONAL CIRCUIT DESCRIPTION. The tuning circuit (figure 4-57) consists of code generator 2A2A7; switch S1, motor B1, and relay K1 in RF Amplifier Electronic Assembly 2A2A4; and switch S1, motor B1, and relay K1 in 1 MC Synthesizer Electronic Subassembly 2A2A6A1. Code generator 2A2A7 consists of switches S3 and S4, which comprise three parallel open-seeking tuning circuits, each employing a five wire coding scheme. Two of these tuning circuits generate a tuning code for positioning the turret assembly in RF Amplifier Electronic Assembly 2A2A4 and the crystal switch in 1 MC Synthesizer Electronic Subassembly 2A2A6A1. The third tuning circuit generates a tuning code for positioning the turret assembly in the AM-3007/URT. This circuit is described in paragraph 4-354 and is illustrated in figure 4-69. The following paragraphs describe the tuning circuits used for tuning the T-827/URT in detail.

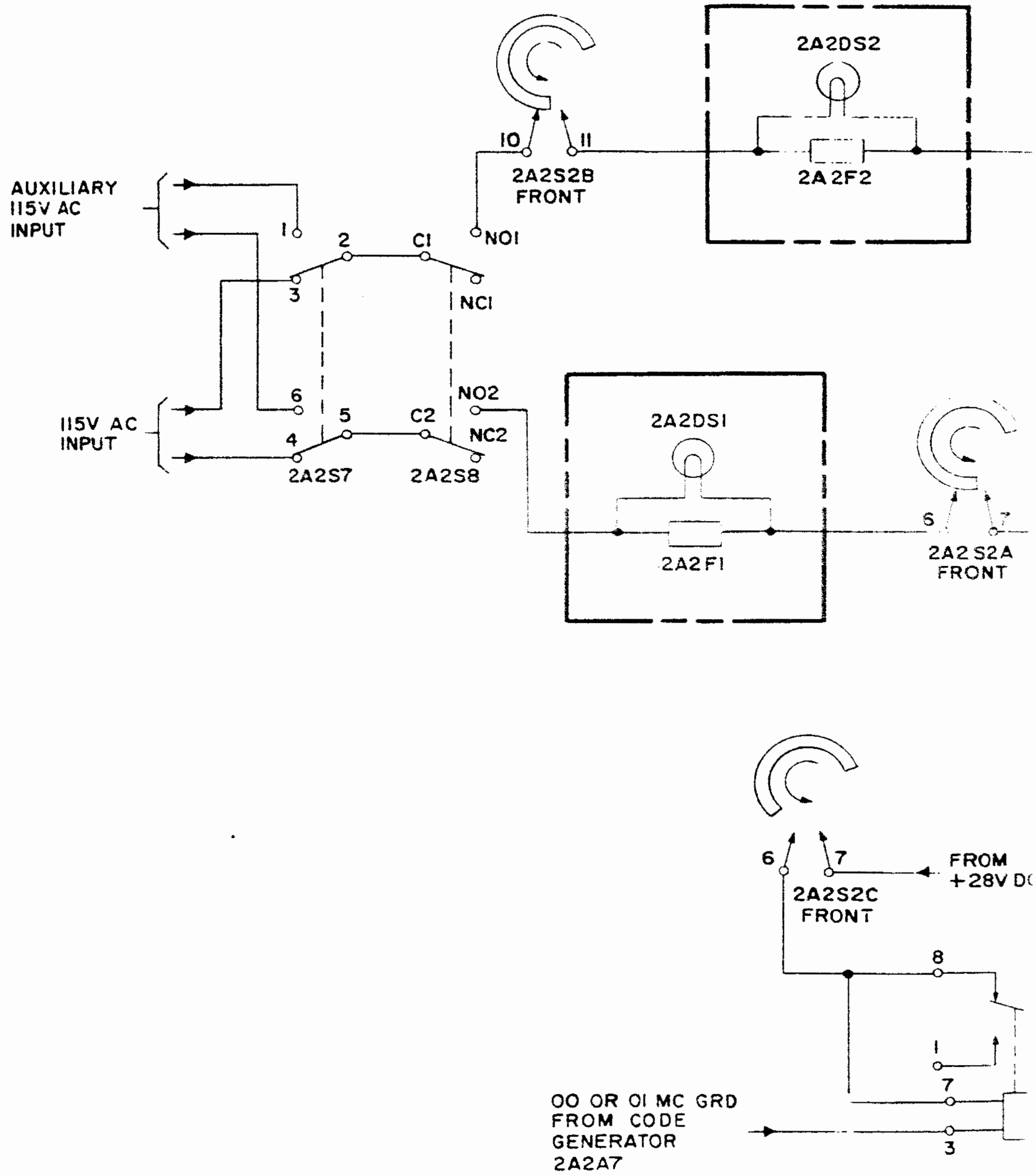
4-260. Switches S3 and S4 in 2A2A7 are controlled by the 10 mcs (MCS) and 1 mcs (MCS) controls on the front panel. These two switches are analagously represented (figure 4-57) by sections A, B, C, D, and E, of which sections A and C form two 28-position masters and sections B and D form two 28-position images. For the actual schematic diagram representation of these switches, see figure 5-16. Section A establishes the tuning code for turret switch S1 in RF Amplifier Electronic Assembly 2A2A4 and section C establishes the tuning code for crystal switch S1 in 1 MC Synthesizer Electronic Subassembly 2A2A6A1. The tuning code generated by section A is one of 28 series of opens and grounds, each series representative of one of the 28 tuning positions of turret switch S1 (refer to table 4-2). The tuning code generated by section C, although also a 28 position switch, is one of 17 series of opens and grounds, each series representative of one of the seventeen positions of crystal switch S1.



NOTE:
UNLESS OTHERWISE NOTED, REF. DESIG. PREFIX IS 2A2A8.

Figure 4-56. Transmitter Power Supply, Simplified Schematic Diagram

201/202


2A2DS2
10
11
2A2S2B
FRONT
2A 2F2
AUXILIARY
115V AC
INPUT
1
2
C1
NO1
3
NC1
6
NO2
5
C2
115V AC
INPUT
NC2
4
2A2S7
2A2S8
2A2DS1
2A2F1
6
7
2A2 S2A
FRONT
6
7
FROM
+28V DC
2A2S2C
FRONT
8
1
7
00 OR 01 MC GRD
FROM CODE
GENERATOR
2A2A7
3

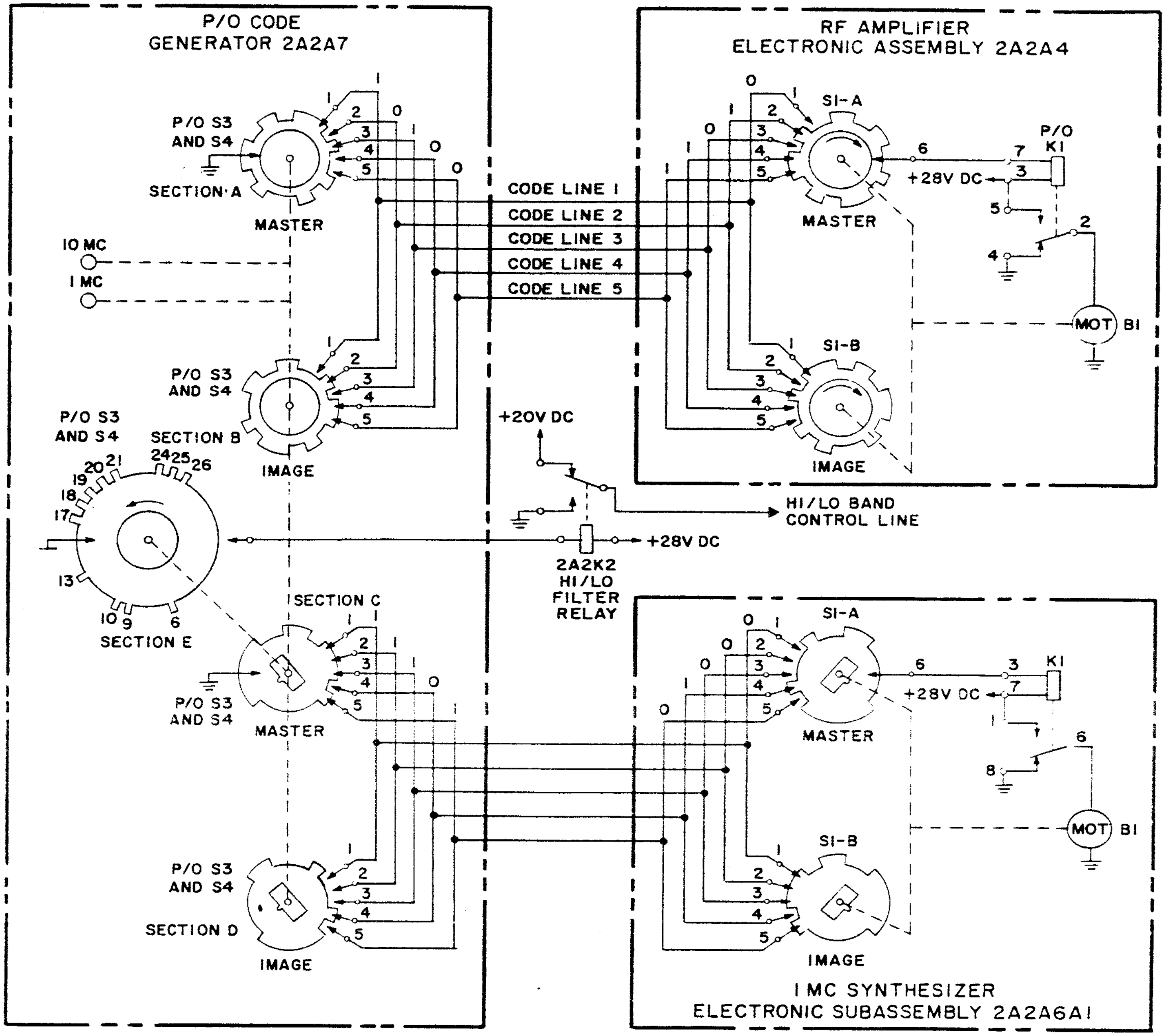


Figure 4-57. Radio Transmitter T-827/URT, Tuning, Simplified Schematic Diagram

(Refer to table 4-2.) Section A (master) applies the coded information to turret switch S1-A (master). A ground path is thus established through the common contact of S1-A to pin 7 of turret motor relay K1, causing it to energize, since positive 28 vdc is applied to pin 3. When turret motor relay K1 energizes, turret motor B1 is energized by the application of a positive 28 vdc through contacts 5 and 2 of turret motor relay K1. When energized, motor B1 rotates, rotating turret switch S1 until the complement of the code on section A (master) is reflected by turret motor switch S1-A (master). When the codes on the two masters are complementary, the ground path to turret motor relay K1 is broken, causing it to deenergize. Similarly, section C generates a code to crystal switch S1 to energize its respective motor to rotate crystal switch S1 to the correct position established by the position of the 1 and 10 mc (MCS) controls on the front panel.

4-261. The image switches in code generator 2A2A7, sections B and D, turret switch S1-B,

TABLE 4-2. TUNING CODE CHART

MCS and 100 KCS CONTROLS SETTING	2A2A4 CODE LINES					2A2A6A1 CODE LINES					AM-3007/URT					
											PASS BAND	CODE LINES				
	1	2	3	4	5	1	2	3	4	5		1	2	3	4	5
2	1	0	1	0	0	1	1	1	0	1	2.0 - 2.499	0	0	0	0	1
2.5											2.5 - 2.999	0	0	0	1	1
3	0	1	0	0	0	1	0	1	1	1	3.0 - 3.499	0	0	1	1	1
3.5											3.5 - 3.999	0	1	1	1	1
4	1	0	0	0	1	1	1	0	1	1	4.0 - 4.999	1	1	1	1	0
5	0	0	0	1	1	0	1	1	0	1	5.0 - 5.999	1	1	1	0	1
6	0	0	1	1	0	0	1	0	0	0	6.0 - 6.999	1	1	0	1	1
7	0	1	1	0	1	1	0	0	1	1	7.0 - 7.999	1	0	1	1	1
8	1	1	0	1	1	1	1	0	0	1	8.0 - 9.999	0	1	1	1	0
9	1	0	1	1	0	1	0	1	0	0						
10	0	1	1	0	0	1	1	0	1	0	10.0 - 11.999	1	1	1	0	0
11	1	1	0	0	0	0	0	1	1	1						
12	1	0	0	0	0	0	0	0	1	1	12.0 - 13.999	1	1	0	0	1
13	0	0	0	0	1	1	0	1	1	1						
14	0	0	0	1	0	0	1	1	1	0	14.0 - 15.999	1	0	0	1	0
15	0	0	1	0	1	0	0	1	1	0						
16	0	1	0	1	1	1	1	1	1	0	16.0 - 17.999	0	0	1	0	0
17	1	0	1	1	1	1	0	0	1	1						
18	0	1	1	1	1	1	1	0	0	1	18.0 - 19.999	0	1	0	0	1
19	1	1	1	1	0	1	1	1	0	0						
20	1	1	1	0	0	0	1	1	1	1	20.0 - 21.999	1	0	0	1	1
21	1	1	0	0	1	0	0	1	1	1						
22	1	0	0	1	0	0	0	0	0	1	22.0 - 23.999	0	0	1	1	0
23	0	0	1	0	0	1	1	1	1	0						
24	0	1	0	0	1	0	1	1	1	0	24.0 - 25.999	0	1	1	0	0
25	1	0	0	1	1	0	0	1	1	0						
26	0	0	1	1	1	1	1	1	1	0	26.0 - 27.999	1	1	0	0	0
27	0	1	1	1	0	0	0	0	1	1						
28	1	1	1	0	1	0	0	1	1	1	28.0 - 29.999	1	0	0	0	0
29	1	1	0	1	0	0	1	1	1	1						

0 indicates open

1 indicates ground

.nd crystal switch S1-B always have the com-
plementary code of their respective masters. This insures that the ground (grounds) will be pplied to the masters whenever a new code is elected. This is accomplished by the cut of he wafer, which is the exact mirror image of ıe respective master. All contacts appearing s opens or grounds at the master, appear as rounds or opens, respectively, at the image.

-262. As shown in figure 4-57, sections A nd B are positioned to represent the code 10100 (x2.xxx mc). If the MCS controls on the front panel were set at x3.xxx mc, sections A and B would be rotated one position counter-clockwise, creating a new code of 01000. (Refer to table 4-2.) A ground path would be established to pin 7 of turret motor relay K1 through code line 2 and turret motor switch S1-A. This energizes turret motor relay K1, which in turn energizes turret motor B1, rotating turret motor switch S1 until the image code 10111 is reflected by turret motor switch S1-A. At this time, the ground path is broken, causing turret motor relay K1 to deenergize. Ground is then applied through contacts 2 and 4 of turret motor relay K1 to turret motor B1. This dynamically brakes turret motor B1. If the MCS controls on the front panel were set at 22.xxx mc rather than x2.xxx mc, the code generated by section A would have been 10000. As shown in figure 4-67, there is no ground path directly between the two masters. This time, the ground path would be through code line 1 to turret motor switch S1-B (image) code line 3 to section B (image) and code line 2 to turret motor switch S1-A (master). Therefore, the ground path to turret motor relay K1 is established using the images. In a similar manner, any code can be traced and the tuning of turret switch S1 will be accomplished for any code shown in table 4-2. Similarly, the codes shown in table 4-2 can be used to energize crystal switch motor K1 to tune crystal switch S1 to the correct position established by the MCS controls on the front panel.

4-263. Section E of code generator 2A2A7 generates the hi/lo band control line codes. The wiper of section E remains open until, it is placed in a mc position that has a tab. At this time, ground is applied to hi/lo filter relay 2A2K2, causing it to energize. When the relay is energized, ground is placed on the hi/lo band control line. When hi/lo filter relay 2A2K2 is deenergized, a positive 20 vdc is applied to the hi/lo band control line.

4-264. TUNING, TEST DATA. Pertinent references and applicable test data for the tuning circuits are as follows:

a. Radio Transmitter T-827/URT, Main Frame, Schematic Diagram, Figure 5-5.

b. RF Amplifier Electronic Assembly, Schematic Diagram, Figure 5-8.

c. 1 MC Synthesizer Electronic Subassembly, Schematic Diagram, Figure 5-10.

d. Transmitter Code Generator Electronic Assembly, Schematic Diagram, Figure 5-16.

e. RF Amplifier Electronic Assembly, Front and Left Side View, Component Location, Figure 5-41.

f. RF Amplifier Electronic Assembly, Rear and Right Side View, Component Location, Figure 5-42.

g. RF Amplifier Electronic Assembly, Turret Removed, Front and Left Side View, Component and Test Point Location, Figure 5-43.

h. RF Amplifier Electronic Assembly, Turret Removed, Rear and Right Side View, Component and Test Point Location, Figure 5-44.

i. 1 MC Synthesizer Electronic Subassembly, Front View, Component Location, Figure 5-75.

j. 1 MC Synthesizer Electronic Subassembly, Rear View, Component Location, Figure 5-76.

k. Code Generator Electronic Assembly, Component Location, Figure 5-141.

l. Required Test Equipment: Multimeter, AN/PSM-4.

4-265. CONTROL SWITCHING, FUNCTIONAL DESCRIPTION. The control switching circuits (see figure 5-5) consist of switches S1, S2, S7, S8, and S9 and relays K1, K3, K4, and K5. These circuits, which form a part of Transmitter Main Frame 2A2, energize and key the circuits required for each mode of operation. The following paragraphs describe the control switching circuits in detail. All components described in the following paragraphs have the reference designation prefix 2A2.

4-266. Primary power (115 vac) for the T-827/URT is received via the J-1265/U, the AM-3007/URT, and cable W7 to pins R and S of connector J4 on the rear of the T-827/URT. In the NORM position of AUX/NORM switch (S7), the 115 vac is routed to interlock switch S8. If desired, primary power may be routed directly to the T-827/URT by setting the AUX/NORM switch (S7) at the AUX position and connecting the primary power to pins A and C of connector J3 on the rear of the T-827/URT, thus bypassing the J-1265/U and the AM-3007/URT. From interlock switch S8, one side of the 115-vac line (J4-S) is passed through fuse F1 and from there goes to contact 6 on the front part of section A of Mode Selector switch (S2), which is an open circuit in the OFF position. The other side of the 115-vac line (J4-R) is routed from interlock switch S8 to contact 10 on the front part of section B of Mode Selector switch (S2), which is also an open circuit in the OFF position.

4-267. In the STD-BY position of Mode Selector switch (S2), the one side of the 115 vac line J4-3 is routed to terminal 6 of power transformer T1. The other side of the 115-vac line, which is switched through section B of switch (S2), is routed from contact 11 through fuse F2 and to terminal 1 of transformer T1, thus completing the power input circuit of the T-827/URT and energizing transformer T1.

4-268. In the following positions of Mode Selector switch (S2), the T-827/URT is energized and ready for operation. In any "ON" position of switch S2, such as USB or CW, one side of the 115 vac line is routed through contacts 10 and 12 of the front part of section B of switch S2 to contact 10 of the rear part of section B of LOCAL/REMOTE switch (S1), and also to pin n of connector J4 on the rear of the T-827/URT. At pin n of connector J4, this lead ends and is not used in the AN/WRC-1. In the REMOTE position of LOCAL/REMOTE switch (S1), the 115 vac is routed through contact 8 to pin U of connector J4 on the rear of the T-827/URT, and from there is routed through the J-1265/U to the Remote Control Box.

4-269. In the STD-BY position of Mode Selector switch (S2), the 6.3-vac, the 110-vdc, and the 28-vdc power supplies are energized. (See paragraph 4-256). The 28 vdc is routed to Frequency Standard Electronic Assembly A5, where the 5 mc oscillator and its associated oven and temperature control circuits are energized. The +28 vdc is routed to grd pulse relay K6, which is not used when the T-827/URT is used as part of the AN/WRC-1, and also to contacts 1, 4, 7, and 9 on the rear part of section C of switch S2. In the OFF and STD-BY positions of Mode Selector switch (S2), the +28 vdc is not switched; however, in the "ON" position of switch S2, the 28 vdc is routed to the remaining 28-vdc relays and also to contact 8 of tune relay K1. When tune relay K1 is de-energized, the 28 vdc is fed via contacts 8 and 6 to the 20 vdc regulator (refer to paragraph 4-256), which produces the 20-vdc B+ supply used in most of the electronic assemblies. Tune relay K1 is energized by placing a ground on pin 3. The purpose of tune relay K1 is two-fold. If either the motor in RF Amplifier Electronic Assembly A4 or the motor in 1 MC Synthesizer Electronic Subassembly A6A1 is energized, indicating a frequency change, a ground is applied to pin 3 of tune relay K1 from the energized motor relay. This energizes tune relay K1, removing the 28 vdc from the regulator circuit and consequently removing the +20 vdc from the electronic assemblies. The ground key line is also routed through normally closed contacts 4 and 2 of tune relay K1. These contacts are broken during the tuning time, so that transmit/receive relay K3 cannot be energized while the motors are tuning. If the MCS controls are placed in the 00 or 01 mc position, the code generator applies a ground to pin 3, energizing tune relay K1, making the T-827/URT inoperative.

4-270. From the power supply, the 6.3-vac line is routed directly to RF Amplifier Electronic Assembly A4, where it is used as heater voltage for rf amplifier tubes V1 and V2. The +110-vdc power supply is used as a plate supply for rf amplifier tubes V1 and V2 in RF Amplifier Electronic Assembly A4, and is routed through contacts 14 and 7 of transmit/receive relay K3. Transmit/receive relay K3 is energized, when the T-827/URT is keyed from any of the various key lines, by grounding pin 9. The power for transmit/receive relay K3 is obtained from pin J of connector J4 (the CU-937/UR interlocked 28-vdc line). If the CU-937/UR is disconnected, it is impossible to key the AN/WRC-1 because the power source for transmit/receive relay K3 is broken. This feature prevents accidental keying of the AN/WRC-1 without a tuned load terminating the AM-3007/URT. This circuit may be disabled, and 28 volts provided at pin J of connector J4, by setting the Antenna Interlock/Override switch, in the AM-3007/URT, at the Override position when it is desired to operate the AN/WRC-1 into a 50-ohm load or directly into a 50-ohm antenna.

4-271. In addition to switching the +110 vdc to RF Amplifier Electronic Assembly A4, transmit/receive relay K3 also switches 20 vdc to Translator/Synthesizer Electronic Assembly A6 in the key down position. This 20 vdc is routed via contacts 4 and 12 to pin 16 of connector J12, placing the various circuits in Translator/Synthesizer Electronic Assembly A6 in the transmit mode. This transmit control 20 vdc is also routed from contact 12 of transmit/receive relay K3 to RF Amplifier Electronic Assembly A4 and Transmitter Mode Selector Electronic Assembly A1 to energize diode gates and other circuits used only when the AN/WRC-1 is keyed.

4-272. SWITCHING FUNCTIONS FOR LOCAL/REMOTE SWITCH S1. Paragraphs 4-273 and 4-274 contain the information on the switching functions for LOCAL/REMOTE switch S1. All components in the following tables have the reference designation prefix 2A2. Switch parts are abbreviated in the following tables, for example: S1-A-F means the front part of section A of switch S1 and S1-B-R means the rear part of section B of switch S1.

4-273. Local Position of LOCAL/REMOTE Switch S1. Table 4-3 contains information concerning voltage routing through LOCAL/REMOTE switch S1 in the LOCAL position.

4-274. REMOTE Position of LOCAL/REMOTE Switch S1. Table 4-4 contains information concerning voltage routing through LOCAL/REMOTE switch S1 in the REMOTE position.

4-275. SWITCHING FUNCTIONS FOR MODE SELECTOR SWITCH S2. Paragraph 4-276 through 4-282 contain switching functions information for Mode Selector switch S2. All components in the following tables have the reference designation prefix 2A2. Switch parts are abbreviated in the following tables, for example: S2-A-R means the rear part of section A of switch S2 and S2-C-F means the front part of section C of switch S2.

TABLE 4-3. LOCAL/REMOTE SWITCH S1, LOCAL POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Local TTY Input (+)	J7-B	S1-A-F	2 and 5	J20-2
Local TTY Input (-)	J7-C	S1-A-F	10 and 1	J20-3
+12 vdc Keyline	J1-E	S1-B-F	2 and 5	K4-7
Mike Audio	J1-C	S1-B-F	1 and 10	S2-B-R-10 and S2-A-R-8
+28 vdc	S2-C-F-3 and S2-C-F-11	S1-B-F	9 and 6	E11 (R3)
Local FSK Key	J7-A	S1-B-R	3 and 6	S2-B-R-2
CW Key	J2-3	S1-B-R	11 and 2	S2-C-R-9

TABLE 4-4. LOCAL/REMOTE SWITCH S1, REMOTE POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
TTY Input (+)	J4-BB	S1-A-F	3 and 5	J20-2
TTY Input (-)	J4-t	S1-A-F	11 and 1	J20-3
600 ohm LSB/ISB Input	J4-g	S1-A-F	7 and 9	J19-20
600 ohm LSB/ISB Input	J4-f	S1-A-R	12 and 2	J19-9
600 ohm USB/AM/ISB Input	J4-q	S1-A-R	4 and 6	S2-C-R-10

TABLE 4-4. LOCAL/REMOTE SWITCH S1, REMOTE POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
600 ohm USB/AM/ISB Input	J4-s	S1-A-R	8 and 10	S2-D-F-5 and 6
PTT +12 vdc Keyline	J4-k	S1-B-F	3 and 5	K4-7
CW/FSK Keyline	J4-c	S1-B-R	4 and 6	S2-B-R-2
			12 and 2	S2-C-R-9
Remóte 115 vac	J4-U	S1-B-R	8 and 10	S2-B-F-12

4-276. LSB Position of Mode Selector Switch S2. Table 4-5 contains information concerning voltage routing through Mode Selector switch S2 in the LSB mode of operation.

4-277. FSK Position of Mode Selector Switch S2. Table 4-6 contains information concerning voltage routing through Mode Selector Switch S2 in the FSK mode of operation.

TABLE 4-5. MODE SELECTOR SWITCH S2, LSB POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Xmit +20 vdc	K3-12	S2-A-R	3 and 2	J17-2, J16-2 & J19-1
			3 and 4	J17-7
LSB Mike Audio	S1-B-F-10	S2-A-R	8 and 9	J19-12
+28 vdc	+28 vdc supply	S2-C-F	9 and 11	S1-B-F-9 and E23
GRD Keyline	K1-2	S2-D-R	3 and 12	J4-K

TABLE 4-6. MODE SELECTOR SWITCH S2, FSK POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Xmit +20 vdc	K3-12	S2-A-F	12 and 10	J20-1
Smit +20 vdc	K3-12	S2-A-R	3 and 4	J17-7
			3 and 5	J17-8, J16-5 and J18-17

TABLE 4-6. MODE SELECTOR SWITCH S2, FSK POSITION (Cont)

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Local/Remote FSK Key	S1-B-R-6	S2-B-R	2 and 4	K4-4
GRD	ground	S2-C-R	2, 3 and 6	J4-G and J18-9
FSK Audio	J20-4	S2-D-F	2 and 4	J18-20

TABLE 4-7. MODE SELECTOR SWITCH S2, AM POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Xmit +20 vdc	K3-12	S2-A-F	1 and 11	J17-4
Xmit +20 vdc	K3-12	S2-A-R	3 and 4	J17-7
			3 and 5	J17-8, J16-5 and J18-17
USB/AM Mike Audio	S1-B-F-10	S2-B-R	10 and 11	J18-12
+28 vdc	+28 vdc supply	S2-C-F	1 and 11	S1-B-F-9 and E23
Remote Audio	S1-A-R-6	S2-C-R	10 and 8	J18-9
Remote Audio	S1-A-R-10	S2-D-F	5 and 3	J18-20
GRD Keyline	K1-2	S2-D-R	5 and 12	J4-K

4-278. AM Position of Mode Selector Switch S2. Table 4-7 contains information concerning voltage routing through Mode Selector switch S2 in the AM mode of operation.

4-279. CW Position of Mode Selector Switch S2. Table 4-8 contains information concerning voltage routing through Mode Selector switch S2 in the CW mode of operation.

TABLE 4-8. MODE SELECTOR SWITCH S2, CW POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Xmit +20 vdc	K3-12	S2-A-F	12 and 2	J17-10
CW GRD	S2-C-R-4	S2-B-R	6 and 4	K4-4
CW GRD	K5-6	S2-C-R	3, 4 and 8	S2-B-R-6 and J18-9

TABLE 4-8. MODE SELECTOR SWITCH S2, CW POSITION (Cont)

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Local/Remote CW Key	S1-B-R-2	S2-C-R	9 and 11	J17-5 and A8-11
Remote Audio	S1-A-R-10	S2-D-F	6 and 4	J18-20

4-280. USB Position of Mode Selector Switch S2. Table 4-9 contains information concerning voltage routing through MODE SELECTOR Switch S2 in the USB mode of operation.

4-281. ISB Position of Mode Selector Switch S2. Table 4-10 contains information concerning voltage routing through MODE SELECTOR switch S2 in the ISB mode of operation.

TABLE 4-9. MODE SELECTOR SWITCH S2, USB POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Xmit +20 vdc	K3-12	S2-A-R	3 and 4	J17-7
Xmit +20 vdc	K3-12	S2-A-R	6 and 5	J17-8, J16-5 and J18-17
USB/AM Mike Audio	S1-B-F-10	S2-B-R	10 and 11	J18-12
+28 vdc	+28 vdc supply	S2-C-F	1 and 3	S1-B-F-9 and E23
Remote Audio	S1-A-R-6	S2-C-R	10 and 12	J18-9
Remote Audio	S1-A-R-10	S2-D-F	5 and 7	J18-20
GRD Keyline	K1-2	S2-D-R	9 and 12	J4-K

TABLE 4-10. MODE SELECTOR SWITCH S2, ISB POSITION

FUNCTION	FROM	THROUGH		TO
		SWITCH	CONTACTS	
Xmit +20 vdc	K3-12	S2-A-R	3 and 2	J17-10
			3 and 4	J17-7
			3 and 5	J17-8, J16-5 and J18-17
ISB Mike Audio	S1-B-F-10	S2-B-R	10 and 12	S9-6
+28 vdc	+28 vdc supply	S2-C-F	4 and 3	S1-B-F-9 and E23
Remote Audio	S1-A-R-6	S2-C-R	10 and 6	J18-9
Remote Audio	S1-A-R-10	S2-D-F	6 and 8	J18-20
GRD Keyline	K1-2	S2-D-R	10 and 12	J4-K

4-282. ISB/FSK Position of Mode Selector Switch S2. Table 4-11 contains information concerning voltage routing through MODE SELECTOR Switch S2 in the ISB/FSK mode of operation.

4-283. RF AMPLIFIER AM-3007/URT, FUNCTIONAL DESCRIPTION.

4-284. RF Amplifier AM-3007/URT (figure 4-58) consists of an input bridge circuit, two amplifier stages, the turret, the turret control circuits, a peak power control (PPC) circuit, an average power control (APC) circuit, a directional coupler, an ac power supply, and a dc-to-dc converter. Several of these circuits are contained on plug-in assemblies. The main functions of the AM-3007/URT are to amplify the rf output from the transmitter to 100 watts peak envelope power (PEP-SSB), 25 watts (AM carrier), or 50 watts (CW or FSK) for application to the antenna through CU-937/UR and to direct the received rf signals from the antenna to the R-1051/URR.

4-285. MAIN SIGNAL FLOW. The rf output from the T-827/URT is applied to the rf input bridge. Here, the input rf is algebraically added to a feedback signal that is 180 degrees out of phase with the input. The feedback loop keeps unit intermodulation distortion at a minimum and keeps the overall gain and sensitivity of the AM-3007/URT relatively constant, regardless of changes in power input or frequency. Since the feedback level is approximately 12 db, the output of the rf input bridge is essentially the input rf minus the 12-db feedback. This signal is applied to driver amplifier 3A2V1. Driver amplifier 3A2V1 is a linear amplifier for all modes of operation. The amplified output of driver amplifier 3A2V1 is applied to the tuned interstage circuit, which is part of the turret assembly. The tuned output circuit for driver amplifier 3A2V1 is one of nineteen transformer assemblies that are automatically switched into the circuit according to the operating frequency by a tuning code generated in the T-827/URT. The transformer assembly connected into the circuit will be resonant in the band in which the operating frequency falls. The rf signal applied to the transformer assembly is coupled to the grid of final power amplifier 3A2V2. Final power amplifier 3A2V2 is also a linear amplifier in AM or SSB operation, but is a class C amplifier in CW or FSK operation. Conversion is accomplished by changing operating voltages when switching from one mode to another. The amplified output of final power amplifier 3A2V2 is applied to a tuned output circuit on the turret assembly. This tuned output circuit is, like that for driver 3A2V1, one of nineteen available filter assemblies that are automatically switched into the circuit according to the operating frequency. The rf signal is coupled through APC/PPC/Directional Coupler Electronic Assembly 3A2A2 to the antenna transfer relay. When the AN/WRC-1 is keyed, the antenna transfer relay is energized, and the rf output is connected to the antenna coupler. When the AN/WRC-1 is not keyed, the antenna transfer relay is de-energized, and any rf signal received is connected from the antenna coupler to the R-1051/URR. In the APC/PPC/Directional Coupler Electronic Assembly, the forward and reverse rf current flow is tapped and applied to RF OUTPUT meter (M2) to provide indication of the VSWR.

TABLE 4-11. MODE SELECTOR SWITCH S2, ISB/FSK POSITION

FUNCTION	FROM	THROUGH SWITCH	THROUGH CONTACTS	TO
Xmit +20 vdc	K3-12	S2-A-F	3 and 5	J20-1
LSB Mike Audio	S1-B-F-10	S2-A-R	8 and 9	J19-12
Xmit +20 vdc	K3-12	S2-A-R	3 and 2	J17-10
			3 and 4	J17-7
			3 and 5	17-8, J16-5 and J18-17
Local/Remote FSK Key	S1-B-R-6	S2-B-R	2 and 4	K4-4
+28 vdc	+28 vdc supply	S2-C-F	4 and 3	S1-B-F-9 and E23
GRD	ground	S2-C-R	2 and 12	J18-9
FSK Audio	J20-4	S2-D-F	9 and 7	J18-20
GRD Keyline	K1-2	S2-D-R	11 and 12	J4-K

4-286. APC AND PPC GENERATION. An average power control signal (APC) and a peak power control signal (PPC) are developed in the AM-3007/URT and applied to the T-827/URT to limit the average and peak power outputs of the T-827/URT at a safe level. Both of these control signals are dependent on the operation of final power amplifier 3A2V2. The control grid bias supply for final power amplifier 3A2V2 passes through the primary of a transformer in the PPC amplifier circuit. Whenever grid current is drawn, the positive peaks are coupled to the PPC amplifier circuit. This input is amplified, clipped, and filtered, and the resultant dc level, which is representative of the peak power output of the AM-3007/URT, limits the output of the peak power controlled if. amplifier in the Transmitter IF. Amplifier Electronic Assembly of the T-827/URT. The rf output of final power amplifier 3A2V2 is applied to the APC detector circuit, where the positive half is envelope-detected and applied to one of the two APC amplifier circuits. In AM or SSB operation, the detected output of the APC detector is applied to APC amplifier Q2; in CW or FSK operation, the detected signal is applied to APC amplifier Q1. The output of APC amplifier Q2 is applied, through a modulation wiper circuit which produces a small peak sawtooth output, to output amplifier Q3. The output of APC amplifier Q1 is applied directly to output amplifier Q3. The output of output amplifier Q3 is filtered, and the resultant dc level, which is representative of the average power output of the rf amplifier, limits the output of the average power controlled if. amplifier in the Transmitter IF. Amplifier Electronic Assembly of the T-827/URT.

4-287. FREQUENCY PROGRAMMING. When an operating frequency is selected at the T-827/URT, a five-wire, open-seeking code is generated and applied to the rf amplifier. When this code is applied, a ground will be applied to energize a series of relays. These relays will apply +28 vdc to the positive side of turret motor B1, which will begin to rotate the turret. When the turret is properly positioned, the code will be satisfied, and the grounds will be removed from the relays. The relays will be de-energized, and a ground will be applied to the positive side of turret motor B1. Grounding the motor provides dynamic braking to keep the turret from overshooting. At the same time, another code will be generated by the encoder portion of decode/encode switch S1 and applied to the antenna coupler (through the J-1265/U) to rough-tune the CU-937/UR to the new frequency. Two terminal boards in the J-1265/U provide for pre-programming the CU-937/UR.

4-288. POWER SUPPLIES. The nominal 115-vac primary power is applied to AC Power Supply Electronic Assembly 3A2A3. From here, it is routed back to the J-1265/U for use in other units. The ac power supply produces the +28 vdc output, which is used to power DC-to-DC Converter Electronic Assembly 3A2A5, the turret motor, and some of the relays in the rf amplifier. DC-to-DC Converter Electronic Assembly 3A2A5 is powered by positive 28 vdc from AC Power Supply Electronic Assembly 3A2A3, or from an external source. This +28 vdc is converted to square-wave ac, transformer coupled to various rectifiers, and rectified to produce the following dc voltages:

a. 940 vdc, 3A2V2 plate supply.

b. 375 vdc, 3A2V2 screen supply.

c. 28 vdc, 3A2V2 filament supply.

d. -30 vdc, 3A2V2 grid bias supply.

e. 190 vdc, 3A2V1 plate and screen supply.

f. 6.75 vdc, 3A2V1 filament supply.

g. -84 vdc, 3A2V1, grid bias supply.

h. 130 vdc, receiver plate supply.

i. 13.5 vdc, remote control supply.

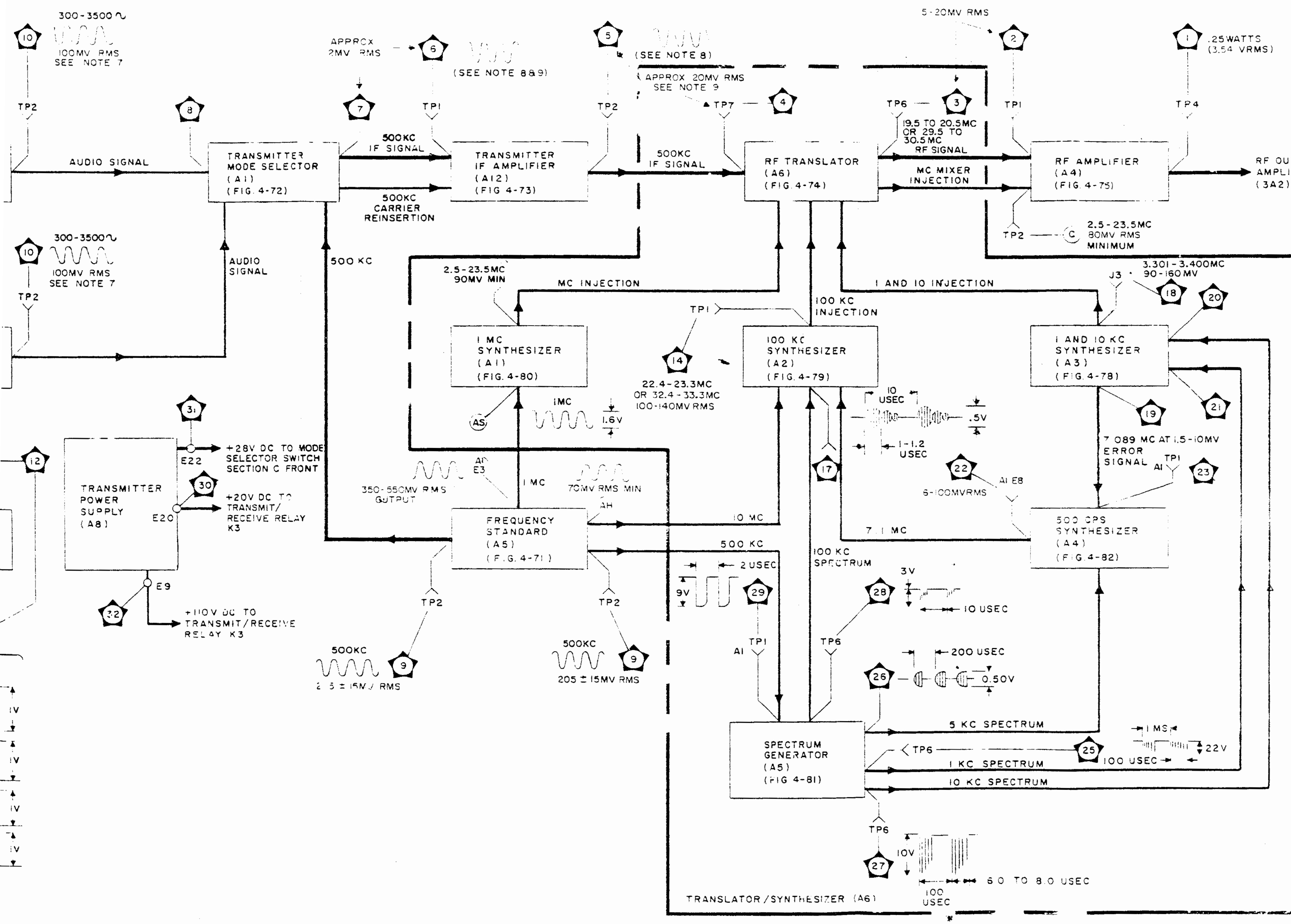
4-289. RF AMPLIFIER AM-3007/URT, TEST DATA.

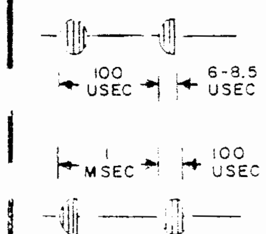
4-290. Pertinent references and applicable test data for the AM-3007/URT are as follows.

a. RF Amplifier AM-3007/URT, Main Frame and Case, Schematic Diagram, Figure 5-19.

b. RF Amplifier AM-3007/URT, Overall Servicing Block Diagram, Figure 4-83.

c. RF Amplifier AM-3007/URT, Top View, Case Removed, Component and Test-Point Location, Figure 5-118.

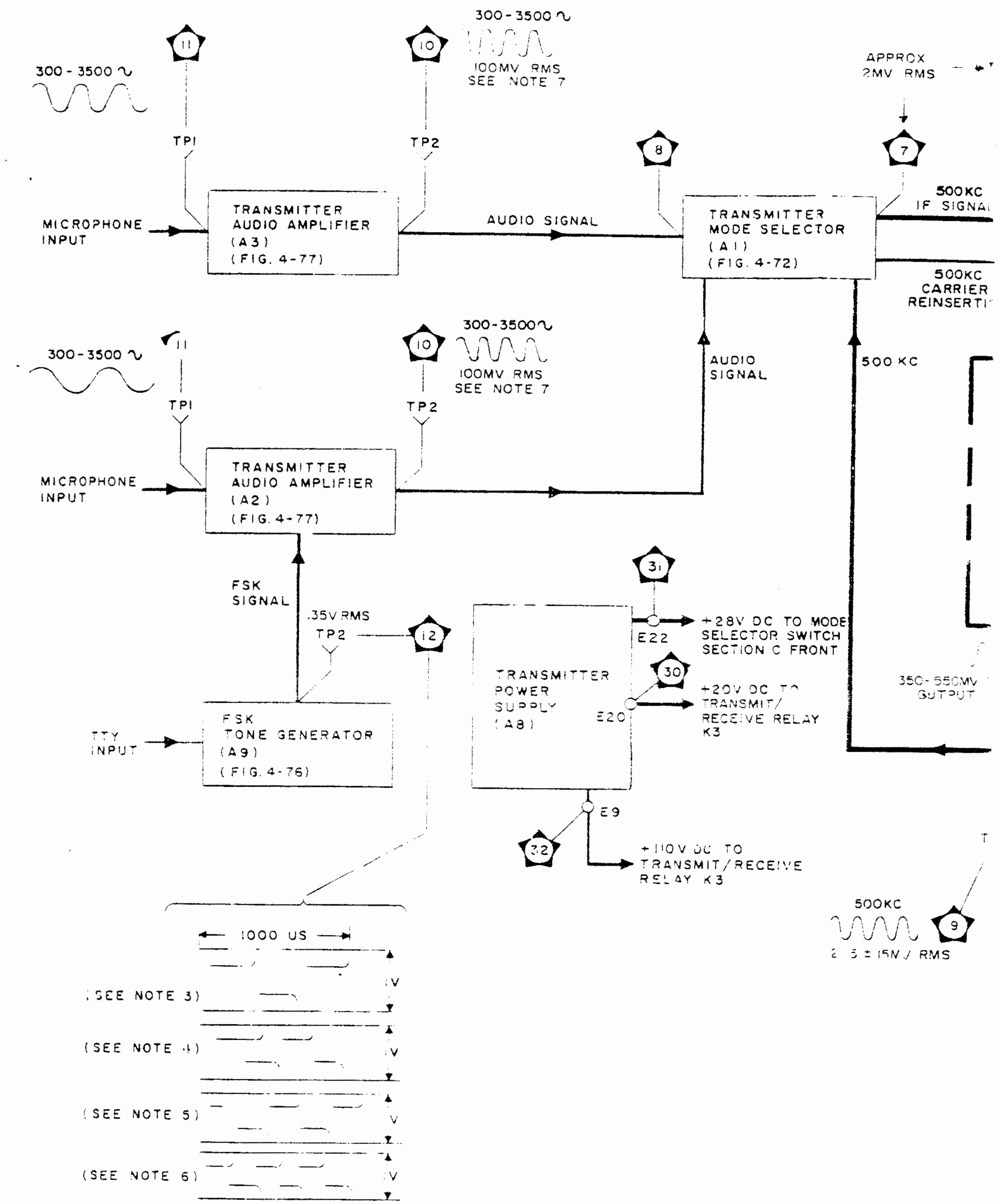


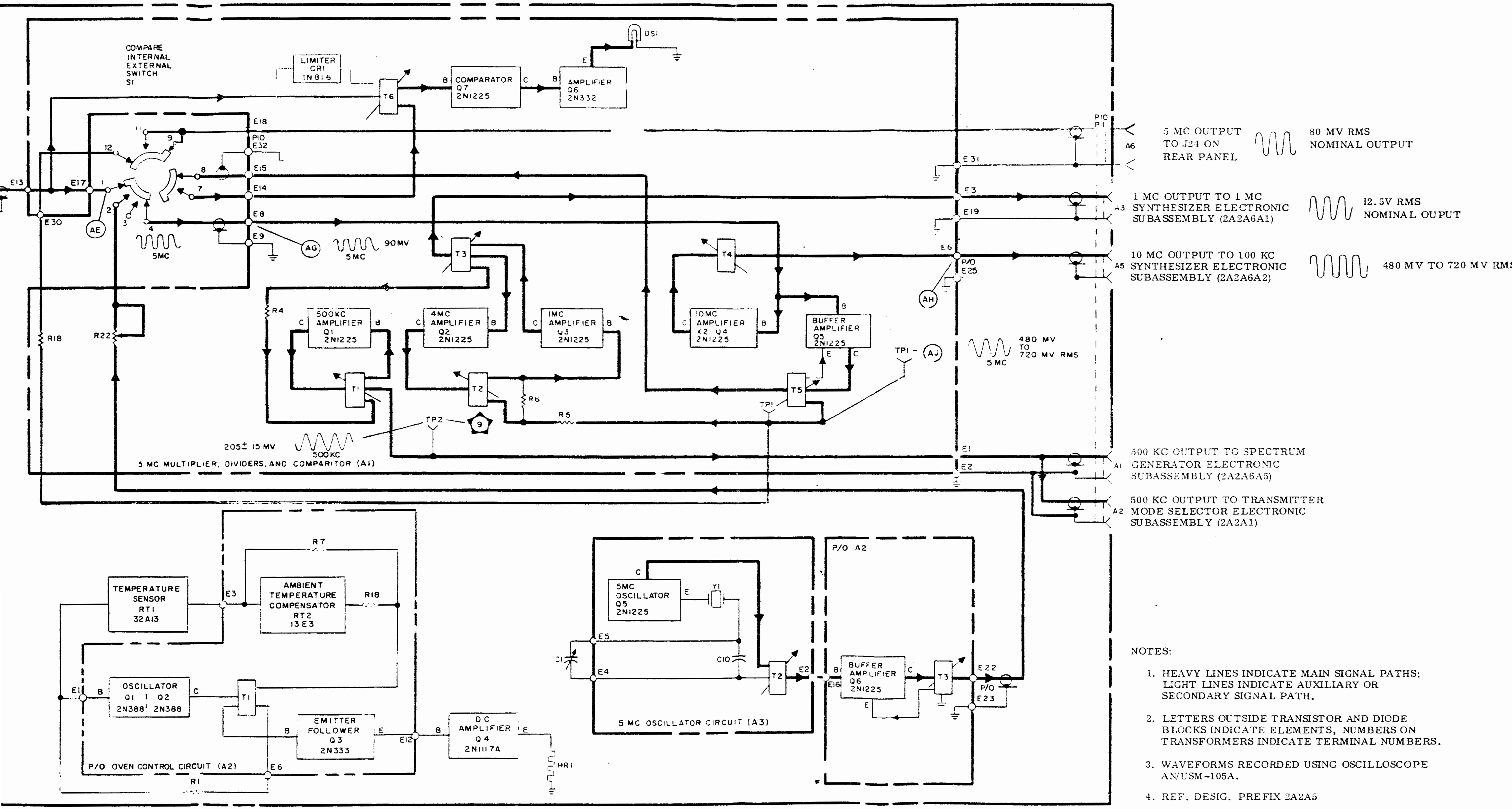


NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATH: LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. WAVEFORMS RECORDED ON OSCILLOSCOPE AN/USM-105A.
3. FREQ - 1575 CPS, FUNCTION - SPACE, CENTER FREQ - 2000 CPS.
4. FREQ - 2125 CPS, FUNCTION - SPACE,CENTER FREQ - 2550 CPS.
5. FREQ - 2425 CPS, FUNCTION - MARK, CENTER FREQ - 2000 CPS.
6. FREQ - 2975 CPS, FUNCTION - MARK, CENTER FREQ - 2550 CPS.
7. NOMINAL OUTPUT 100MV RMS - SINGLE TONE 150 MV INPUT AT PINS 20 AND 9 OF CONNECTOR P1, MEASURED WITH ELECTRONIC MULTIMETER ME-6( )/U.
8. AM MODE, CARRIER, WITH MODULATION AS PER NOTE 7.
9. GAIN SUBJECT TO CHANGE WITH SETTING OF GAIN ADJ. 2A2A12R15 (REFER TO PARA 5-27).
10. UNLESS OTHERWISE SPECIFIED, ALL RMS VOLTAGES MEASURES WITH ELECTRONIC MULTIMETER CCVO-91CA.

Figure 4-70. Radio Transmitter T-827/URT, Overall Servicing Block Diagram

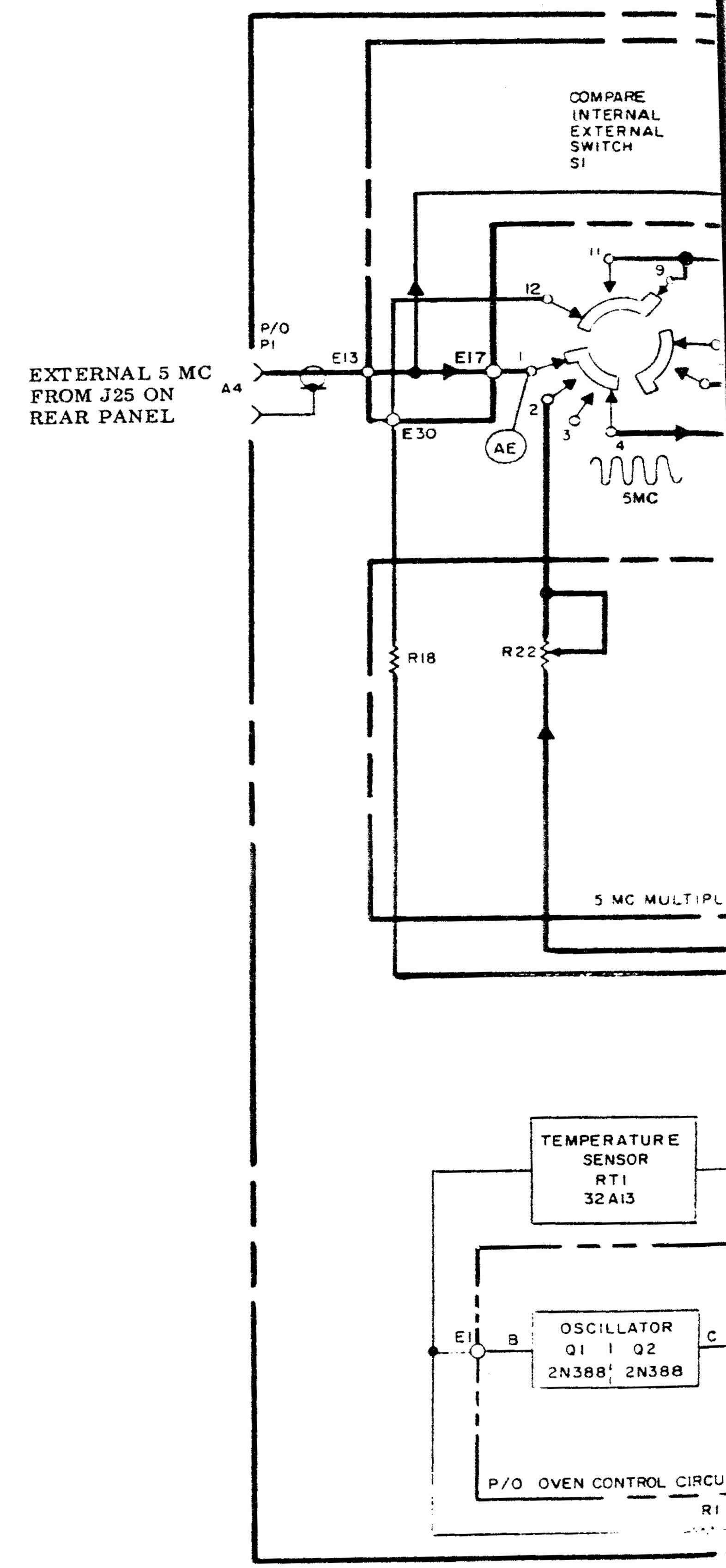

300 - 3500 ∿
TP1
TP2
300 - 3500 ∿
100MV RMS
SEE NOTE 7
APPROX
2MV RMS
MICROPHONE INPUT
TRANSMITTER AUDIO AMPLIFIER (A3) (FIG. 4-77)
AUDIO SIGNAL
TRANSMITTER MODE SELECTOR (A1) (FIG. 4-72)
500KC IF SIGNAL
500KC CARRIER REINSERTION
AUDIO SIGNAL
500 KC
MICROPHONE INPUT
TRANSMITTER AUDIO AMPLIFIER (A2) (FIG. 4-77)
FSK SIGNAL
.35V RMS
TTY INPUT
FSK TONE GENERATOR (A9) (FIG. 4-76)
TRANSMITTER POWER SUPPLY (A8)
E22
+28V DC TO MODE SELECTOR SWITCH SECTION C FRONT
E20
+20V DC TO TRANSMIT/RECEIVE RELAY K3
E9
+110V DC TO TRANSMIT/RECEIVE RELAY K3
350-550MV OUTPUT
500KC
1000 US
(SEE NOTE 3)
(SEE NOTE 4)
(SEE NOTE 5)
(SEE NOTE 6)



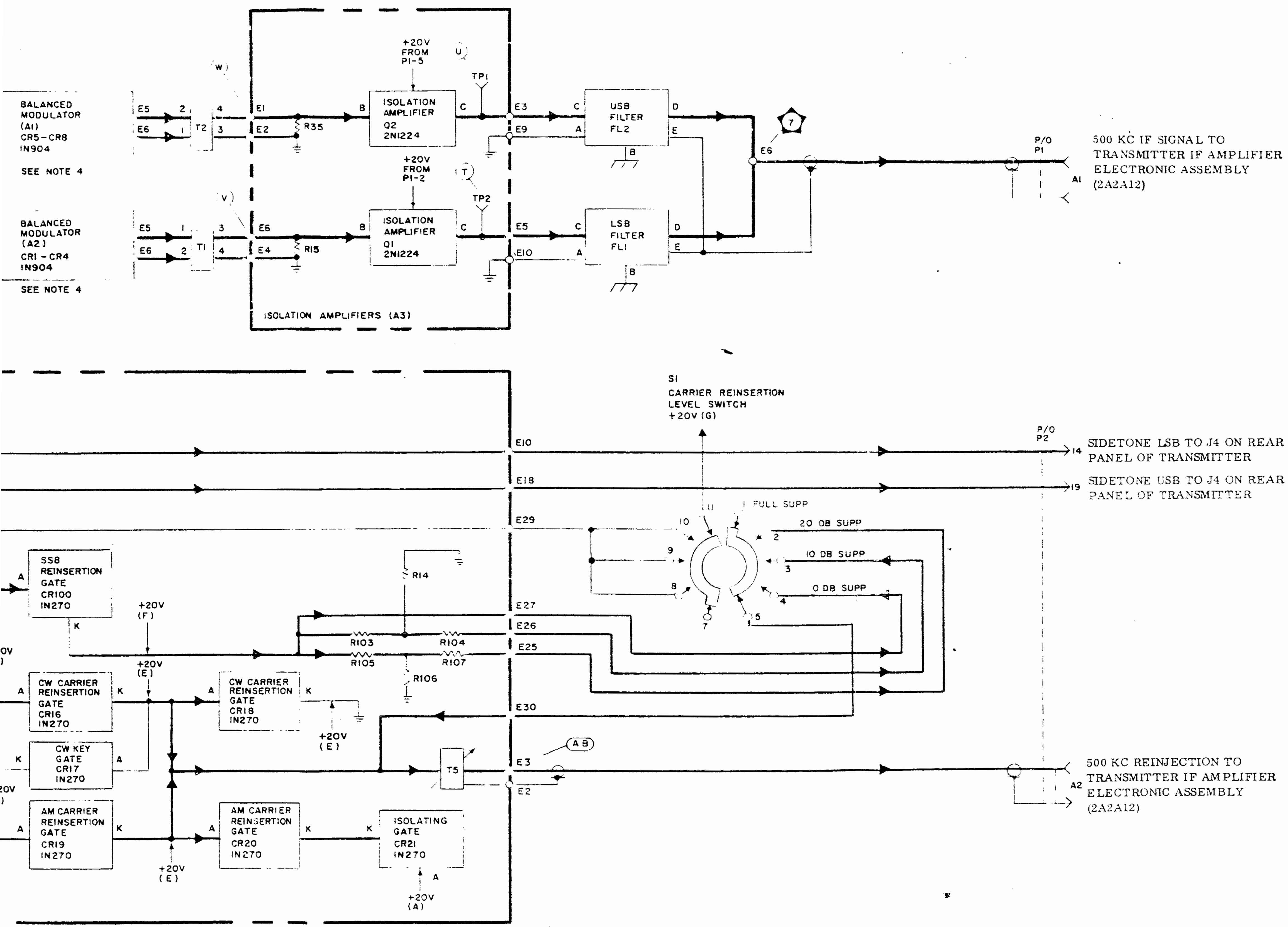
NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATH.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENTS, NUMBERS ON TRANSFORMERS INDICATE TERMINAL NUMBERS.
3. WAVEFORMS RECORDED USING OSCILLOSCOPE AN/USM-105A.
4. REF. DESIG. PREFIX 2A2A5

Figure 4-71. Frequency Standard Electronic Assembly, Servicing Block Diagram


COMPARE
INTERNAL
EXTERNAL
SWITCH
S1
EXTERNAL 5 MC
FROM J25 ON
REAR PANEL
P/O
P1
A4
E13
E17
E30
AE
5MC
R18
R22
5 MC MULTIPL
TEMPERATURE
SENSOR
RT1
32A13
OSCILLATOR
Q1 Q2
2N388 2N388
E1
B
C
P/O OVEN CONTROL CIRCUI
R1

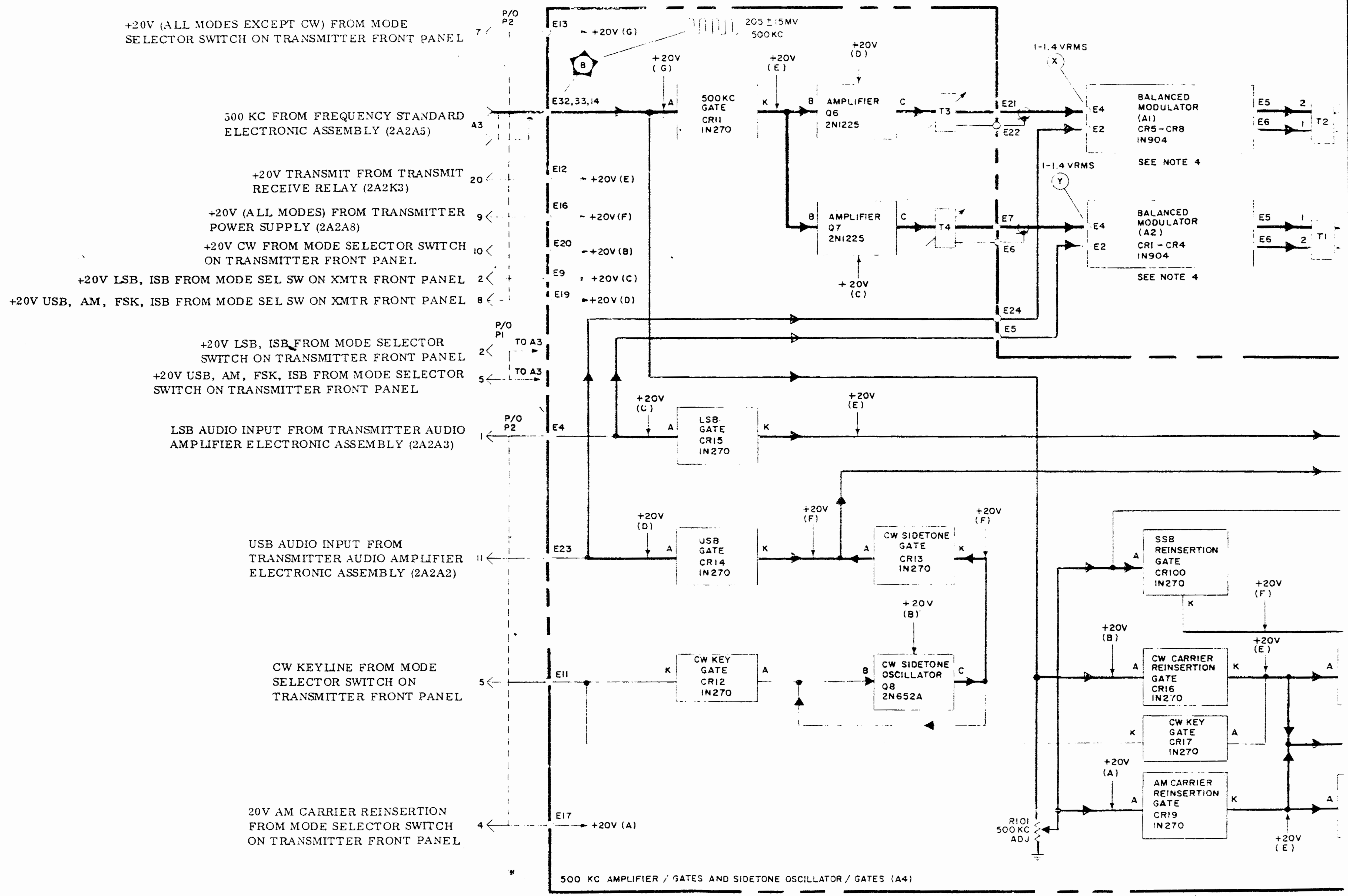
251/252



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENT. NUMBERS ON TRANSFORMERS INDICATE TERMINAL NUMBERS.
3. THE INPUT AT P1-2, 5 AND P2-2, 4, 7, 8, 9, 10, AND 20 ARE GATE CONTROL SIGNALS. THE APPLICATIONS OF THESE ARE INDICATED ON THIS DIAGRAM BY ⟶
4. SEE FIGURE 5-6 FOR A DETAILED SCHEMATIC OF BALANCED MODULATOR.
5. ALL VOLTAGES ARE DC UNLESS OTHERWISE SPECIFIED.
6. REF. DESIG. PREFIX 2A2A1.

Figure 4-72. Transmitter Mode Selector Electronic Assembly, Servicing Block Diagram


+20V (ALL MODES EXCEPT CW) FROM MODE SELECTOR SWITCH ON TRANSMITTER FRONT PANEL
500 KC FROM FREQUENCY STANDARD ELECTRONIC ASSEMBLY (2A2A5)
+20V TRANSMIT FROM TRANSMIT RECEIVE RELAY (2A2K3)
+20V (ALL MODES) FROM TRANSMITTER POWER SUPPLY (2A2A8)
+20V CW FROM MODE SELECTOR SWITCH ON TRANSMITTER FRONT PANEL
+20V LSB, ISB FROM MODE SEL SW ON XMTR FRONT PANEL
+20V USB, AM, FSK, ISB FROM MODE SEL SW ON XMTR FRONT PANEL
+20V LSB, ISB FROM MODE SELECTOR SWITCH ON TRANSMITTER FRONT PANEL
+20V USB, AM, FSK, ISB FROM MODE SELECTOR SWITCH ON TRANSMITTER FRONT PANEL
LSB AUDIO INPUT FROM TRANSMITTER AUDIO AMPLIFIER ELECTRONIC ASSEMBLY (2A2A3)
USB AUDIO INPUT FROM TRANSMITTER AUDIO AMPLIFIER ELECTRONIC ASSEMBLY (2A2A2)
CW KEYLINE FROM MODE SELECTOR SWITCH ON TRANSMITTER FRONT PANEL
20V AM CARRIER REINSERTION FROM MODE SELECTOR SWITCH ON TRANSMITTER FRONT PANEL
P/O P2
P/O P1
TO A3
205 ± 15MV 500KC
500KC GATE CR11 1N270
AMPLIFIER Q6 2N1225
AMPLIFIER Q7 2N1225
T3
T4
1-1.4 VRMS
BALANCED MODULATOR (A1) CR5-CR8 1N904
BALANCED MODULATOR (A2) CR1-CR4 1N904
SEE NOTE 4
T2
T1
LSB GATE CR15 1N270
USB GATE CR14 1N270
CW SIDETONE GATE CR13 1N270
CW KEY GATE CR12 1N270
CW SIDETONE OSCILLATOR Q8 2N652A
SSB REINSERTION GATE CR100 1N270
CW CARRIER REINSERTION GATE CR16 1N270
CW KEY GATE CR17 1N270
AM CARRIER REINSERTION GATE CR19 1N270
R101 500 KC ADJ
500 KC AMPLIFIER / GATES AND SIDETONE OSCILLATOR / GATES (A4)

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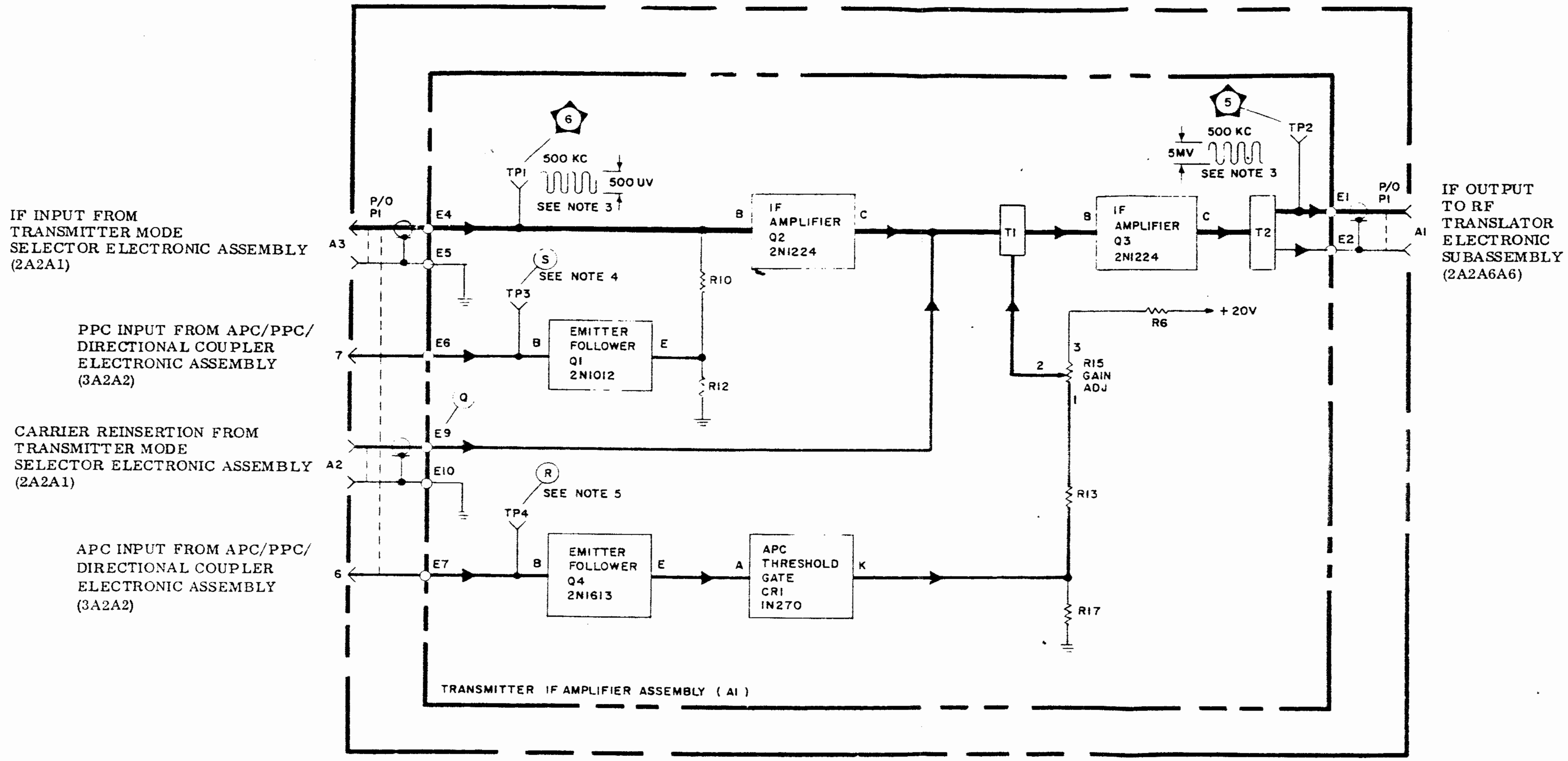
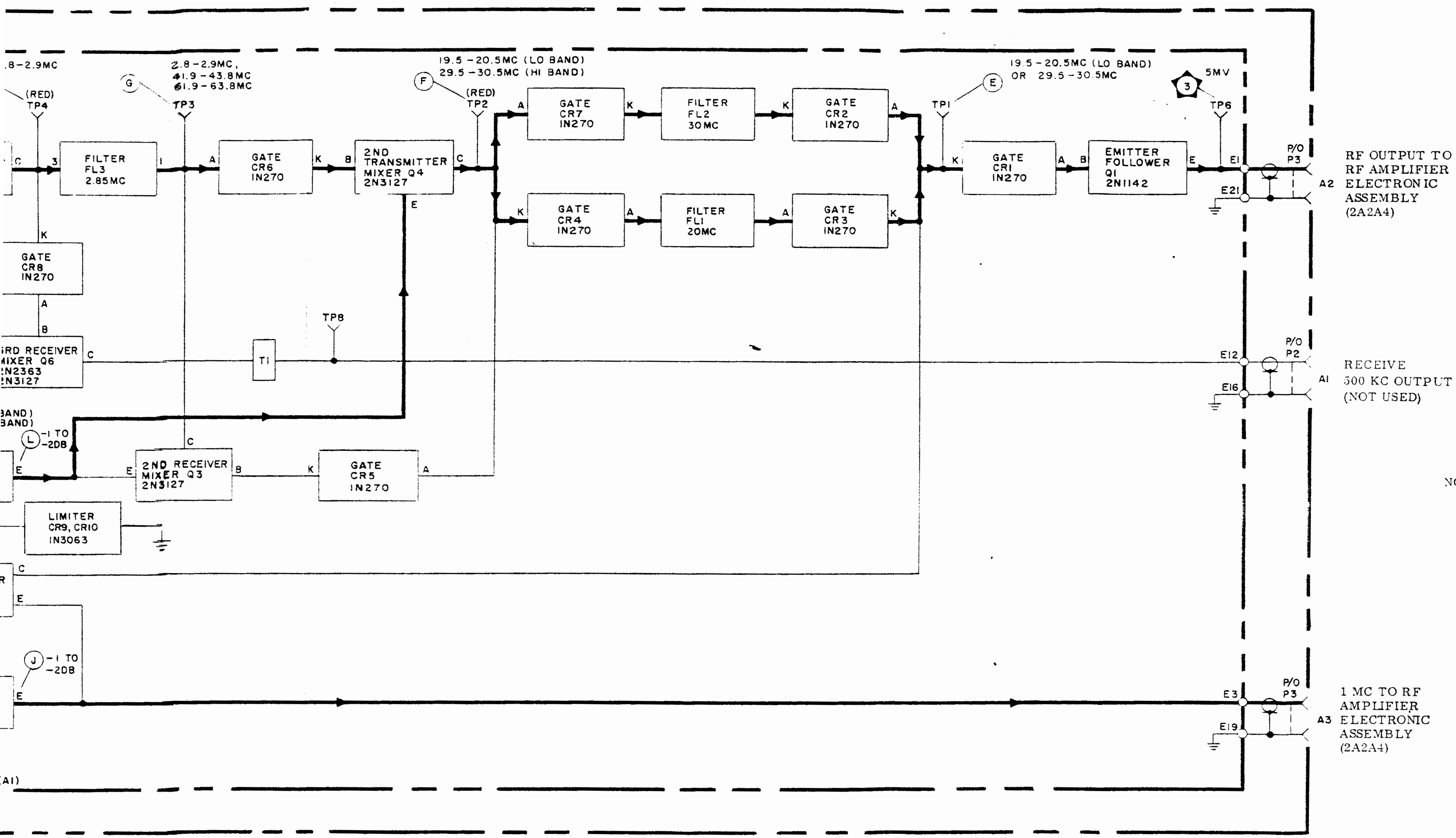
255/256



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND D BLOCKS INDICATE ELEMENT.
3. AM MODE, CARRIER, WITH NO MODUL
4. VOLTAGE AT THIS POINT (TP3) IS A FU OF THE DRIVE LEVEL TO THE OUTPUT OF THE AM-3007/URT. UNDER CONDIT NO DRIVE OR INSUFFICIENT DRIVE TO GRID CURRENT IN THE FINAL STAGE, NOMINALLY AT 5V DC. APPLICATION MODULATION TO THE FINAL STAGE, SUFFICIENT AMPLITUDE TO DRAW GR CURRENT, WILL SUPERIMPOSE GRID PULSES ON THE LINE.
5. TP4 WILL SHOW 0V DC UNLESS AM-300 HAS RF OUTPUT. IN AM MODE, WITH OUTPUT FROM AM-3007/URT, TP4 WIL +5.2 TO +5.8V DC.
6. WAVEFORMS RECORDED USING OSCILL AN/USM-105A.
7. ALL VOLTAGES DC UNLESS OTHERWIS SPECIFIED.
8. REF. DESIG. PREFIX 2A2A12.

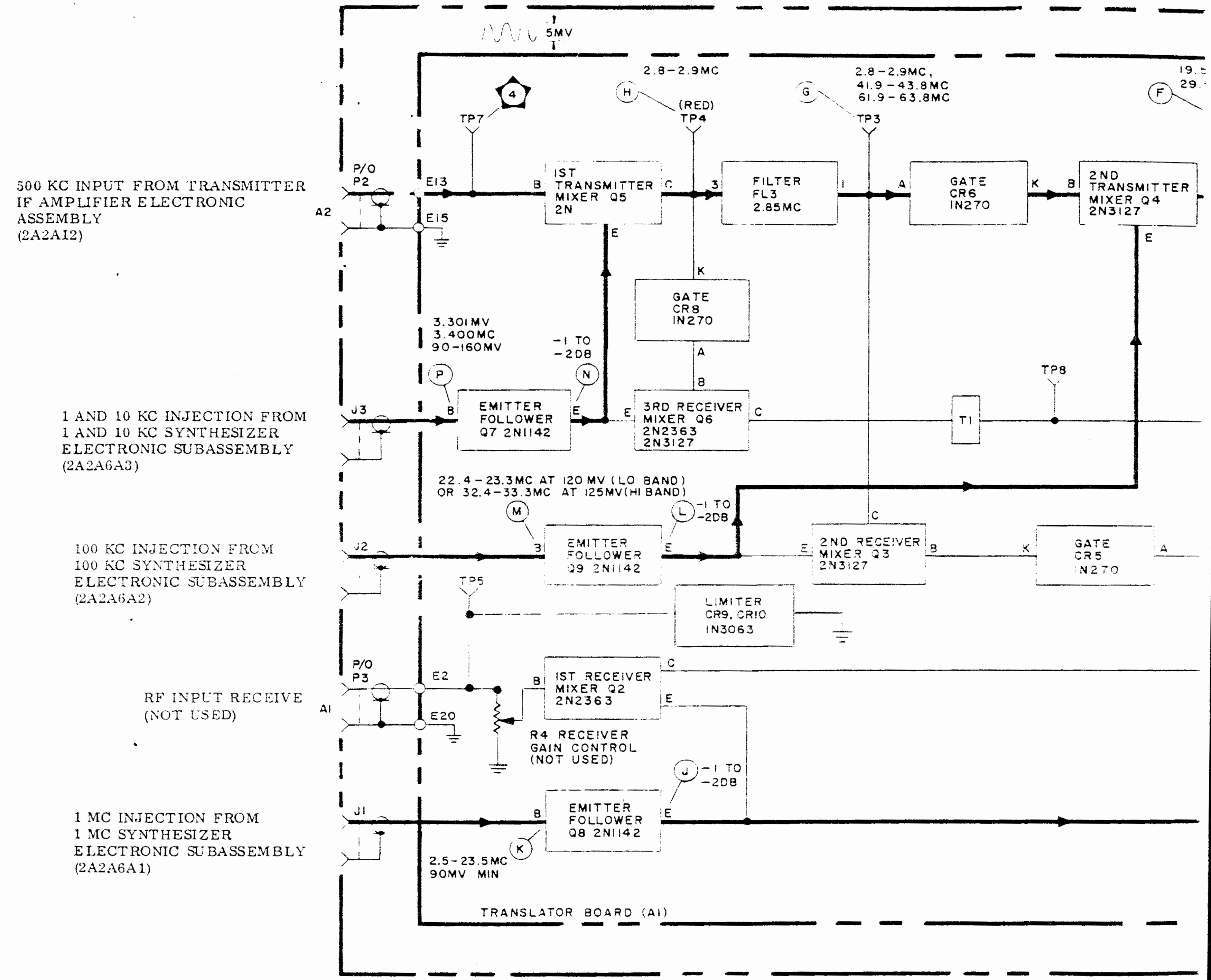
Figure 4-73. Transmitter IF. Ampli Electronic Assembly, Servicing Block Diagram

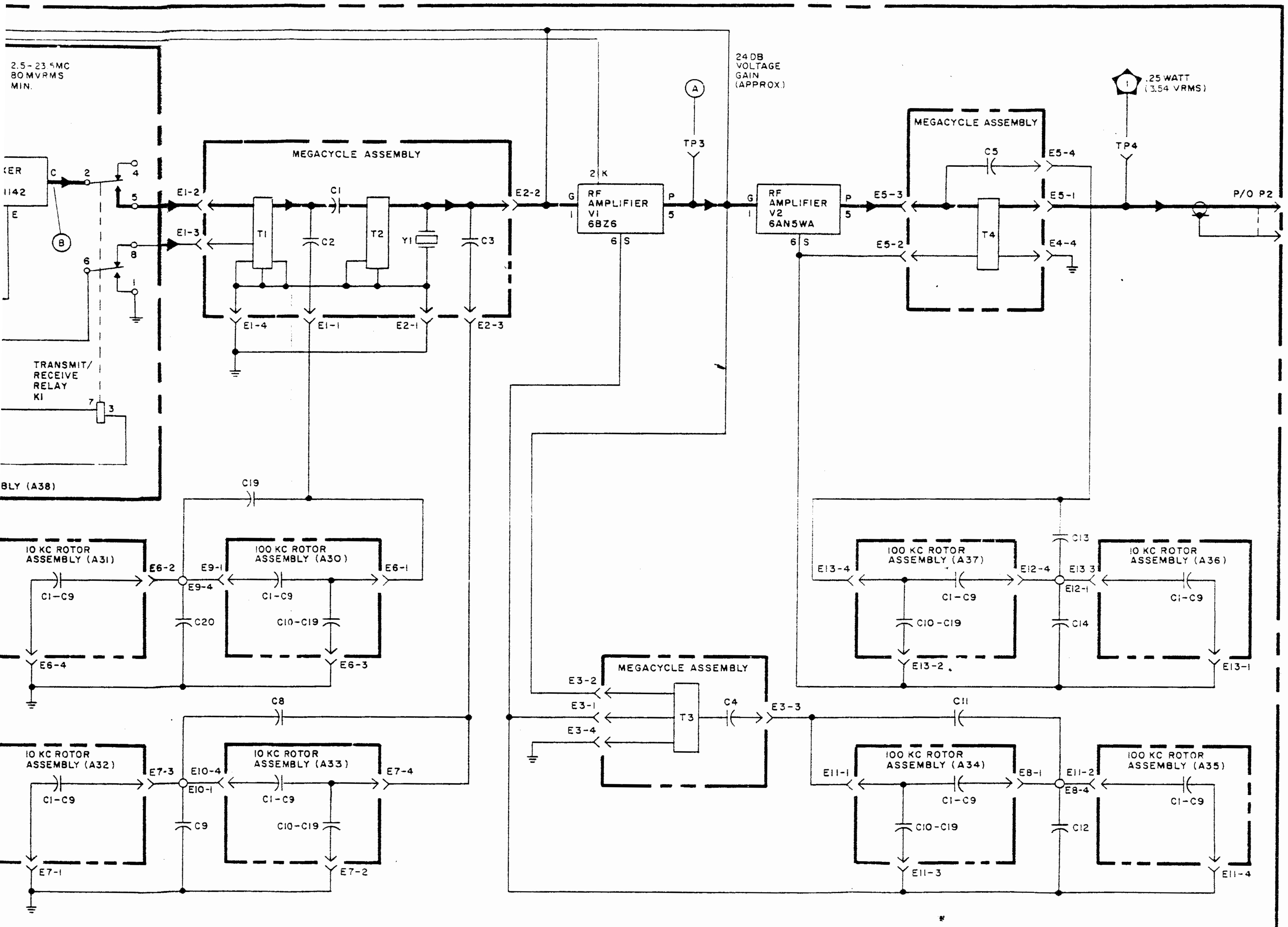


NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENTS.
3. REF. DESIG. PREFIX 2A2A6A6.

Figure 4-74. RF Translator Electronic Subassembly, Servicing Block Diagram


500 KC INPUT FROM TRANSMITTER IF AMPLIFIER ELECTRONIC ASSEMBLY (2A2A12)
1 AND 10 KC INJECTION FROM 1 AND 10 KC SYNTHESIZER ELECTRONIC SUBASSEMBLY (2A2A6A3)
100 KC INJECTION FROM 100 KC SYNTHESIZER ELECTRONIC SUBASSEMBLY (2A2A6A2)
RF INPUT RECEIVE (NOT USED)
1 MC INJECTION FROM 1 MC SYNTHESIZER ELECTRONIC SUBASSEMBLY (2A2A6A1)
5MV
2.8-2.9MC
(RED) TP4
2.8-2.9MC, 41.9-43.8MC 61.9-63.8MC
TP3
TP7
P/O P2
E13
E15
A2
1ST TRANSMITTER MIXER Q5 2N
FILTER FL3 2.85MC
GATE CR6 1N270
2ND TRANSMITTER MIXER Q4 2N3127
GATE CR8 1N270
3.301MV 3.400MC 90-160MV
-1 TO -2DB
J3
EMITTER FOLLOWER Q7 2N1142
3RD RECEIVER MIXER Q6 2N2363 2N3127
T1
TP8
22.4-23.3MC AT 120 MV (LO BAND) OR 32.4-33.3MC AT 125MV(HI BAND)
-1 TO -2DB
J2
EMITTER FOLLOWER Q9 2N1142
2ND RECEIVER MIXER Q3 2N3127
GATE CR5 1N270
TP5
LIMITER CR9, CR10 1N3063
P/O P3
E2
E20
A1
1ST RECEIVER MIXER Q2 2N2363
R4 RECEIVER GAIN CONTROL (NOT USED)
-1 TO -2DB
J1
EMITTER FOLLOWER Q8 2N1142
2.5-23.5MC 90MV MIN
TRANSLATOR BOARD (A1)

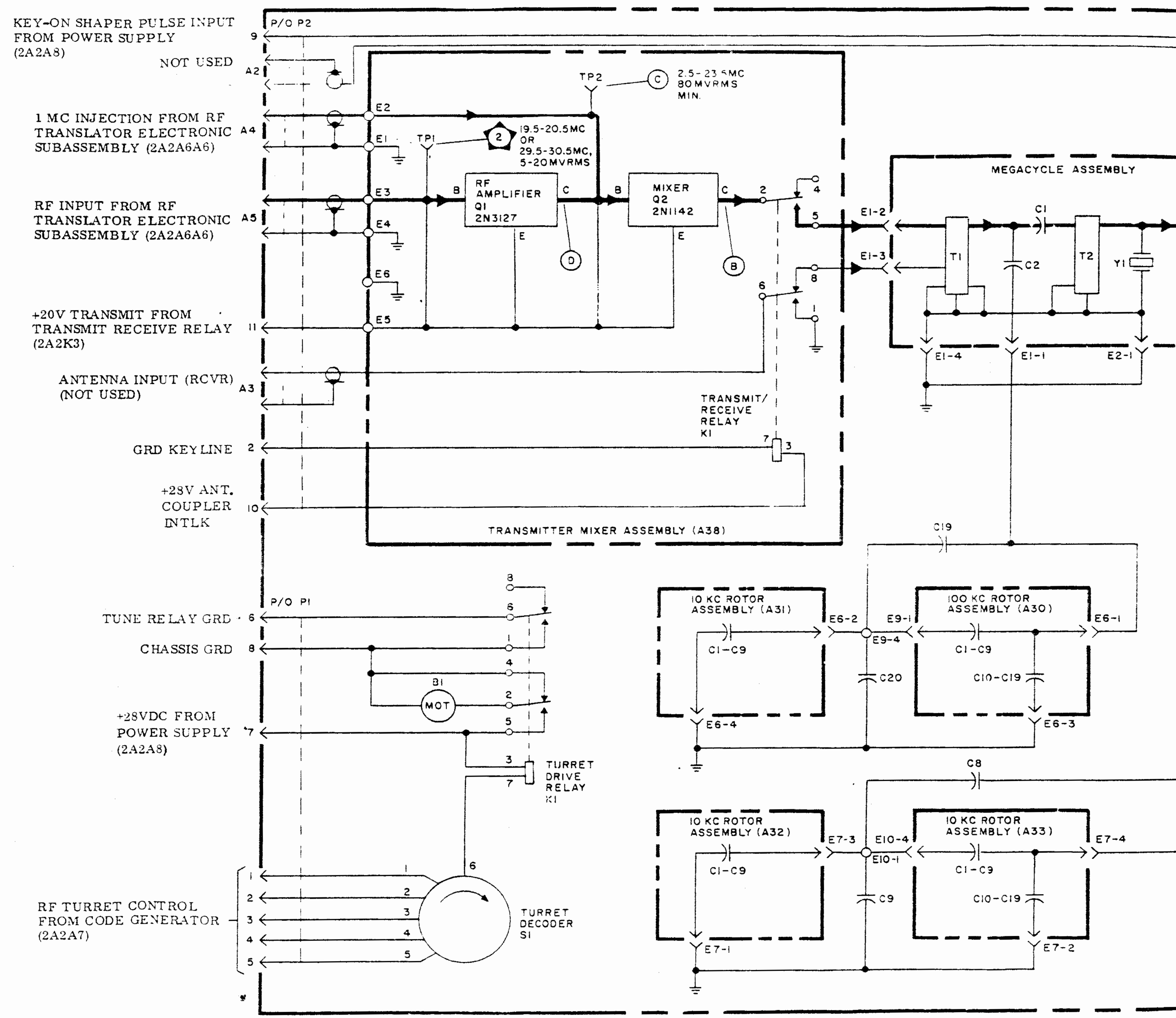


RF OUTPUT TO
RF AMPLIFIER AM-3007/URT
(3A2)

NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND TUBE BLOCKS INDICATE ELEMENT.
3. ALL VOLTAGES ARE DC UNLESS OTHERWISE SPECIFIED.
4. REF. DESIG. PREFIX 2A2A4.

Figure 4-75. RF Amplifier Electronic Assembly, Servicing Block Diagram


KEY-ON SHAPER PULSE INPUT FROM POWER SUPPLY (2A2A8)
NOT USED
1 MC INJECTION FROM RF TRANSLATOR ELECTRONIC SUBASSEMBLY (2A2A6A6)
RF INPUT FROM RF TRANSLATOR ELECTRONIC SUBASSEMBLY (2A2A6A6)
+20V TRANSMIT FROM TRANSMIT RECEIVE RELAY (2A2K3)
ANTENNA INPUT (RCVR) (NOT USED)
GRD KEYLINE
+28V ANT. COUPLER INTLK
P/O P2
TP2
2.5-23.5MC 80MVRMS MIN.
TP1
19.5-20.5MC OR 29.5-30.5MC, 5-20MVRMS
RF AMPLIFIER Q1 2N3127
MIXER Q2 2N1142
MEGACYCLE ASSEMBLY
TRANSMIT/ RECEIVE RELAY K1
TRANSMITTER MIXER ASSEMBLY (A38)
P/O P1
TUNE RELAY GRD
CHASSIS GRD
+28VDC FROM POWER SUPPLY (2A2A8)
MOT
TURRET DRIVE RELAY K1
RF TURRET CONTROL FROM CODE GENERATOR (2A2A7)
TURRET DECODER S1
10 KC ROTOR ASSEMBLY (A31)
100 KC ROTOR ASSEMBLY (A30)
10 KC ROTOR ASSEMBLY (A32)
10 KC ROTOR ASSEMBLY (A33)
C1-C9
C10-C19
C19
C20
C8
C9

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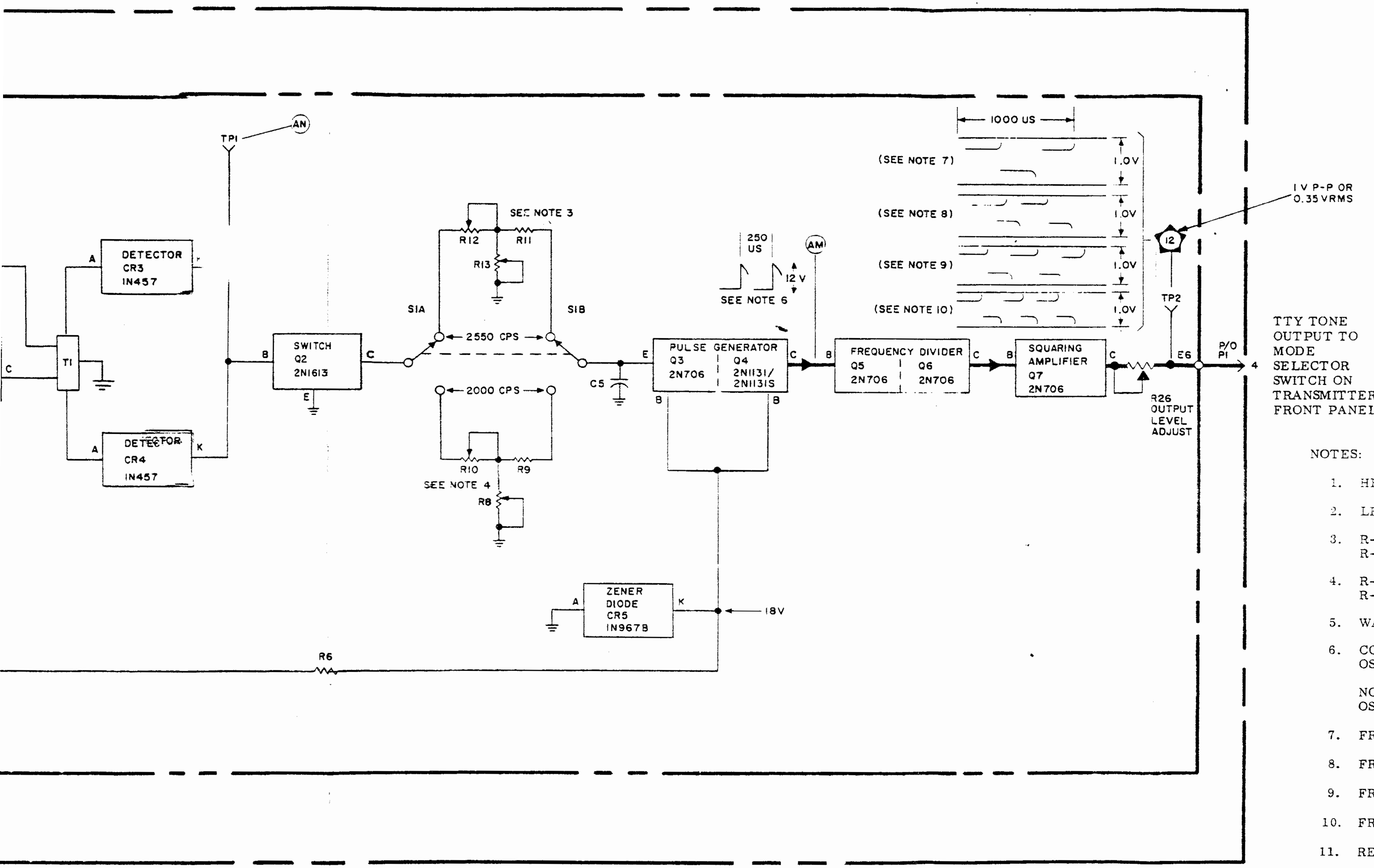


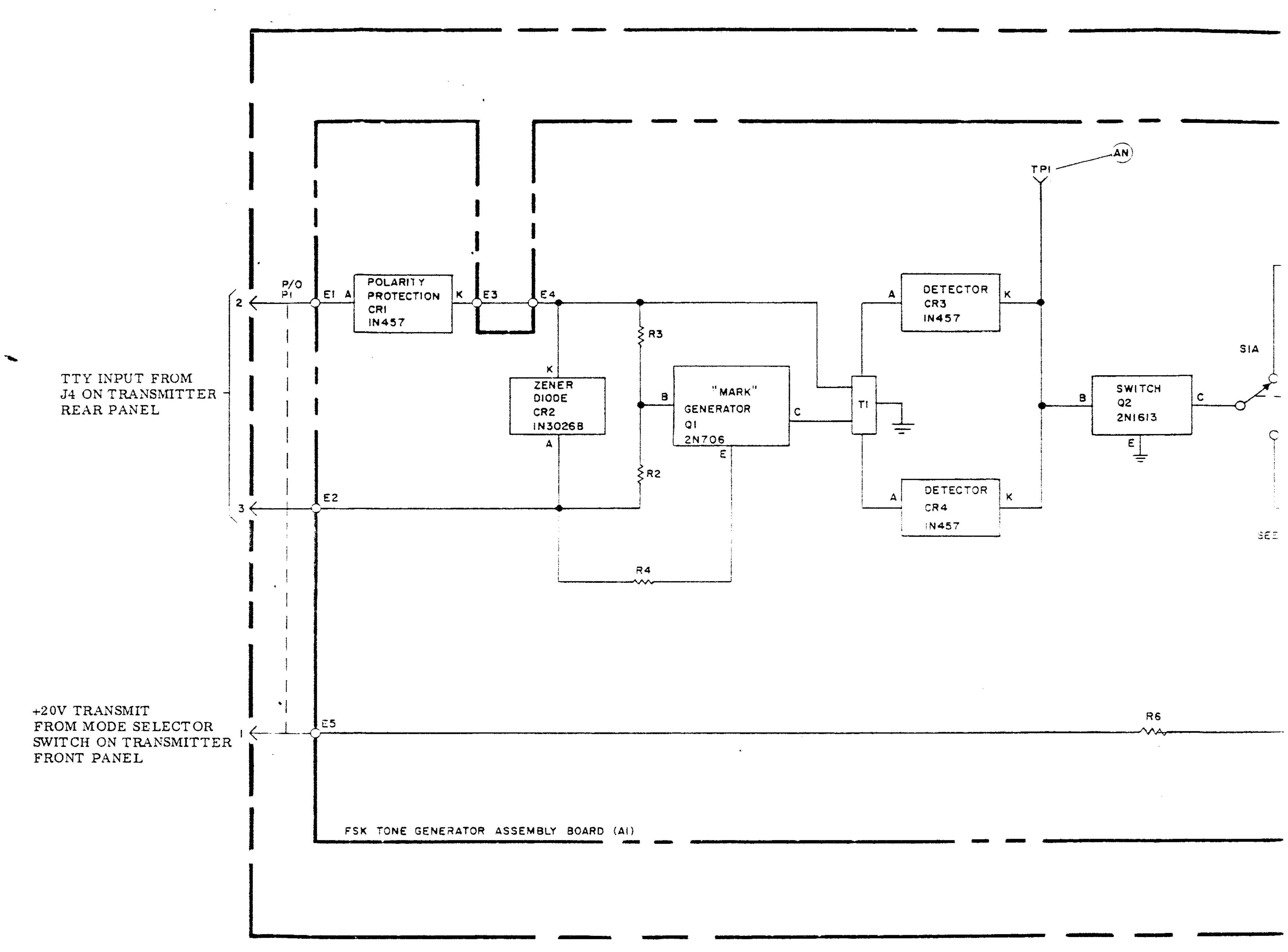
TTY TONE OUTPUT TO MODE SELECTOR SWITCH ON TRANSMITTER FRONT PANEL

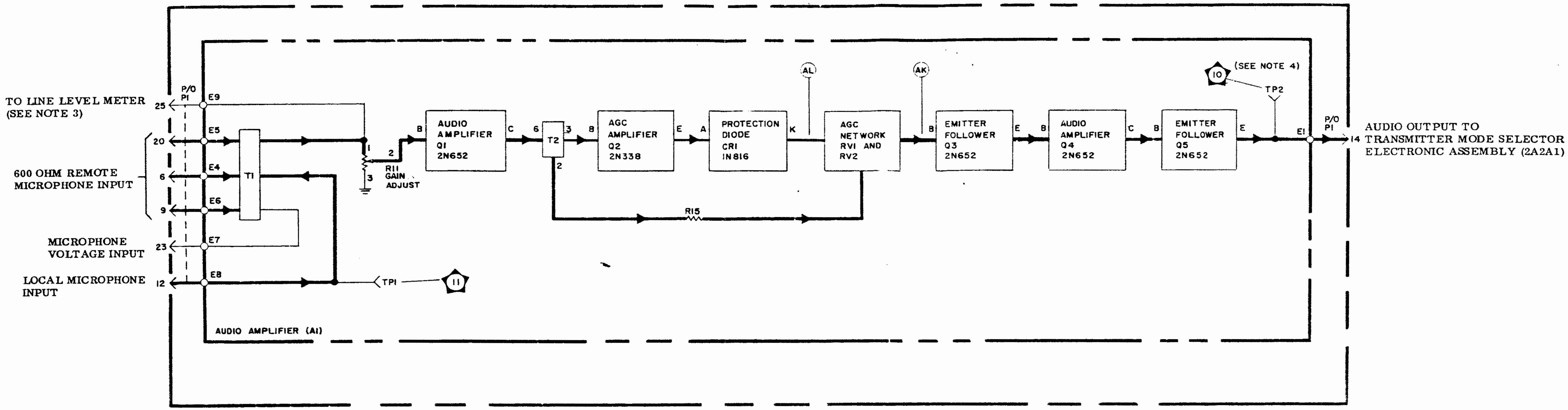
NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS.
2. LETTERS OUTSIDE OF TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENTS.
3. R-12 ADJUSTED FOR 2550 CPS CENTER FREQ "MARK" (2975 CPS)
   R-13 ADJUSTED FOR 2550 CPS CENTER FREQ "SPACE" (2125 CPS).
4. R-10 ADJUSTED FOR 2000 CPS CENTER FREQ "MARK" (2425 CPS)
   R-8 ADJUSTED FOR 2000 CPS CENTER FREQ "SPACE" (1575 CPS).
5. WAVEFORMS RECORDED ON OSCILLOSCOPE AN/USM-105A.
6. COLLECTOR OF Q4 TTY FUNCTION: SPACE
   OSCILLOSCOPE SETTING: 0.5 V/CM X 10, 100 USEC/CM.

   NOTES 7, 8, 9, 10 APPLY TO WAVEFORM AT TP2.
   OSCILLOSCOPE SETTING: 0.5V/CM X 10, 100 USEC/CM.
7. FREQ - 1575 CPS, FUNCTION - SPACE, CENTER FREQ - 2000 CPS.
8. FREQ - 2125 CPS, FUNCTION - SPACE, CENTER FREQ - 2550 CPS.
9. FREQ - 2425 CPS, FUNCTION - MARK, CENTER FREQ - 2000 CPS.
10. FREQ - 2975 CPS, FUNCTION - MARK, CENTER FREQ - 2550 CPS.
11. REF. DESIG. PREFIX 2A2A9.

Figure 4-76. FSK Tone Generator Electronic Assembly, Servicing Block Diagram


TTY INPUT FROM
J4 ON TRANSMITTER
REAR PANEL
+20V TRANSMIT
FROM MODE SELECTOR
SWITCH ON TRANSMITTER
FRONT PANEL
P/O
P1
E1
E2
E3
E4
E5
POLARITY
PROTECTION
CR1
1N457
ZENER
DIODE
CR2
1N3026B
R2
R3
R4
"MARK"
GENERATOR
Q1
2N706
T1
DETECTOR
CR3
1N457
DETECTOR
CR4
1N457
TP1
AN
SWITCH
Q2
2N1613
S1A
R6
FSK TONE GENERATOR ASSEMBLY BOARD (A1)



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.

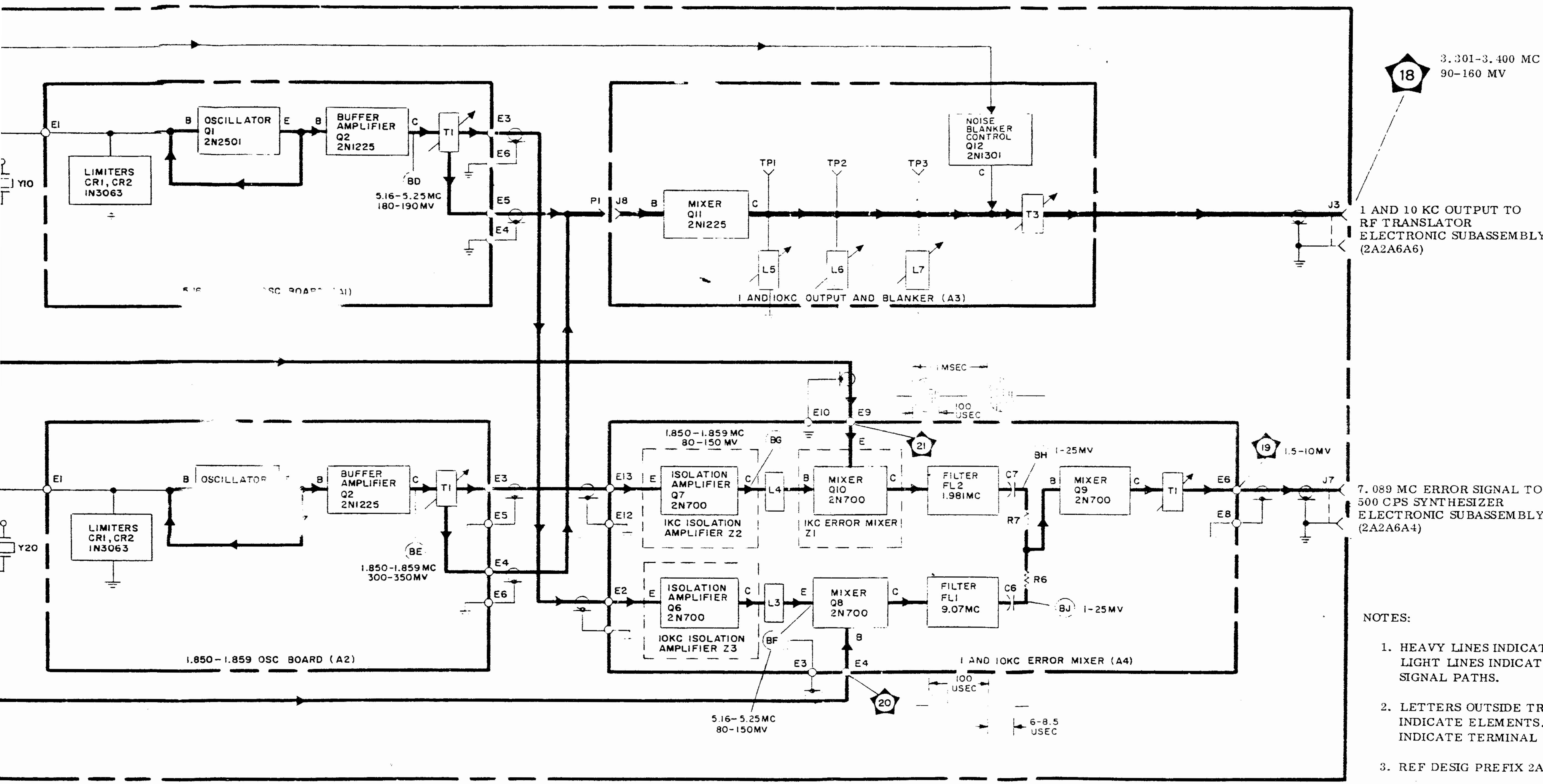
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENT. NUMBERS ON TRANSFORMERS INDICATE TERMINAL NUMBERS.

3. DURING LSB OPERATION THE AUDIO LEVEL AT P1-25 IS OBSERVED ON THE LSB LINE LEVEL METER (M1). DURING USB OPERATION THE AUDIO LEVEL AT P1-25 IS OBSERVED ON THE USB LINE LEVEL METER (M2).

4. NOMINAL OUTPUT 100MV RMS - SINGLE TONE 150MV INPUT AT PINS 20 AND 9 OF CONNECTOR P1.

5. REF. DESIG. PREFIX 2A2A2 AND 2A2A3.

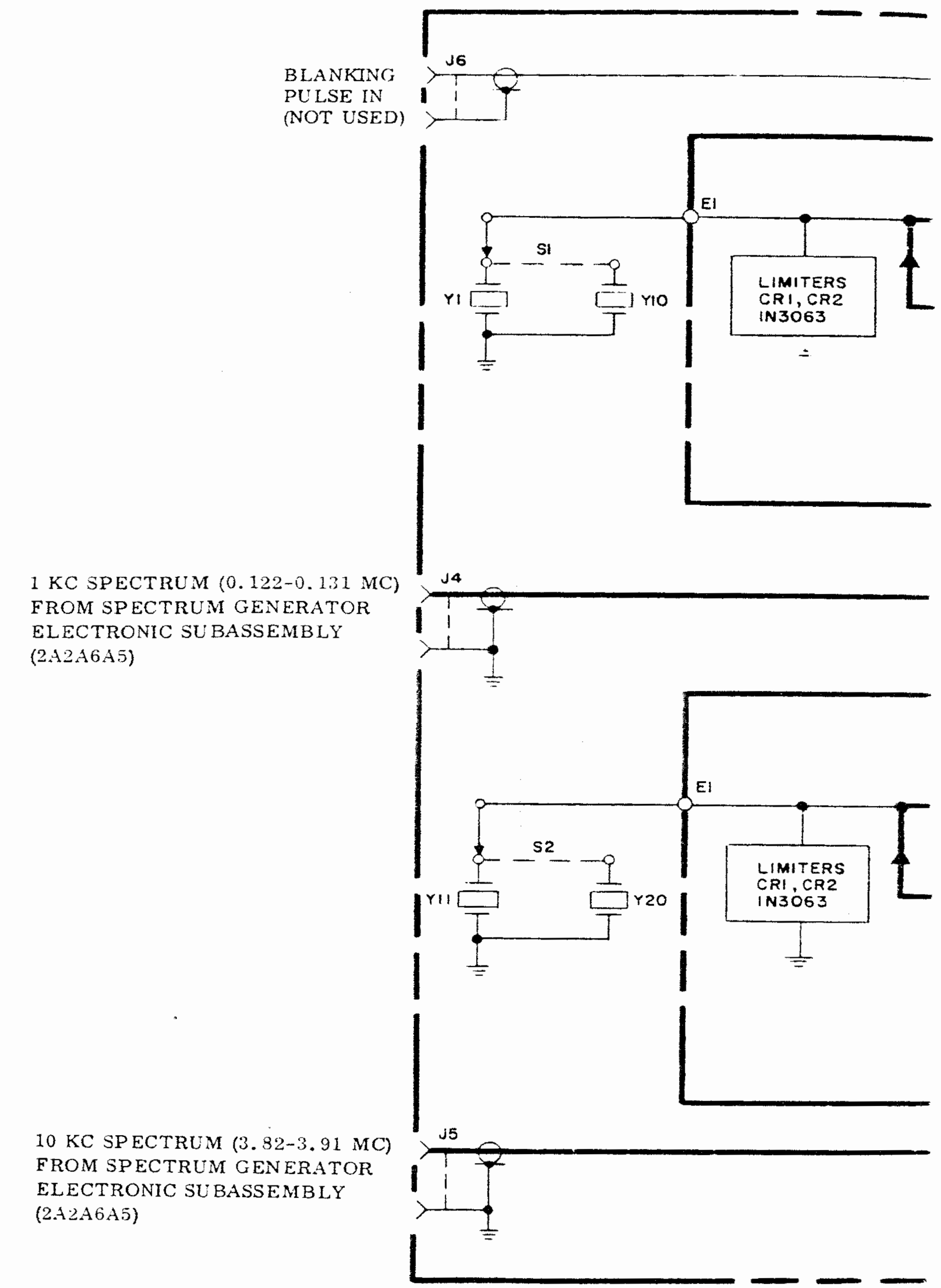
Figure 4-77. Transmitter Audio Amplifier Electronic Assembly, Servicing Block Diagram

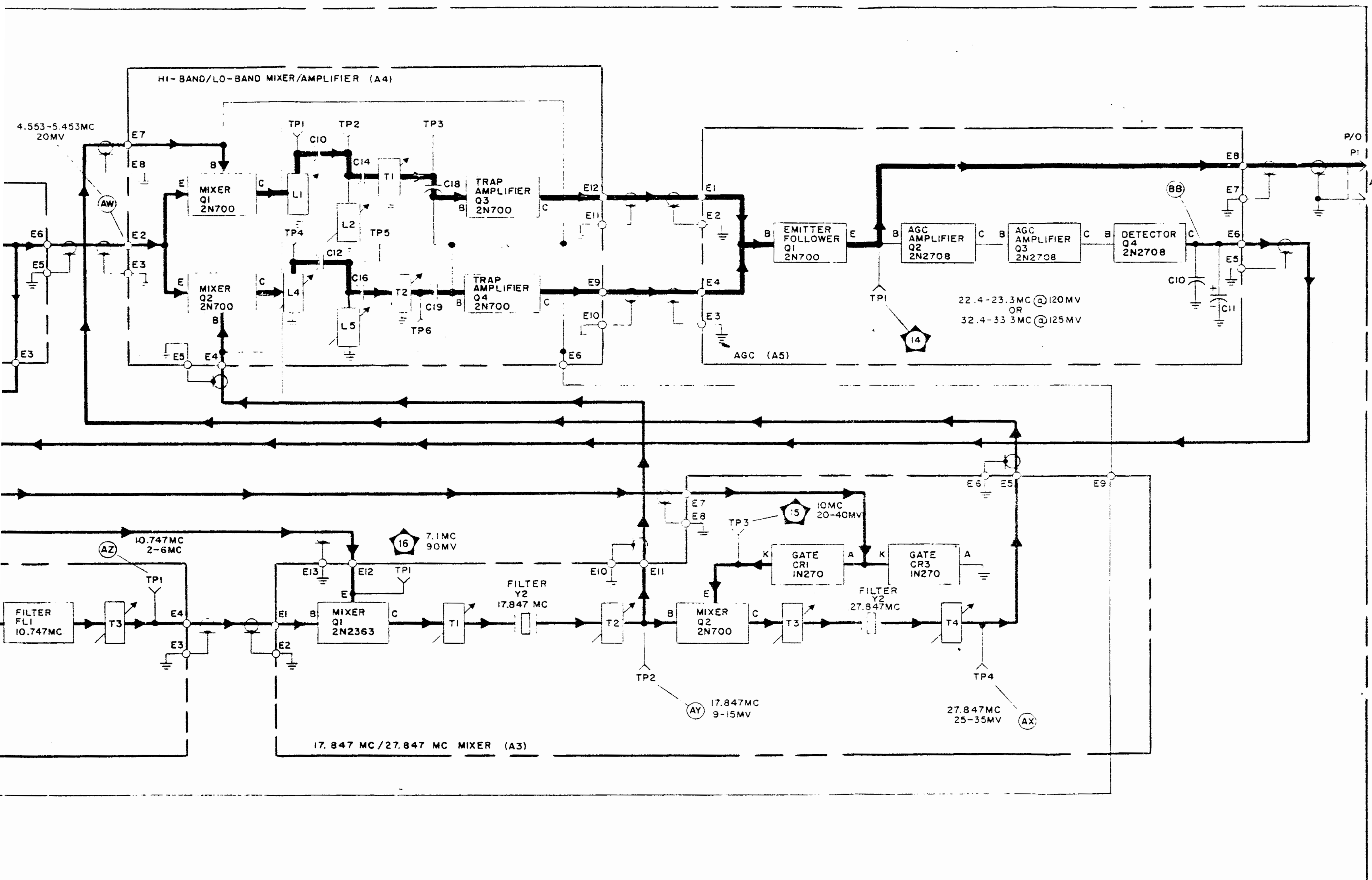


NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENTS. NUMBERS ON TRANSFORMERS INDICATE TERMINAL NUMBERS.
3. REF DESIG PREFIX 2A2A6A3.

Figure 4-78. 1 and 10 KC Synthesizer Electronic Subassembly Servicing Block Diagram


BLANKING
PULSE IN
(NOT USED)
J6
E1
S1
Y1
Y10
LIMITERS
CR1, CR2
1N3063
1 KC SPECTRUM (0.122-0.131 MC)
FROM SPECTRUM GENERATOR
ELECTRONIC SUBASSEMBLY
(2A2A6A5)
J4
E1
S2
Y11
Y20
LIMITERS
CR1, CR2
1N3063
10 KC SPECTRUM (3.82-3.91 MC)
FROM SPECTRUM GENERATOR
ELECTRONIC SUBASSEMBLY
(2A2A6A5)
J5



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCK INDICATE ELEMENTS.
3. REF. DESIG. PREFIX 2A2A6A2.

Figure 4-79. 100 KC Synthesizer Electronic Subassembly, Servicing Block Diagram

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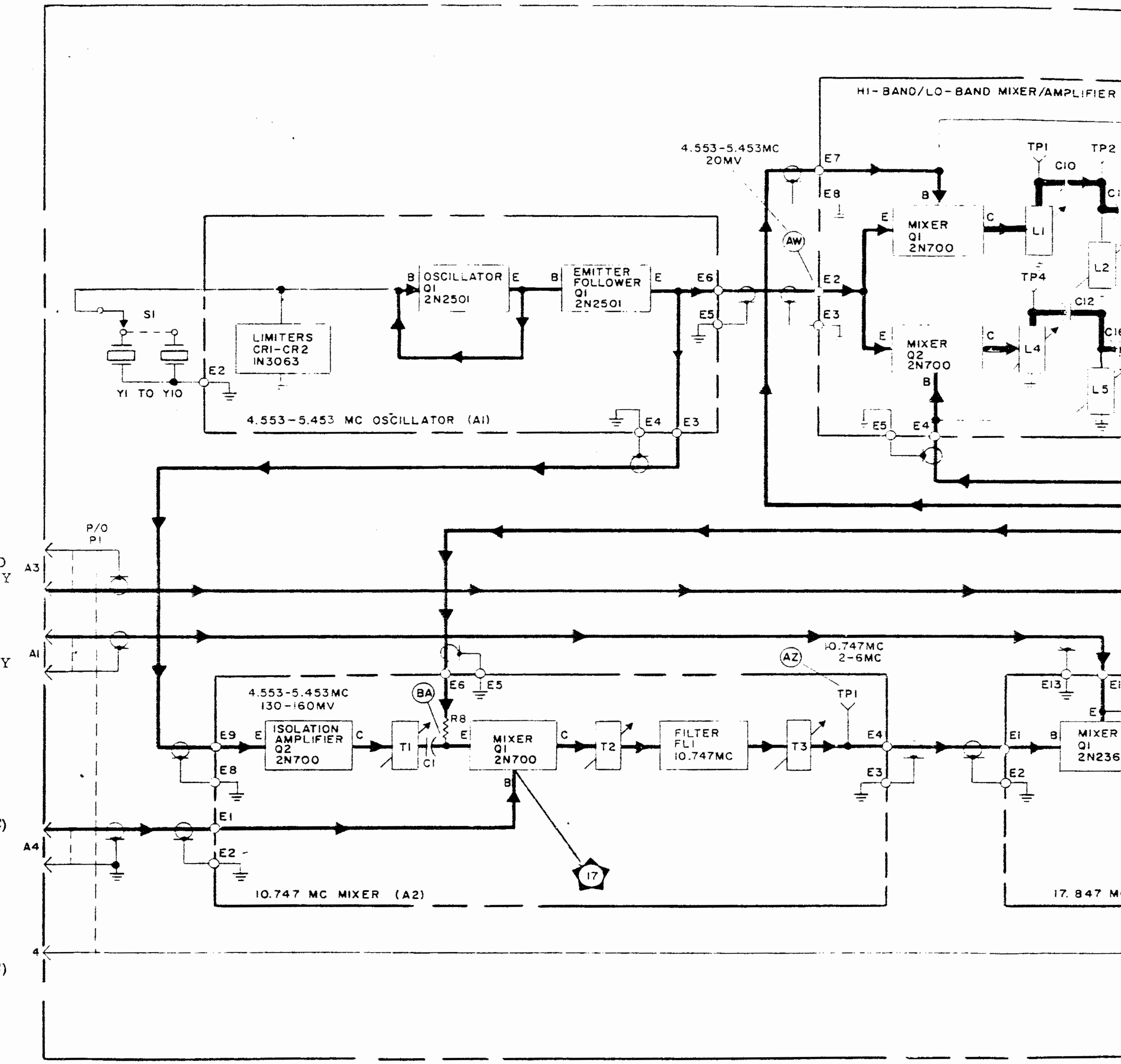


'0 KC SPECTRUM (15.3 - 16.2 MC)
OM SPECTRUM GENERATOR
ELECTRONIC SUBASSEMBLY
(2A2A6A5)

NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENTS.
3. WAVEFORMS RECORDED USING OSCILLOSCOPE AN/USM-105A.
4. REF. DESIG. PREFIX 2A6A1

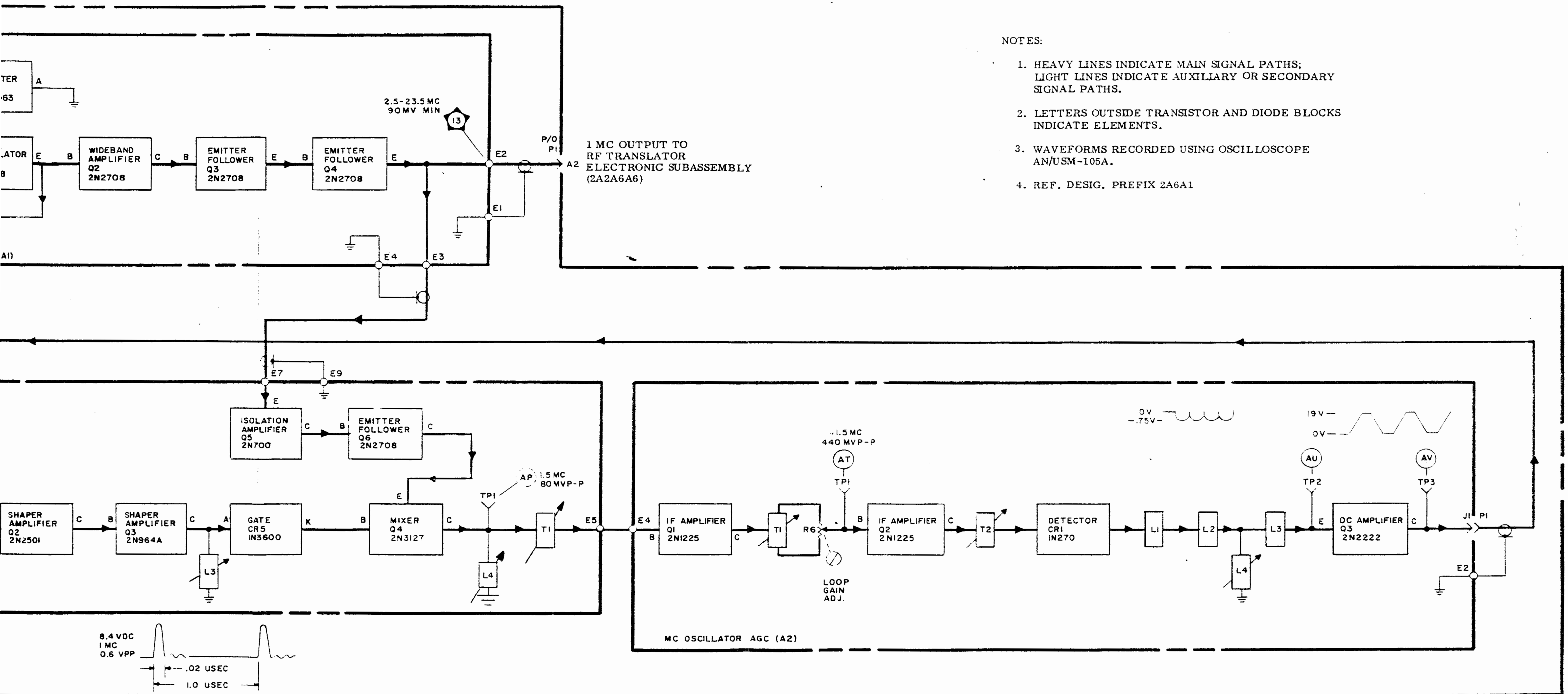
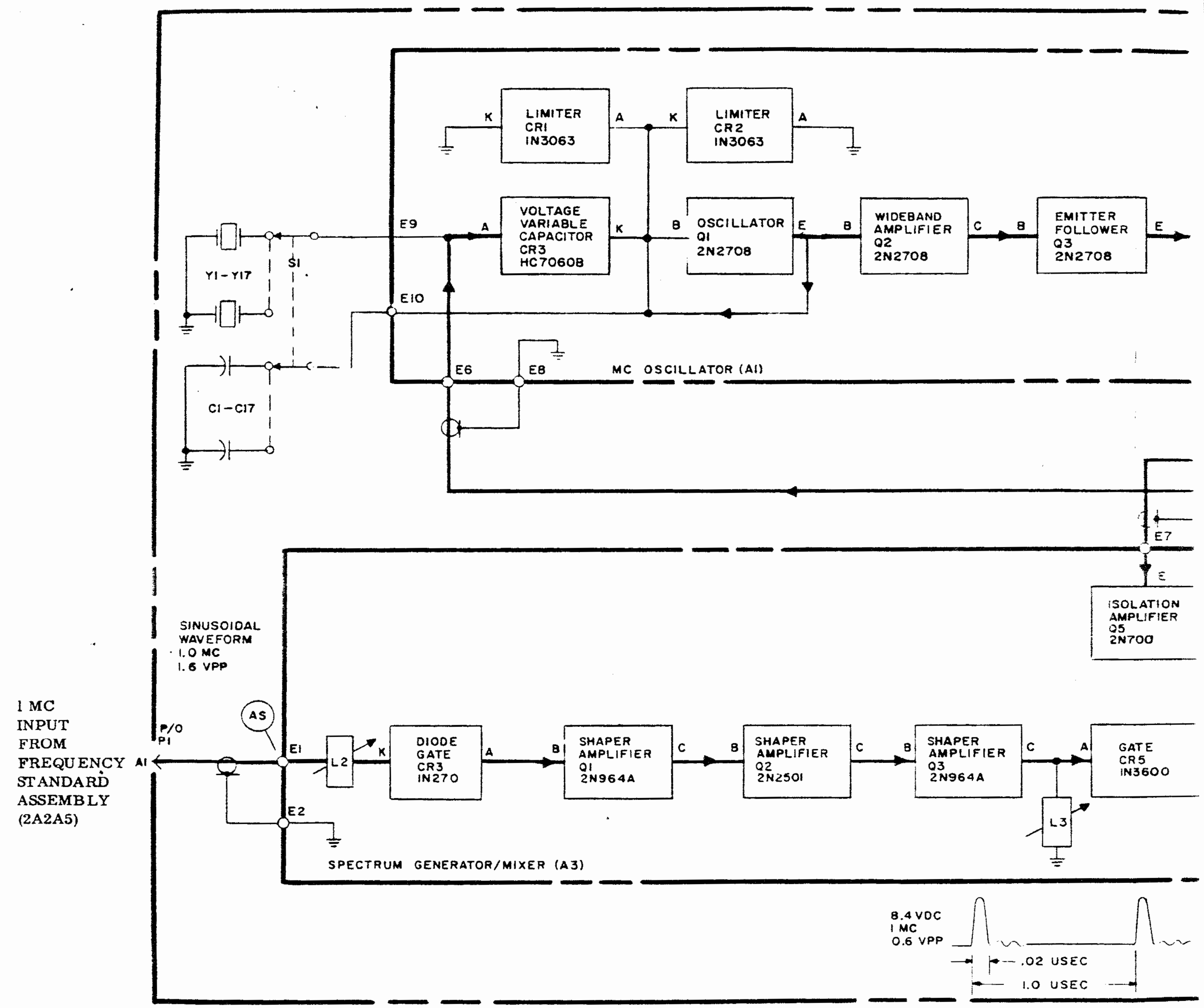
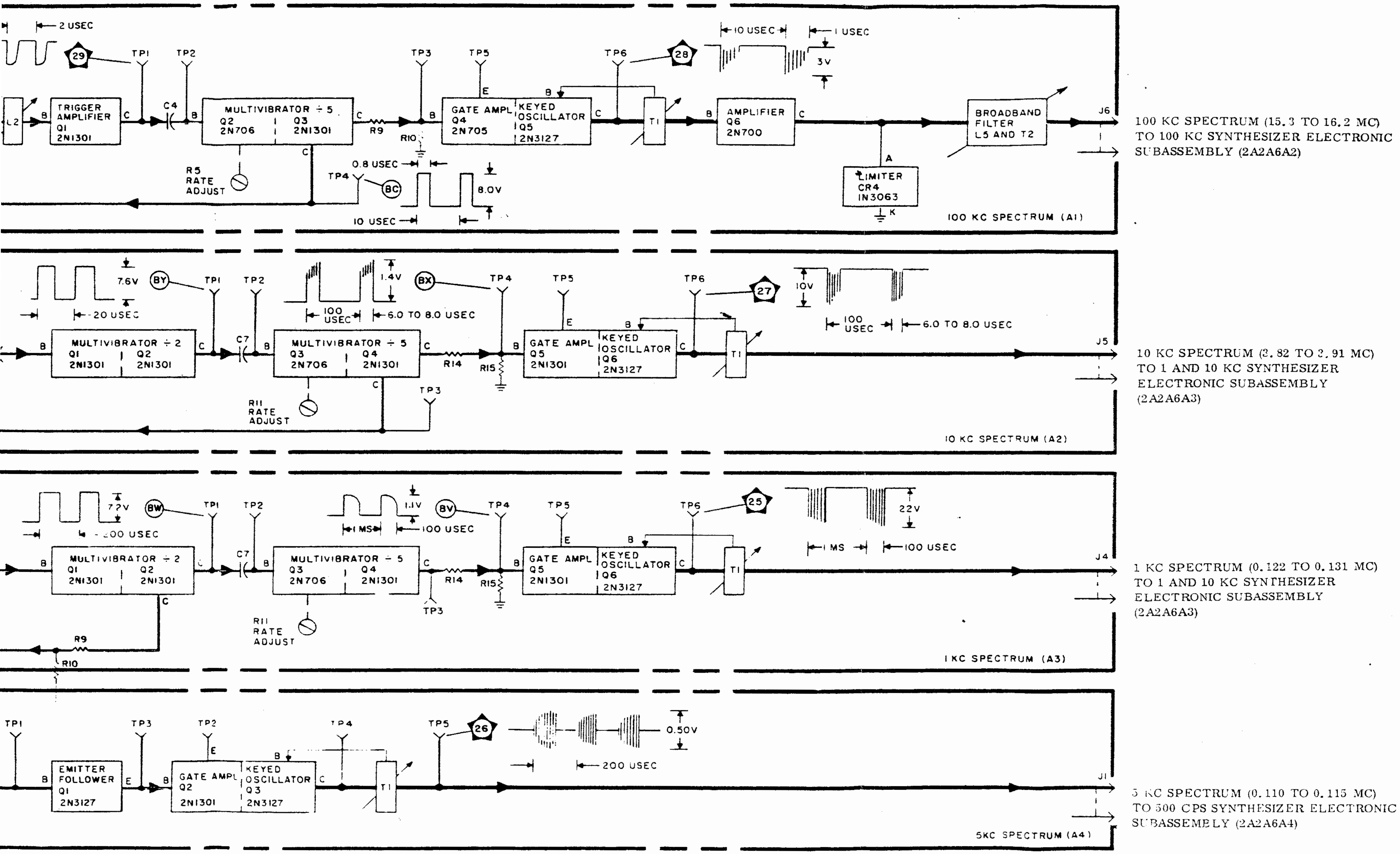


Figure 4-80. 1 MC Synthesizer Electronic Subassembly, Servicing Block Diagram

269/270

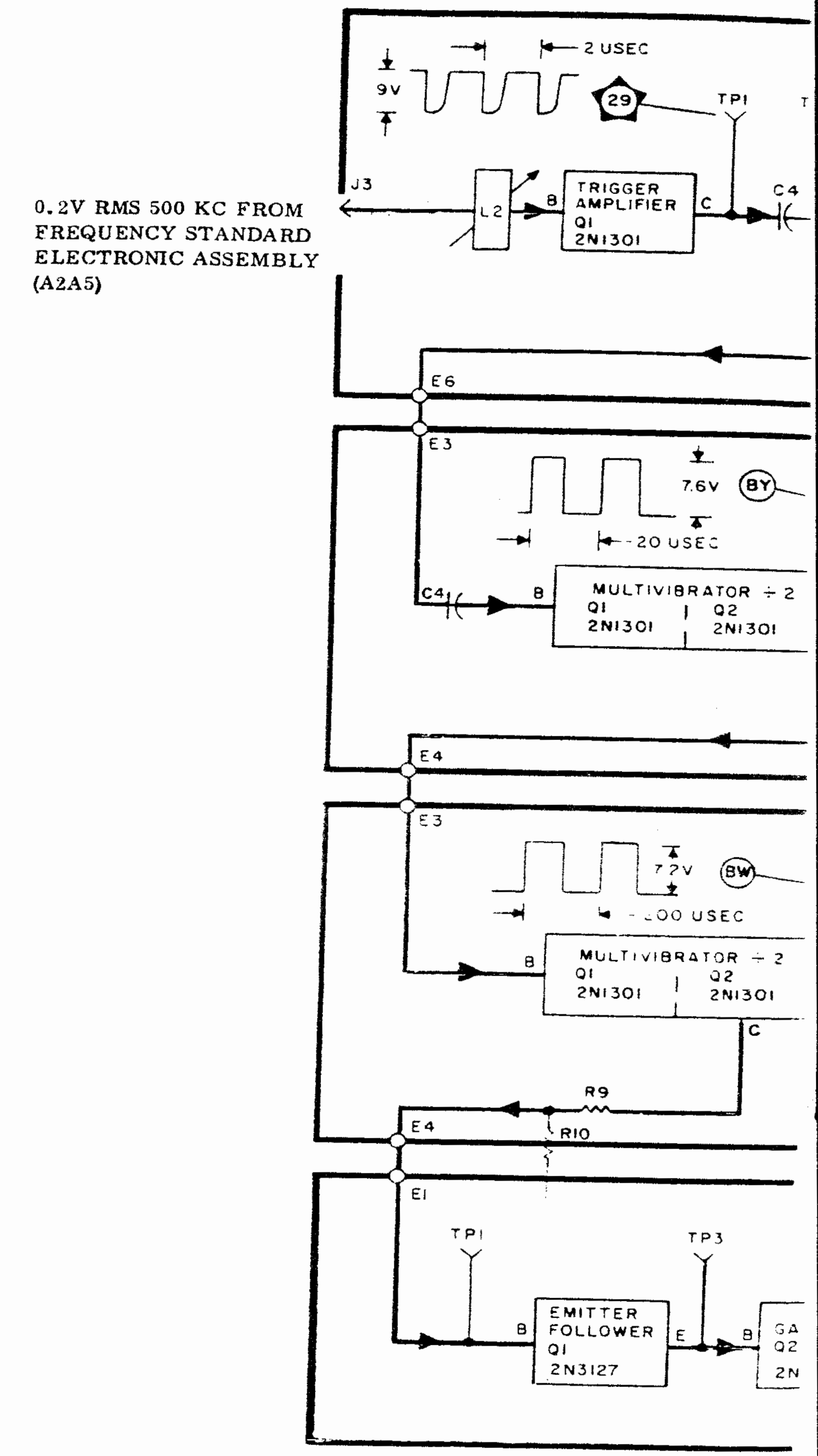

1 MC
INPUT
FROM
FREQUENCY
STANDARD
ASSEMBLY
(2A2A5)
LIMITER
CR1
IN3063
LIMITER
CR2
IN3063
VOLTAGE
VARIABLE
CAPACITOR
CR3
HC7060B
OSCILLATOR
Q1
2N2708
WIDEBAND
AMPLIFIER
Q2
2N2708
EMITTER
FOLLOWER
Q3
2N2708
Y1-Y17
C1-C17
S1
E9
E10
E6
E8
MC OSCILLATOR (A1)
E7
ISOLATION
AMPLIFIER
Q5
2N700
SINUSOIDAL
WAVEFORM
1.0 MC
1.6 VPP
AS
P/O
P1
A1
E1
E2
L2
DIODE
GATE
CR3
IN270
SHAPER
AMPLIFIER
Q1
2N964A
SHAPER
AMPLIFIER
Q2
2N2501
SHAPER
AMPLIFIER
Q3
2N964A
GATE
CR5
IN3600
L3
SPECTRUM GENERATOR/MIXER (A3)
8.4 VDC
1 MC
0.6 VPP
.02 USEC
1.0 USEC

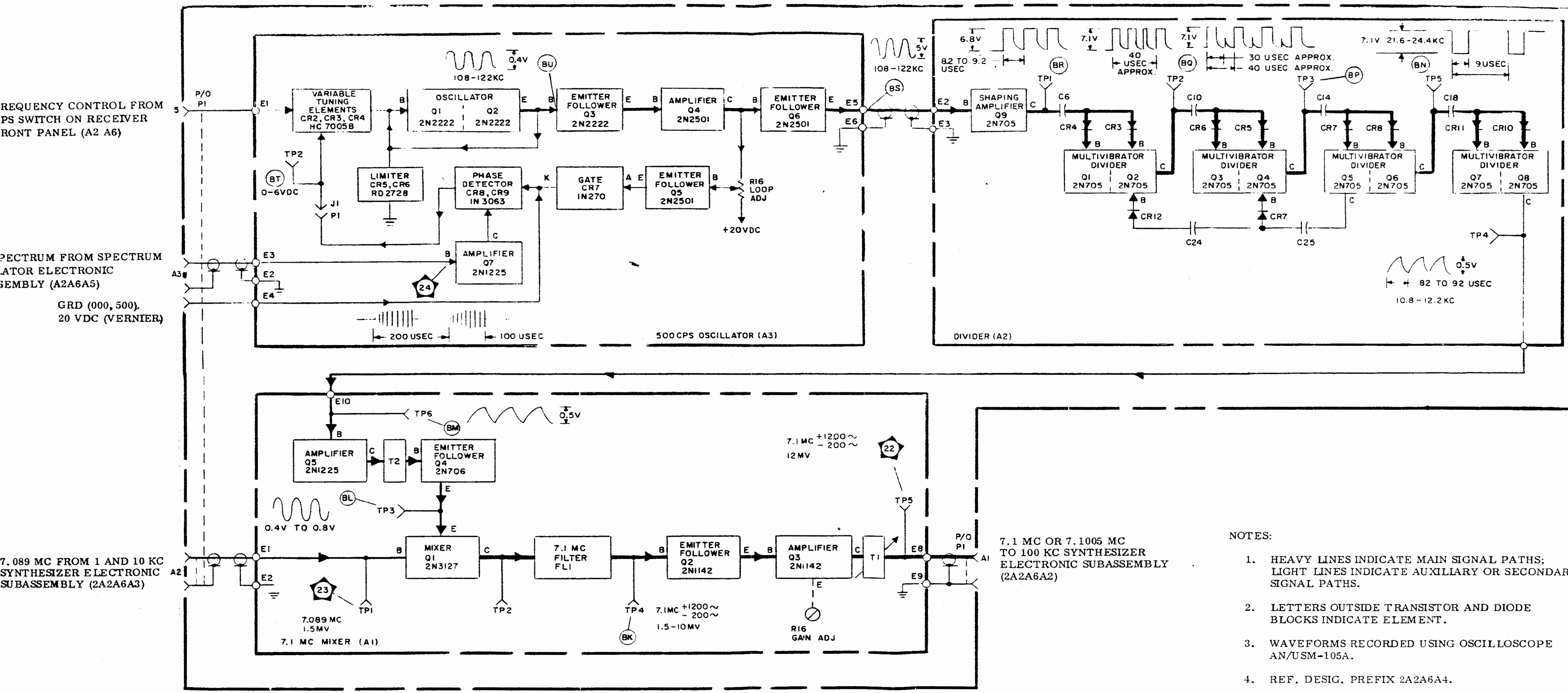


NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCK INDICATE ELEMENTS.
3. WAVEFORMS RECORDED USING OSCILLOSCOPE AN USM-105A.
4. REF. DESIG. PREFIX 2A6A5.

Figure 4-81. Spectrum Generator Electronic Subassembly, Servicing Block Diagram

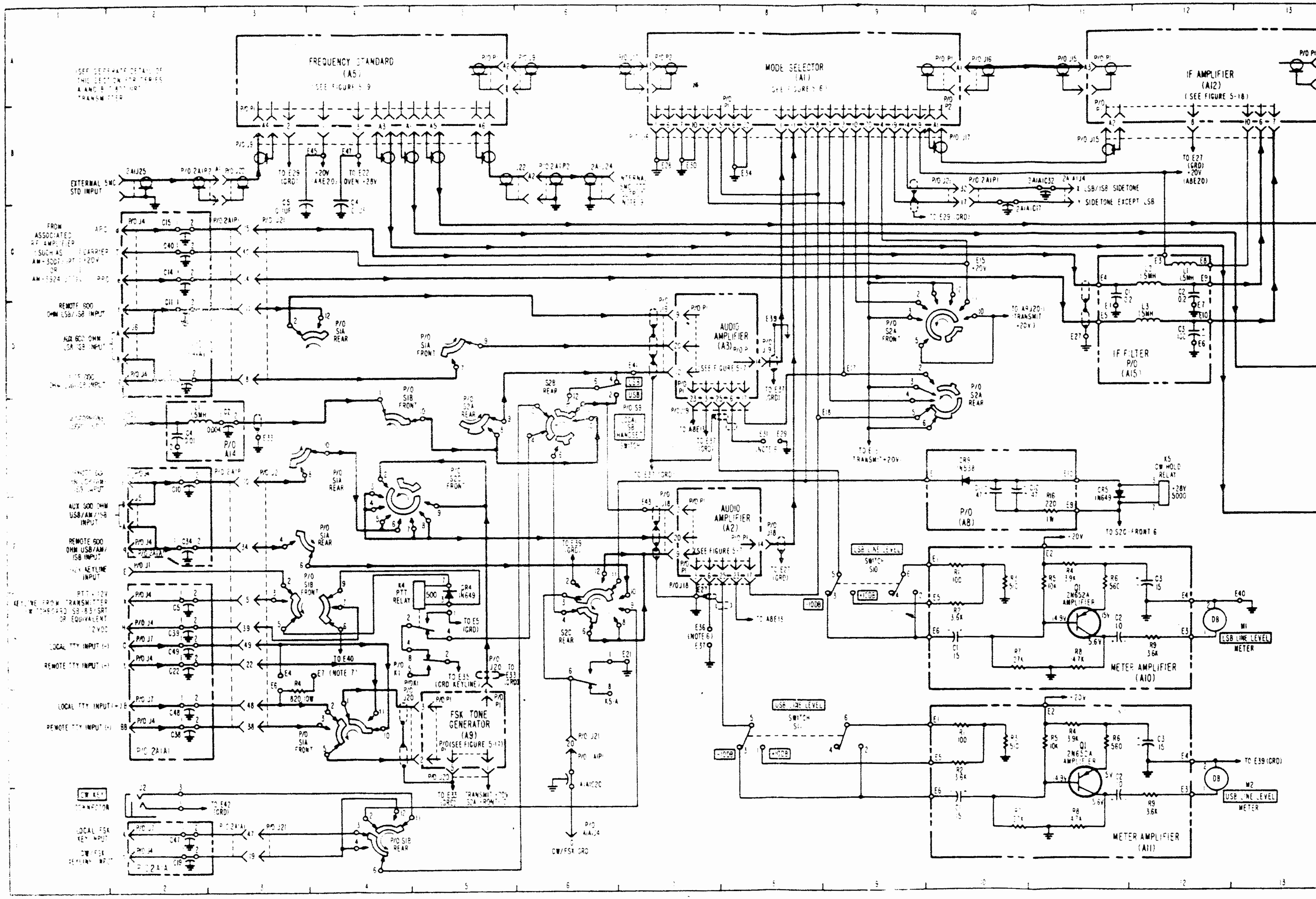

0.2V RMS 500 KC FROM
FREQUENCY STANDARD
ELECTRONIC ASSEMBLY
(A2A5)
2 USEC
9V
29
TP1
J3
L2
B
TRIGGER
AMPLIFIER
Q1
2N1301
C
C4
E6
E3
7.6V
BY
20 USEC
C4
MULTIVIBRATOR ÷ 2
Q1
2N1301
Q2
2N1301
E4
E3
BW
MULTIVIBRATOR ÷ 2
Q1
2N1301
Q2
2N1301
C
R9
R10
E4
E1
TP1
TP3
EMITTER
FOLLOWER
Q1
2N3127
E



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR AND DIODE BLOCKS INDICATE ELEMENT.
3. WAVEFORMS RECORDED USING OSCILLOSCOPE AN/USM-105A.
4. REF. DESIG. PREFIX 2A2A6A4.

Figure 4-82. 500 CPS Synthesizer Electronic Subassembly, Service Block Diagram



CAUTION

WHEN MAKING RESISTANCE CHECKS AT SEMI-CONDUCTOR DEVICES, USE ONLY THE HIGHER SCALES OF THE MULTIMETER SO AS TO AVOID UNINTENTIONAL DAMAGE TO THE SEMI-CONDUCTOR DEVICE DUE TO THE METERS INTERNAL VOLTAGE

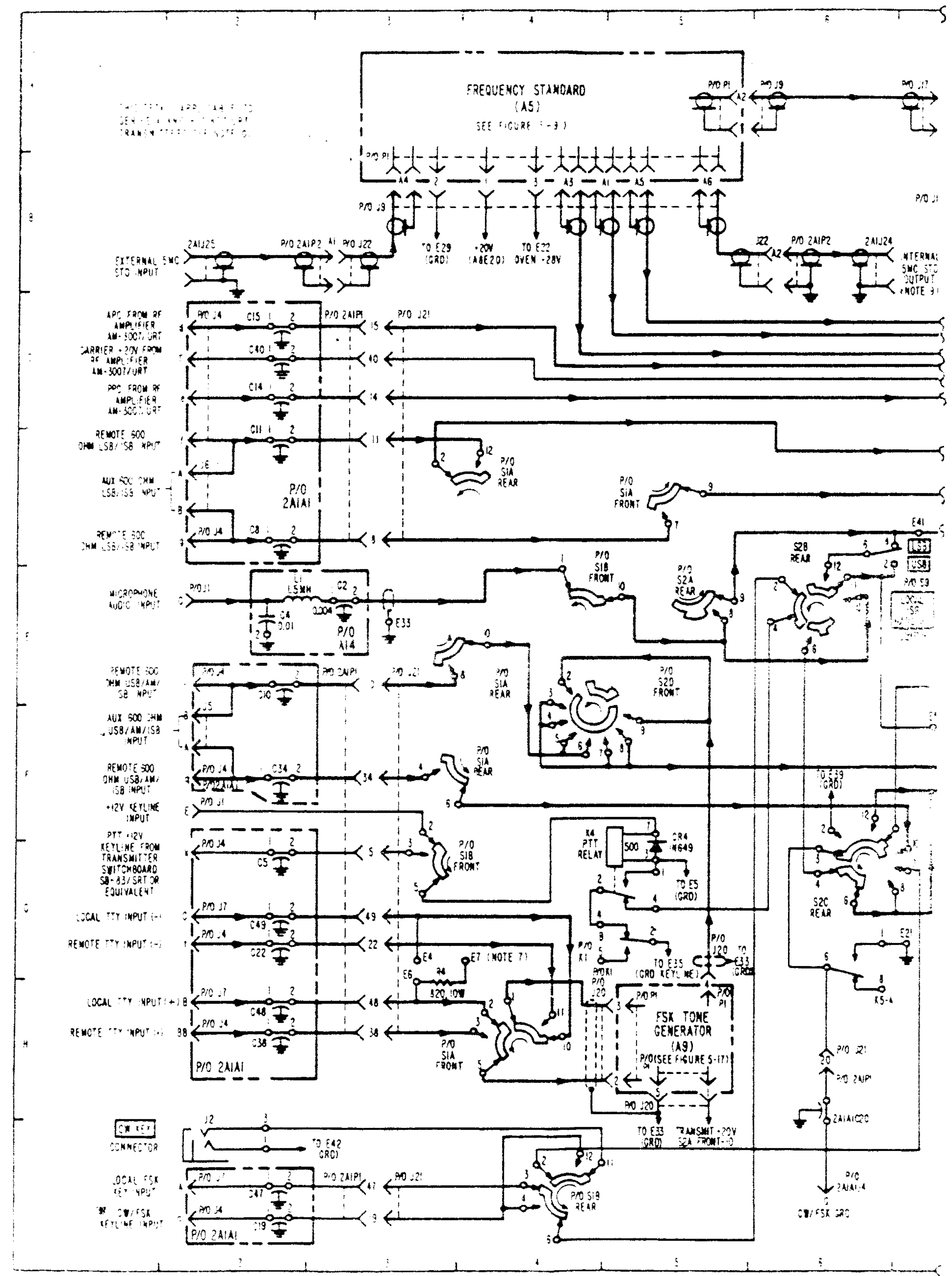
NOTES

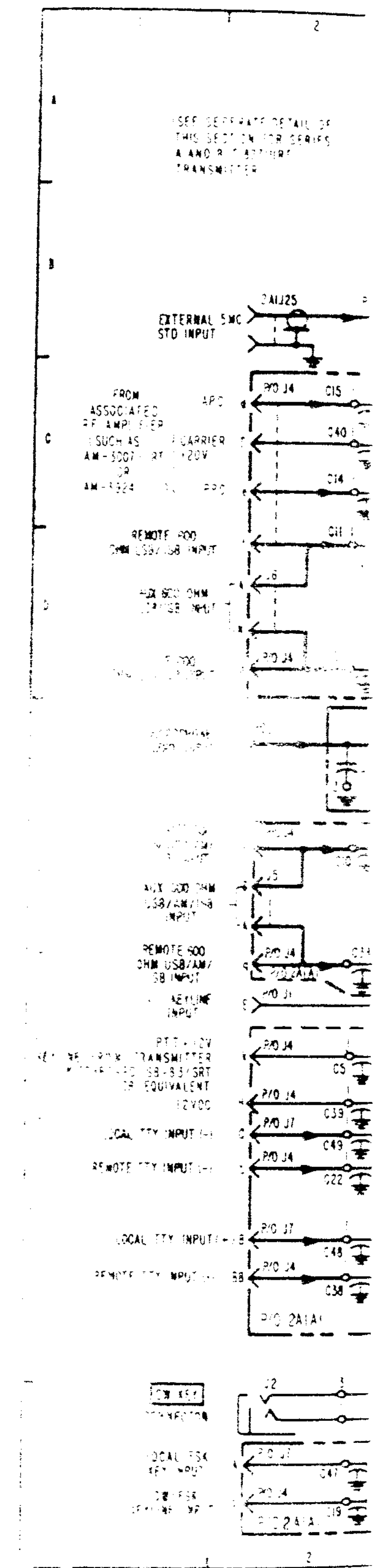
1. EXCEPT FOR CASE-MOUNTED ITEMS (BASIC PREFIX A1), PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH 2A2 AND APPROPRIATE BOARD NUMBER WHERE APPLICABLE.
2. UNLESS OTHERWISE SPECIFIED
   a. ALL RESISTANCE VALUES ARE IN OHMS K-INDICATES THOUSANDS OF OHMS
   b. ALL RESISTORS ARE 1/4 WATT, ± 5% TOL.
   c. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. NUMBERS ADJACENT TO WINDINGS AND COILS INDICATE DC RESISTANCE (VALUES LESS THAN ONE OHM ARE NOT SHOWN)
4. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4.
5. PINS L AND m OF J4 ARE USED TO PROVIDE ENERGIZING VOLTAGES FOR REMOTE OPERATION OF TRANSMIT/RECEIVE RELAY K3 AND PTT RELAY K4 WHEN THE ASSOCIATED AMPLIFIER USED WITH THE TRANSMITTER DOES NOT SUPPLY THESE VOLTAGES. THESE CONNECTIONS AND THE ONES ON PINS n, F, AND P ARE NOT USED. IF VOLTAGE IS REQUIRED ON PIN L IN THE REMOTE MODE OF OPERATION, JUMPER E11 TO E23.
6. TO CONNECT CENTER TAPS OF THE 600-OHM AUDIO TRANSFORMER WINDINGS TO GROUND, JUMPER E36 TO E37 AND E29 TO E31.
7. JUMPER E4 TO E7 IF NECESSARY FOR PROPER LOOP CURRENT ADJUSTMENT (5 TO 75MA) (LOCAL TTY OPERATION).
8. ▭ INDICATES EQUIPMENT OPERATION MARKING (FRONT PANEL CONTROL)
9. FREQUENCY STANDARD ELECTRONIC ASSEMBLY SWITCH S1 MUST BE SET AT COMPARE TO OBTAIN 5-MC STANDARD OUTPUT.
10. THIS DRAWING IS APPLICABLE TO T-827/URT TRANSMITTERS HAVING SERIAL NUMBERS PREFIXED WITH LETTERS A, B, AND C. THE MAIN SCHEMATIC SHOWS THE SERIES C CONFIGURATION. SERIES A AND B T-827/URT CIRCUITS HAVING SERIES C CHANGES ARE SHOWN IN THEIR ORIGINAL CONFIGURATION IN SEPARATE DETAILS WHERE REQUIRED.

Figure 5-5. Radio Transmitter T-827/URT, Chassis and Main Frame, Schematic Diagram (Sheet 1 of 2)

LOCATION INDEX

	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
	16I	A6P11	17B	A8C11	10F	A10R9	12G
ront)	4H, 5D	A6P12	16B	A8CR1	33C	A11C1	10I
ar)	3D, 3E, 3F	A6P13	15B	A8CR2	34C	A11C2	11I
ont)	3G, 4E	A6P14	15D	A8CR3	33C	A11C3	12H
ear)	4I, 30C	A6P15	15D	A8CR4	34C	A11Q1	11H
	19H	A6P16	15D	A8CR5	33D	A11R1	10H
ront)	10D, 32D	A6P17	15D	A8CR6	34D	A11R2	10H
ear)	5E, 10E	A6P18	15D	A8CR7	33D	A11R3	10H
ront)	31D	A6P19	15C	A8CR8	34D	A11R4	11H
ear)	6E	A6P21	14D	A8CR9	10E	A11R5	11H
ront)	32H	A6P22	14E	A8CR10	34G	A11R6	11H
ear)	6G	A6P23	14C	A9CR11	34F	A11R7	10I
ront)	4F	A6P24	14D	A9CR12	34F	A11R8	11I
ear)	21C	A6P25	14D	A8CR13	35F	A11R9	12I
	23F	A6P26	14E	A8Q1	34F	A12P1	11A, 11B, 12B,
	23F	A6A1P1	17E, 17F, 18F	A8Q2	34F		13A, 13B
nt)	22F	A6A2P1	16C, 17C	A8Q3	35F	A13DS3	36D
r)	21F	A6A3J1	15D	A8Q4	35F	A13DS4	37D
	16G	A6A3J3	15D	A8R1	35D	A14C1	32I
	30D	A6A3J4	15D	A8R2	33F	A14C2	3E
	31D	A6A3J5	15D	A8R3	34F	A14C3	33I
	32A	A6A3J6	15D	A8R4	35E	A14C4	2E
	9F	A6A3J7	15D	A8R5	35F	A14L1	2E
	8H	A6A4P1	16E	A8R6	35E	A15C1	11D
	33C	A6A5J1	14E	A8R7	35E	A15C2	12D
	7B, 10A	A6A5J2	14E	A8R8	35F	A15C3	12D
	7A, 8B,	A6A5J3	14D	A8R9	36E	A15L1	12C
	9B, 10B	A6A5J4	14D	A8R10	36F	A15L2	12C
	7F, 8F	A6A5J5	14D	A8R11	36F	A15L3	12D
	7D, 8D	A6A5J6	14D	A8R12	34F	A15R1	19D
	20B, 21B	A6A6J1	17B	A8R13	33G	A16R1	14G
	19A, 19B, 20B,	A6A6J2	16B	A8R14	33G	A16R2	15G
	21B, 22A, 22B	A6A6J3	15B	A8R15	34C	A16R3	14G
	3B, 4B, 5A, 5B	A6A6J4	17B	A8R16	11F		
	18C	A6A6J5	17B	A9J20	5G, 5H		
	16B	A6A6J6	16B	A9P1	5H		
	17E, 17F, 18F	A6A6J7	17B	A10C1	10G		
	16D, 16E	A7P8	20E, 20F, 21E,	A10C2	11G		
	16C, 16D, 17C		21F, 22E, 22F	A10C3	12F		
	13D, 13F, 14C,	A8C1	34D	A10Q1	11G		
	16F, 17F, 18C,	A8C2	34D	A10R1	10F		
	18D, 18E, 18F	A8C3	33E	A10R2	10G		
	14A, 15F, 18B	A8C4	34E	A10R3	10F		
	14B, 18A, 18B	A8C5	36E	A10R4	11F		
	16B	A8C6	36E	A10R5	11F		
	17B	A8C7	34G	A10R6	11F		
	17B	A8C8	34G	A10R7	10G		
	17B	A8C9	34C	A10R8	11G		
		A8C10	10F				





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PART LOCATION INDEX

REF DESIG	LOC
2A1J23	24A
2A1J24	6B
2A1J25	2B
2A1P1	3C, 3D, 3E, 3F, 3G, 3H, 3I, 6H, 10B, 10C, 22C, 22D, 22E, 30A, 30B, 30C, 30D, 30E, 30F, 30G, 30H, 35A, 35H, 35L, 36E
2A1P2	3B, 6B, 23A
2A1A1C1	29D
2A1A1C2	29D
2A1A1C3	36I
2A1A1C4	36E
2A1A1C5	2G
2A1A1C6	29H
2A1A1C7	29A
2A1A1C8	2D
2A1A1C9	29B
2A1A1C10	2E
2A1A1C11	2D
2A1A1C12	24C
2A1A1C13	29G
2A1A1C14	2C
2A1A1C15	2C
2A1A1C16	29C
2A1A1C17	10C
2A1A1C19	2I
2A1A1C20	6H
2A1A1C21	29A
2A1A1C22	2G
2A1A1C23	24E
2A1A1C24	36H
2A1A1C25	36I
2A1A1C26	24E
2A1A1C27	29H
2A1A1C28	24E
2A1A1C31	24D
2A1A1C32	11B
2A1A1C33	24D
2A1A1C34	2F
2A1A1C35	24D
2A1A1C36	29F

REF DESIG	LOC
2A1A1C37	36A
2A1A1C38	2H
2A1A1C39	2G
2A1A1C40	2C
2A1A1C41	29C
2A1A1C43	29E
2A1A1C44	29G
2A1A1C45	29C
2A1A1C46	29D
2A1A1C47	2I
2A1A1C48	2H
2A1A1C49	2G
2A1A1C50	29H
2A1A1J3	28D, 28H
2A1A1J4	2C, 2D, 2E, 2F, 2G, 2H, 2I, 6I, 11B, 24C, 24D, 24E, 28A, 28B, 28C, 28D, 28E, 28G, 28H, 37A, 37E, 37F, 37G, 37H,
A1A1J5	37I
A1A1J6	2F
A1A1J7	2D
C1	2G, 2H, 2I, 28I
C2	35C
C3	33F
C4	31I
C5	4B
CR1	3B
CR2	31E
CR3	20G
CR4	32C
CR5	5G
CR6	11F
CR7	32G
CR8	21C
CR9	32I
DS1	20G
DS2	32D
F1	32D
F2	32C
J1	2E, 2F, 37A, 37B, 37I
J2	2I
J5	13A
J8	20E, 20F, 21E, 21F, 22E, 22F
J9	3B, 4B, 5B

REF DESIG	LOC
J10	20B, 21B
J11	19A, 19B, 20B, 21B, 22A, 22B
J12	13D, 13F, 14C, 16F, 17F, 18C, 18D, 18E, 18F
J13	14A
J14	18A, 18B
J15	11A, 11B, 12B, 13B
J16	7B, 10A
J17	7A, 8B, 9B, 10B
J18	7F, 8F
J19	7D, 7E, 8D, 8E
J21	3C, 3D, 3E, 3F, 3G, 3H, 3I, 6H, 10B, 10C, 22C, 22D, 22E, 30A, 30B, 30C, 30D, 30F, 30G, 30H, 34A, 34H, 34I, 36E
J22	3B, 6B, 23A
K1	32E
K1A	32F
K1B	5G
K2	19G
K2A	19E
K2B	19G
K3	32C
K3 (A, B)	19C
K3C	31G
K3D	34C
K4	5F
K5	12F
K5A	6G
K6	32G
K6A	34I
L1	34C
L2	35D
M1	12G
M2	12H
Q1	33F
R1	35C
R2	36D
R3	31H
R4	3H

REF DESIG	LOC
S1	16I
S1A (Front)	4H, 5D
S1A (Rear)	3D, 3E, 3F
S1B (Front)	3G, 4E
S1B (Rear)	4I, 30C
S2	19H
S2A (Front)	10D, 32D
S2A (Rear)	5E, 10E
S2B (Front)	31D
S2B (Rear)	6E
S2C (Front)	32H
S2C (Rear)	6G
S2D (Front)	4F
S2D (Rear)	21C
S3	23F
S4	23F
S5 (Front)	22F
S5 (Rear)	21F
S6	16G
S7	30D
S8	31D
S9	32A
S10	9F
S11	3H
T1	33C
A1P1	7B, 10A
A1P2	7A, 8B, 9B, 10B
A2P1	7F, 8F
A3P1	7D, 8D
A4P1	20B, 21B
A4P2	19A, 19B, 20B, 21B, 22A, 22B
A5P1	3B, 4B, 5A, 5B
A6C1	18C
A6C2	16B
A6J4	17E, 17F, 18F
A6J5	16D, 16E
A6J6	16C, 16D, 17C
A6P1	13D, 13F, 14C, 16F, 17F, 18C, 18D, 18E, 18F
A6P2	14A, 15F, 18B
A6P3	14B, 18A, 18B
A6P7	16B
A6P8	17B
A6P9	17B
A6P10	17B

REF DESIG
A6P11
A6P12
A6P13
A6P14
A6P15
A6P16
A6P17
A6P18
A6P19
A6P21
A6P22
A6P23
A6P24
A6P25
A6P26
A6A1P1
A6A2P1
A6A3J1
A6A3J3
A6A3J4
A6A3J5
A6A3J6
A6A3J7
A6A4P1
A6A5J1
A6A5J2
A6A5J3
A6A5J4
A6A5J5
A6A5J6
A6A6J1
A6A6J2
A6A6J3
A6A6J4
A6A6J5
A6A6J6
A6A6J7
A7P8
A8C1
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A8C9
A8C10

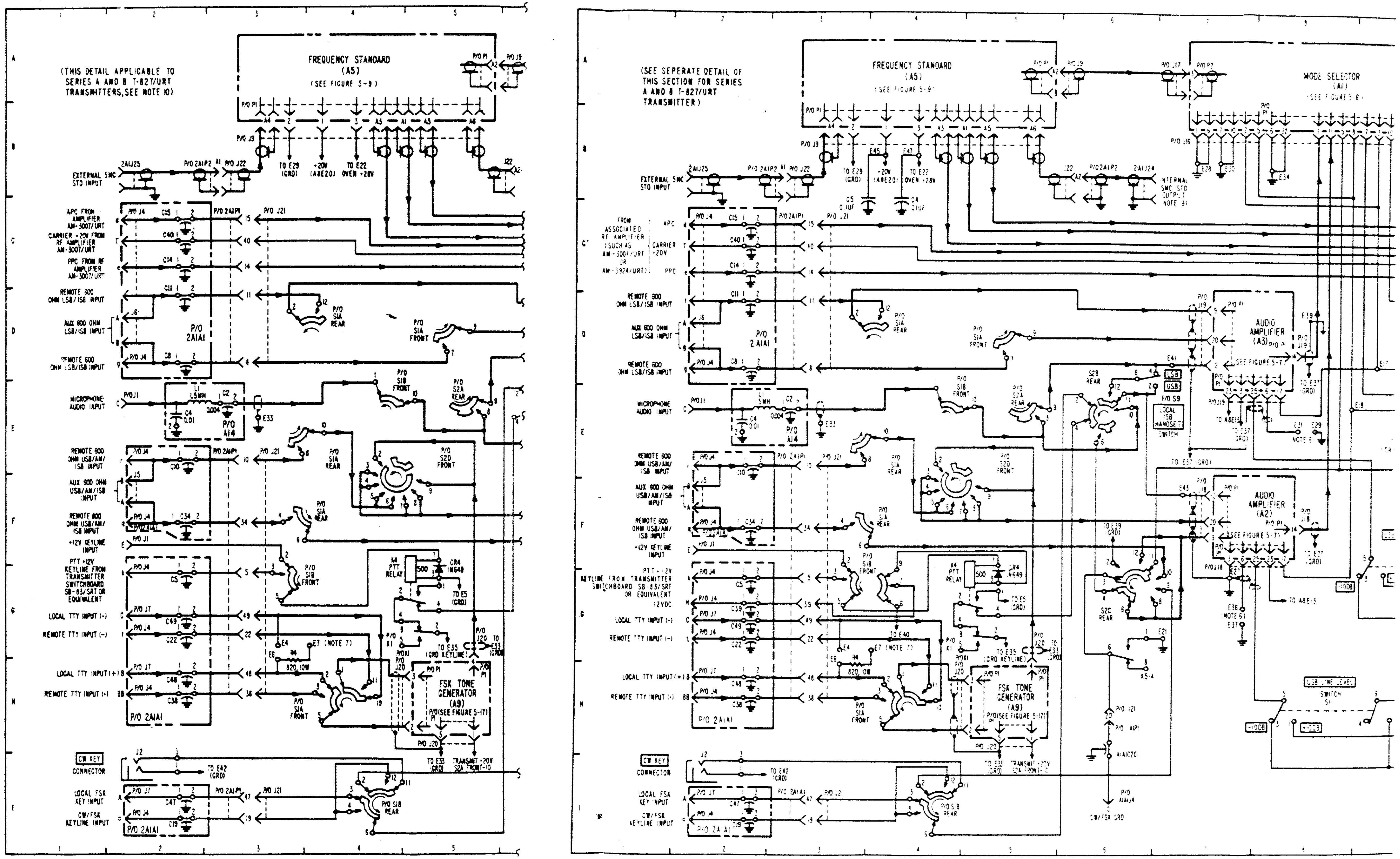
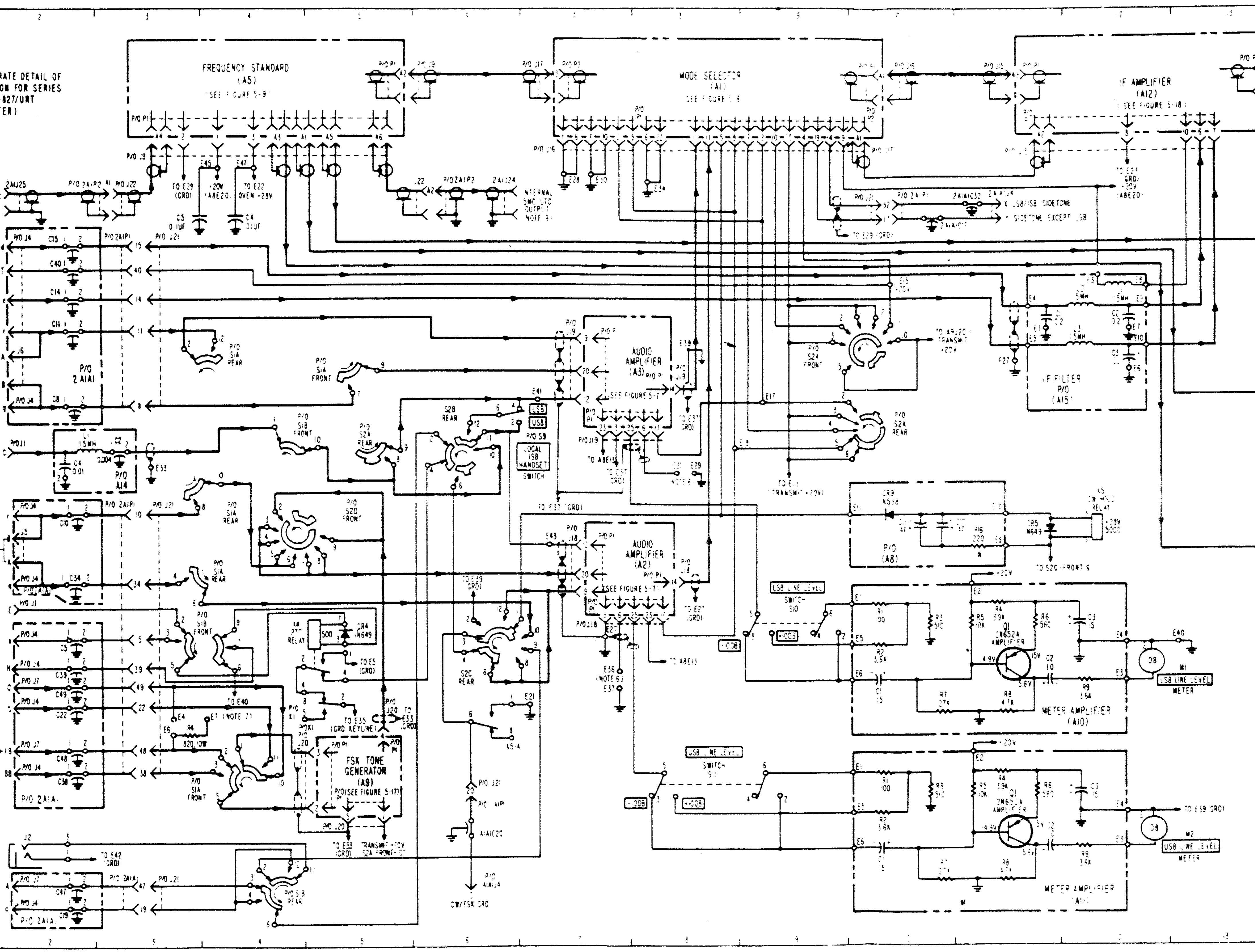


Figure 5-5. Radio Transmitter T-827/URT, Chassis and Main Frame, Schematic Diagram (Sheet 1 of 2)



CAUTION

WHEN MAKING RESISTANCE CHECKS AT SEMI-CONDUCTOR DEVICES, USE ONLY THE HIGHER SCALES OF THE MULTIMETER SO AS TO AVOID UNINTENTIONAL DAMAGE TO THE SEMI-CONDUCTOR DEVICE DUE TO THE METERS INTERNAL VOLTAGE

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH 2A2 UNLESS OTHERWISE SPECIFIED.
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTANCE VALUES ARE IN OHMS K- INDICATES THOUSANDS OF OHMS
   b. ALL RESISTORS ARE 1/4 WATT, ±5% TOL.
   c. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. NUMBERS ADJACENT TO WINDINGS AND COILS INDICATE DC RESISTANCE (VALUES LESS THAN ONE OHM ARE NOT SHOWN)
4. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4
5. PINS L AND m OF J4 ARE USED TO PROVIDE ENERGIZING VOLTAGES FOR REMOTE OPERATION OF TRANSMIT/RECEIVE RELAY K3 AND PTT RELAY K4 WHEN THE ASSOCIATED AMPLIFIER USED WITH THE TRANSMITTER DOES NOT SUPPLY THESE VOLTAGES. THESE CONNECTIONS AND THE ONES ON PINS n, F, AND P ARE NOT USED IN THE AN/WRC-1. IF VOLTAGE IS REQUIRED ON PIN L IN THE REMOTE MODE OF OPERATION, JUMPER E11 TO E23
6. TO CONNECT CENTER TAPS OF THE 600-OHM AUDIO TRANSFORMER WINDINGS TO GROUND, JUMPER E36, TO E37 AND E29 TO E31.
7. JUMPER E4 TO E7 IF NECESSARY FOR PROPER LOOP CURRENT ADJUSTMENT (5 TO 75MA) (LOCAL TTY OPERATION)
8. [box] INDICATES EQUIPMENT OPERATION MARKING (FRONT PANEL CONTROL)
9. FREQUENCY STANDARD ELECTRONIC ASSEMBLY SWITCH S1 MUST BE SET AT COMPARE TO OBTAIN 5-MC STANDARD OUTPUT
10. THIS DRAWING IS APPLICABLE TO T-827/URT TRANSMITTERS HAVING SERIAL NUMBERS PREFIXED WITH LETTERS A, B, AND C. THE MAIN SCHEMATIC SHOWS THE SERIES C CONFIGURATION. SERIES A AND B T-827/URT CIRCUITS HAVING SERIES C CHANGES ARE SHOWN IN THEIR ORIGINAL CONFIGURATION IN SEPARATE DETAILS WHERE REQUIRED

REF DESIG	LOC
2A1J23	24A
2A1J24	6B
2A1J25	2B
2A1P1	3C, 3D
	3F, 3C
	3I, 6H
	10C, 2
	22D, 2
	30A, 3
	30C, 3
	30E, 3
	30G, 3
	35A, 3
	35L, 3
2A1P2	3B, 6
2A1A1C1	29D
2A1A1C2	29D
2A1A1C3	36I
2A1A1C4	36E
2A1A1C5	2G
2A1A1C6	29H
2A1A1C7	29A
2A1A1C8	2D
2A1A1C9	29B
2A1A1C10	2E
2A1A1C11	2D
2A1A1C12	24C
2A1A1C13	29G
2A1A1C14	2C
2A1A1C15	2C
2A1A1C16	29C
2A1A1C17	10C
2A1A1C19	2I
2A1A1C20	6H
2A1A1C21	29A
2A1A1C22	2G
2A1A1C23	24E
2A1A1C24	36H
2A1A1C25	36I
2A1A1C26	24E
2A1A1C27	29H
2A1A1C28	24E
2A1A1C31	24D
2A1A1C32	11B
2A1A1C33	24D
2A1A1C34	2F
2A1A1C35	24D
2A1A1C36	29F

PART LOCATION INDEX

REF DESIG	LOC
2A1J23	24A
2A1J24	6B
2A1J25	2B
2A1P1	3C, 3D, 3E, 3F, 3G, 3H, 3I, 6H, 10B, 10C, 22C, 22D, 22E, 30A, 30B, 30C, 30D, 30E, 30F, 30G, 30H, 35A, 35H, 35L, 36E
2A1P2	3B, 6B, 23A
2A1A1C1	29D
2A1A1C2	29D
2A1A1C3	36I
2A1A1C4	36E
2A1A1C5	2G
2A1A1C6	29H
2A1A1C7	29A
2A1A1C8	2D
2A1A1C9	29B
2A1A1C10	2E
2A1A1C11	2D
2A1A1C12	24C
2A1A1C13	29G
2A1A1C14	2C
2A1A1C15	2C
2A1A1C16	29C
2A1A1C17	10C
2A1A1C19	2I
2A1A1C20	6H
2A1A1C21	29A
2A1A1C22	2G
2A1A1C23	24E
2A1A1C24	36H
2A1A1C25	36I
2A1A1C26	24E
2A1A1C27	29H
2A1A1C28	24E
2A1A1C31	24D
2A1A1C32	11B
2A1A1C33	24D
2A1A1C34	2F
2A1A1C35	24D
2A1A1C36	29F
2A1A1C37	36A
2A1A1C38	2H
2A1A1C39	2G
2A1A1C40	2C
2A1A1C41	29C
2A1A1C43	29E
2A1A1C44	29G
2A1A1C45	29C
2A1A1C46	29D
2A1A1C47	2I
2A1A1C48	2H
2A1A1C49	2G
2A1A1C50	29H
2A1A1J3	28D, 28H
2A1A1J4	2C, 2D, 2E, 2F, 2G, 2H, 2I, 6I, 11B, 24C, 24D, 24E, 28A, 28B, 28C, 28D, 28E, 28G, 28H, 37A, 37E, 37F, 37G, 37H,
A1A1J5	37I
A1A1J6	2F
A1A1J7	2D
C1	2G, 2H, 2I, 28I
C2	35C
C3	33F
C4	31I
C5	4B
CR1	3B
CR2	31E
CR3	20G
CR4	32C
CR5	5G
CR6	11F
CR7	32G
CR8	21C
CR9	32I
DS1	20G
DS2	32D
F1	32D
F2	32C
J1	2E, 2F, 37A, 37B, 37I
J2	2I
J5	13A
J8	20E, 20F, 21E, 21F, 22E, 22F
J9	3B, 4B, 5B
J10	20B, 21B
J11	19A, 19B, 20B, 21B, 22A, 22B
J12	13D, 13F, 14C, 16F, 17F, 18C, 18D, 18E, 18F
J13	14A
J14	18A, 18B
J15	11A, 11B, 12B, 13B
J16	7B, 10A
J17	7A, 8B, 9B, 10B
J18	7F, 8F
J19	7D, 7E, 8D, 8E
J21	3C, 3D, 3E, 3F, 3G, 3H, 3I, 6H, 10B, 10C, 22C, 22D, 22E, 30A, 30B, 30C, 30D, 30F, 30G, 30H, 34A, 34H, 34I, 36E
J22	3B, 6B, 23A
K1	32E
K1A	32F
K1B	5G
K2	19G
K2A	19E
K2B	19G
K3	32C
K3 (A, B)	19C
K3C	31G
K3D	34C
K4	5F
K5	12F
K5A	6G
K6	32G
K6A	34I
L1	34C
L2	35D
M1	12G
M2	12H
Q1	33F
R1	35C
R2	36D
R3	31H
R4	3H
S1	16I
S1A (Front)	4H, 5D
S1A (Rear)	3D, 3E, 3F
S1B (Front)	3G, 4E
S1B (Rear)	4I, 30C
S2	19H
S2A (Front)	10D, 32D
S2A (Rear)	5E, 10E
S2B (Front)	31D
S2B (Rear)	6E
S2C (Front)	32H
S2C (Rear)	6G
S2D (Front)	4F
S2D (Rear)	21C
S3	23F
S4	23F
S5 (Front)	22F
S5 (Rear)	21F
S6	16G
S7	30D
S8	31D
S9	32A
S10	9F
S11	8H
T1	33C
A1P1	7B, 10A
A1P2	7A, 8B, 9B, 10B
A2P1	7F, 8F
A3P1	7D, 8D
A4P1	20B, 21B
A4P2	19A, 19B, 20B, 21B, 22A, 22B
A5P1	3B, 4B, 5A, 5B
A6C1	18C
A6C2	16B
A6J4	17E, 17F, 18F
A6J5	16D, 16E
A6J6	16C, 16D, 17C
A6P1	13D, 13F, 14C, 16F, 17F, 18C, 18D, 18E, 18F
A6P2	14A, 15F, 18B
A6P3	14B, 18A, 18B
A6P7	16B
A6P8	17B
A6P9	17B
A6P10	17B
A6P11	17B
A6P12	16B
A6P13	15B
A6P14	15D
A6P15	15D
A6P16	15D
A6P17	15D
A6P18	15D
A6P19	15C
A6P21	14D
A6P22	14E
A6P23	14C
A6P24	14D
A6P25	14D
A6P26	14E
A6A1P1	17E, 17F, 18F
A6A2P1	16C, 17C
A6A3J1	15D
A6A3J3	15D
A6A3J4	15D
A6A3J5	15D
A6A3J6	15D
A6A3J7	15D
A6A4P1	16E
A6A5J1	14E
A6A5J2	14E
A6A5J3	14D
A6A5J4	14D
A6A5J5	14D
A6A5J6	14D
A6A6J1	17B
A6A6J2	16B
A6A6J3	15B
A6A6J4	17B
A6A6J5	17B
A6A6J6	16B
A6A6J7	17B
A7P8	20E, 20F, 21E, 21F, 22E, 22F
A8C1	34D
A8C2	34D
A8C3	33E
A8C4	34E
A8C5	36E
A8C6	36E
A8C7	34G
A8C8	34G
A8C9	34C
A8C10	10F
A8C11	10F
A8CR1	33C
A8CR2	34C
A8CR3	33C
A8CR4	34C
A8CR5	33D
A8CR6	34D
A8CR7	33D
A8CR8	34D
A8CR9	10E
A8CR10	34G
A9CR11	34F
A9CR12	34F
A8CR13	35F
A8Q1	34F
A8Q2	34F
A8Q3	35F
A8Q4	35F
A8R1	35D
A8R2	33F
A8R3	34F
A8R4	35E
A8R5	35F
A8R6	35E
A8R7	35E
A8R8	35F
A8R9	36E
A8R10	36F
A8R11	36F
A8R12	34F
A8R13	33G
A8R14	33G
A8R15	34C
A8R16	11F
A9J20	5G, 5H
A9P1	5H
A10C1	10G
A10C2	11G
A10C3	12F
A10Q1	11G
A10R1	10F
A10R2	10G
A10R3	10F
A10R4	11F
A10R5	11F
A10R6	11F
A10R7	10G
A10R8	11G
A10R9	12G
A11C1	10I
A11C2	11I
A11C3	12H
A11Q1	11H
A11R1	10H
A11R2	10H
A11R3	10H
A11R4	11H
A11R5	11H
A11R6	11H
A11R7	10I
A11R8	11I
A11R9	12I
A12P1	11A, 11B, 12B, 13A, 13B
A13DS3	36D
A13DS4	37D
A14C1	32I
A14C2	3E
A14C3	33I
A14C4	2E
A14L1	2E
A15C1	11D
A15C2	12D
A15C3	12D
A15L1	12C
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A15R1	19D
A16R1	14G
A16R2	15G
A16R3	14G

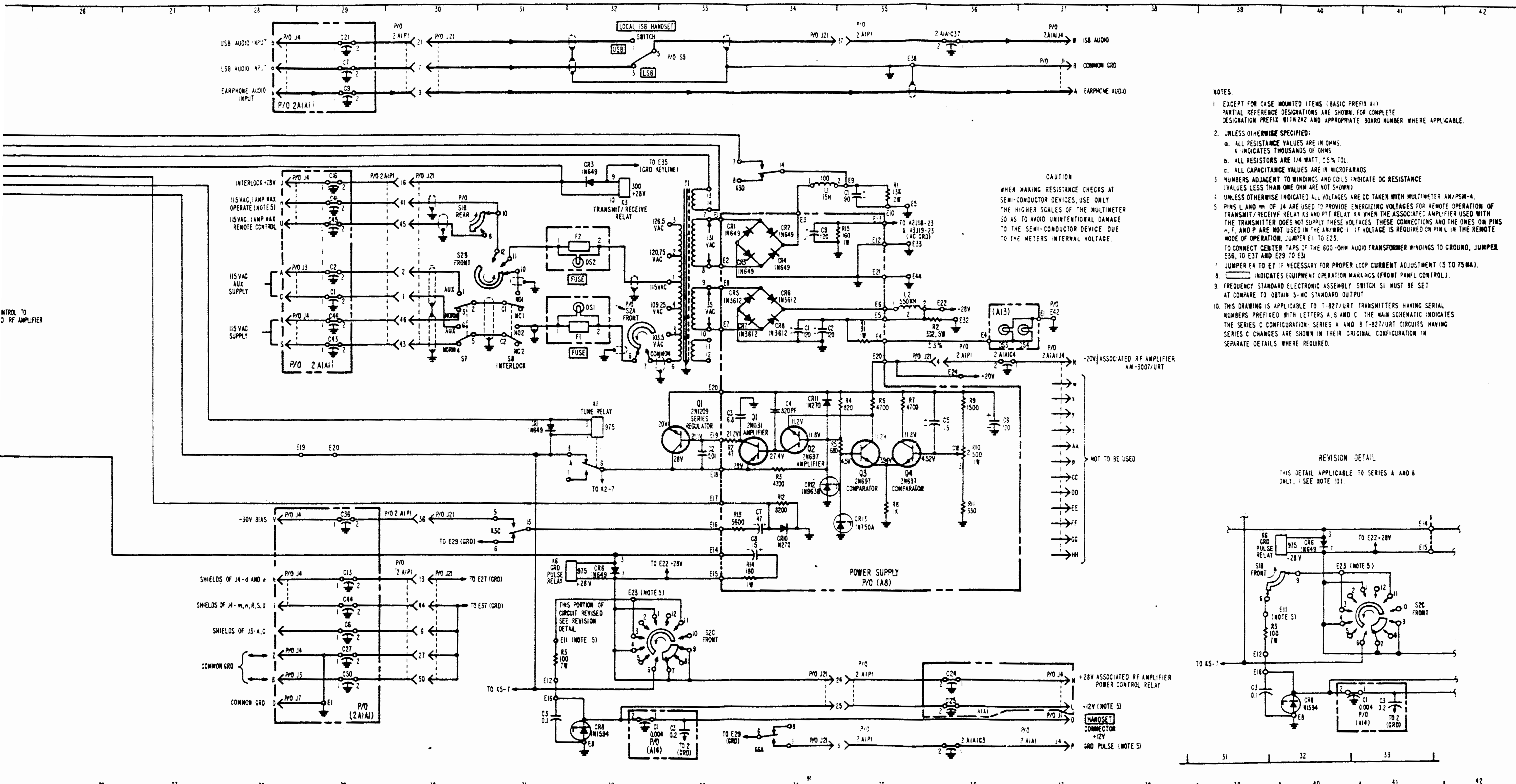
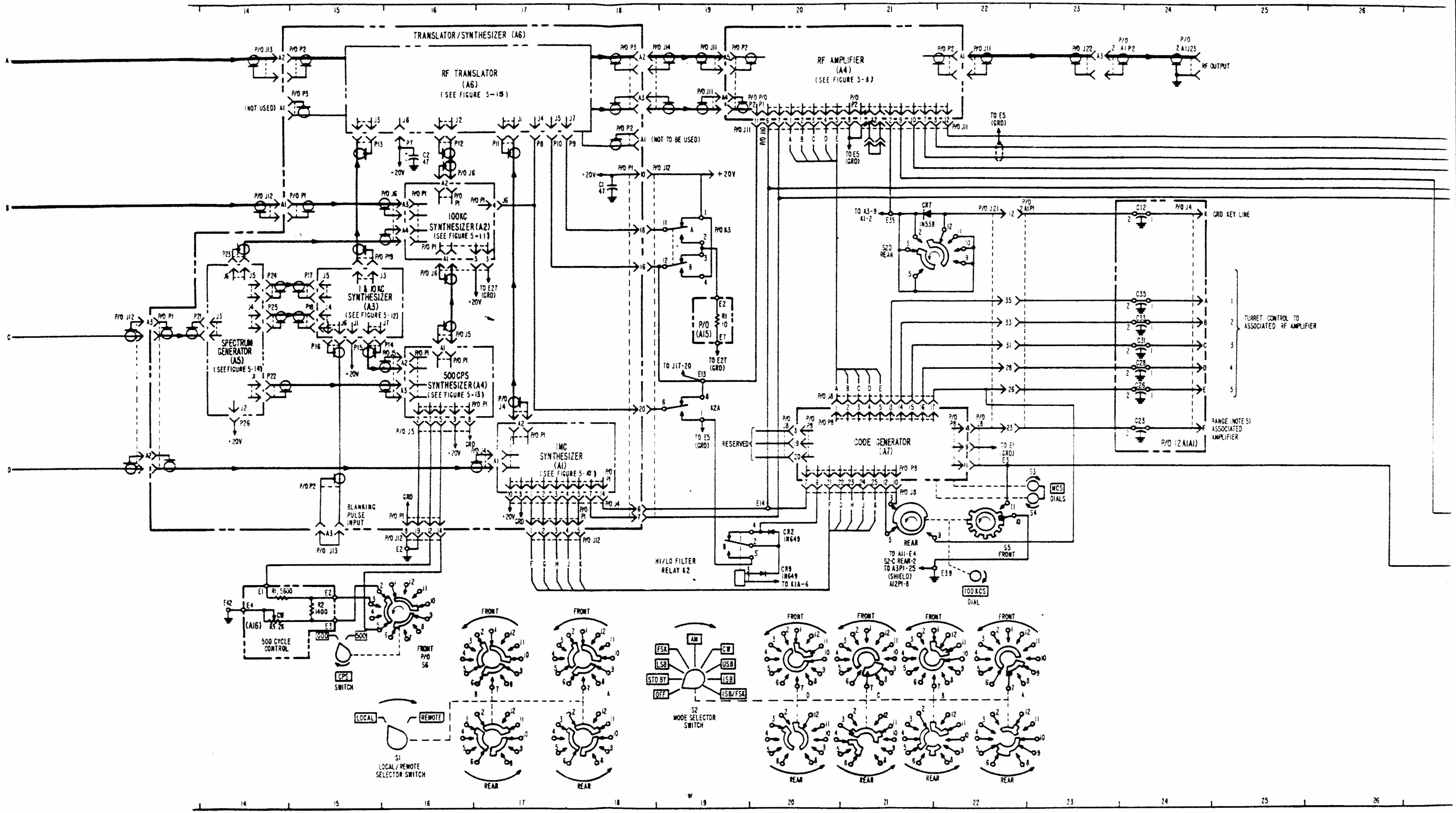
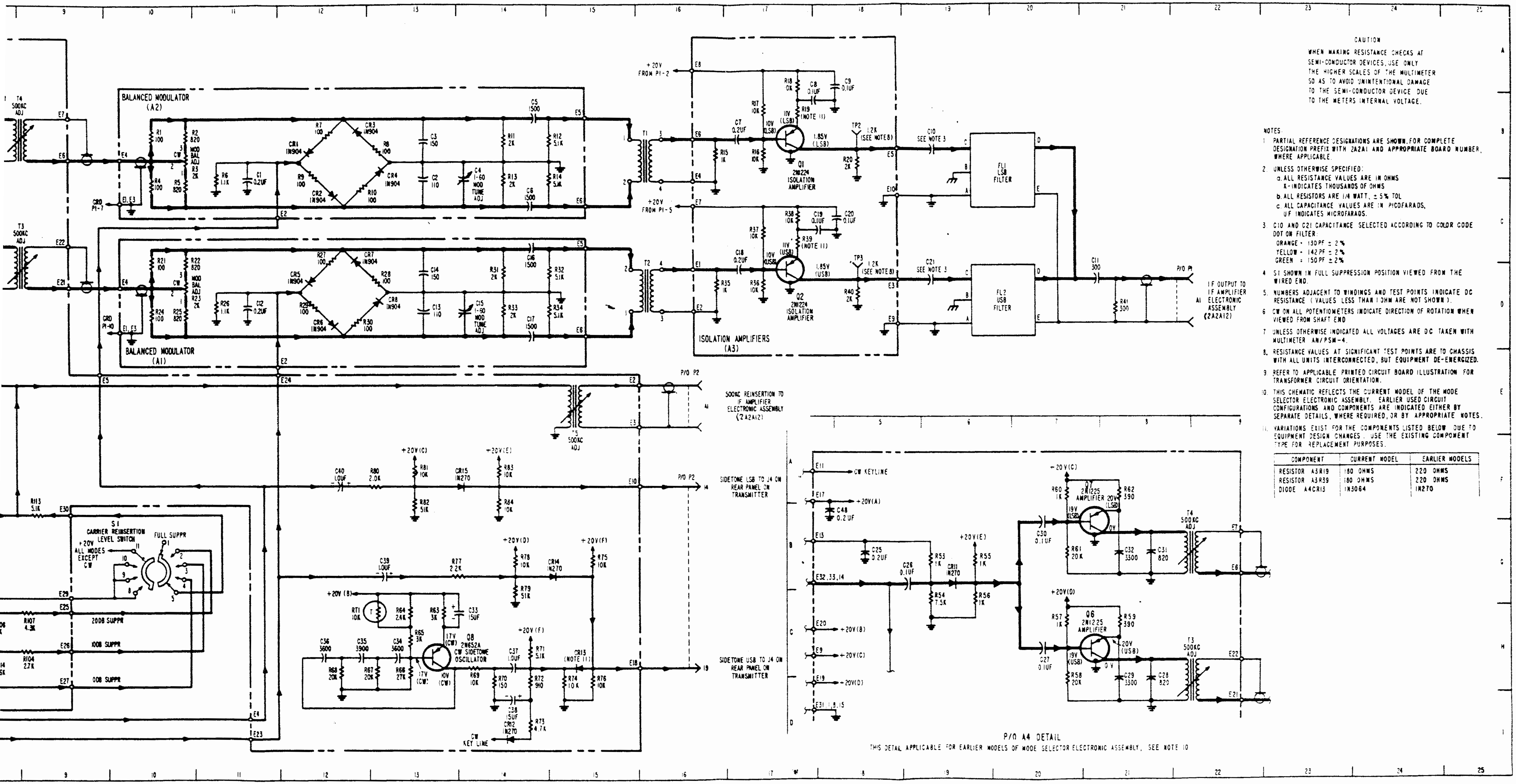


Figure 5-5. Radio Transmitter T-827/URT, Chassis and Main Frame, Schematic Diagram (Sheet 2 of 2)


TRANSLATOR/SYNTHESIZER (A6)
RF TRANSLATOR
(A6)
(SEE FIGURE 5-15)
RF AMPLIFIER
(A4)
(SEE FIGURE 5-8)
RF OUTPUT
100KC
SYNTHESIZER (A2)
(SEE FIGURE 5-11)
1 & 10 KC
SYNTHESIZER
(A3)
(SEE FIGURE 5-12)
SPECTRUM
GENERATOR
(A5)
(SEE FIGURE 5-14)
500CPS
SYNTHESIZER (A4)
(SEE FIGURE 5-13)
1MC
SYNTHESIZER
(A1)
(SEE FIGURE 5-10)
CODE GENERATOR
(A7)
GRD KEY LINE
TURRET CONTROL TO
ASSOCIATED RF AMPLIFIER
RANGE (NOTE 5)
ASSOCIATED
AMPLIFIER
HI/LO FILTER
RELAY K2
BLANKING
PULSE
INPUT
500 CYCLE
CONTROL
CPS
SWITCH
LOCAL
REMOTE
S1
LOCAL/REMOTE
SELECTOR SWITCH
FSK
LSB
STD BY
OFF
AM
CW
USB
LSB/FSK
S2
MODE SELECTOR
SWITCH
MCS
DIALS
100 KCS
DIAL
FRONT
REAR
RESERVED



CAUTION

WHEN MAKING RESISTANCE CHECKS AT SEMI-CONDUCTOR DEVICES, USE ONLY THE HIGHER SCALES OF THE MULTIMETER SO AS TO AVOID UNINTENTIONAL DAMAGE TO THE SEMI-CONDUCTOR DEVICE DUE TO THE METERS INTERNAL VOLTAGE.

NOTES:

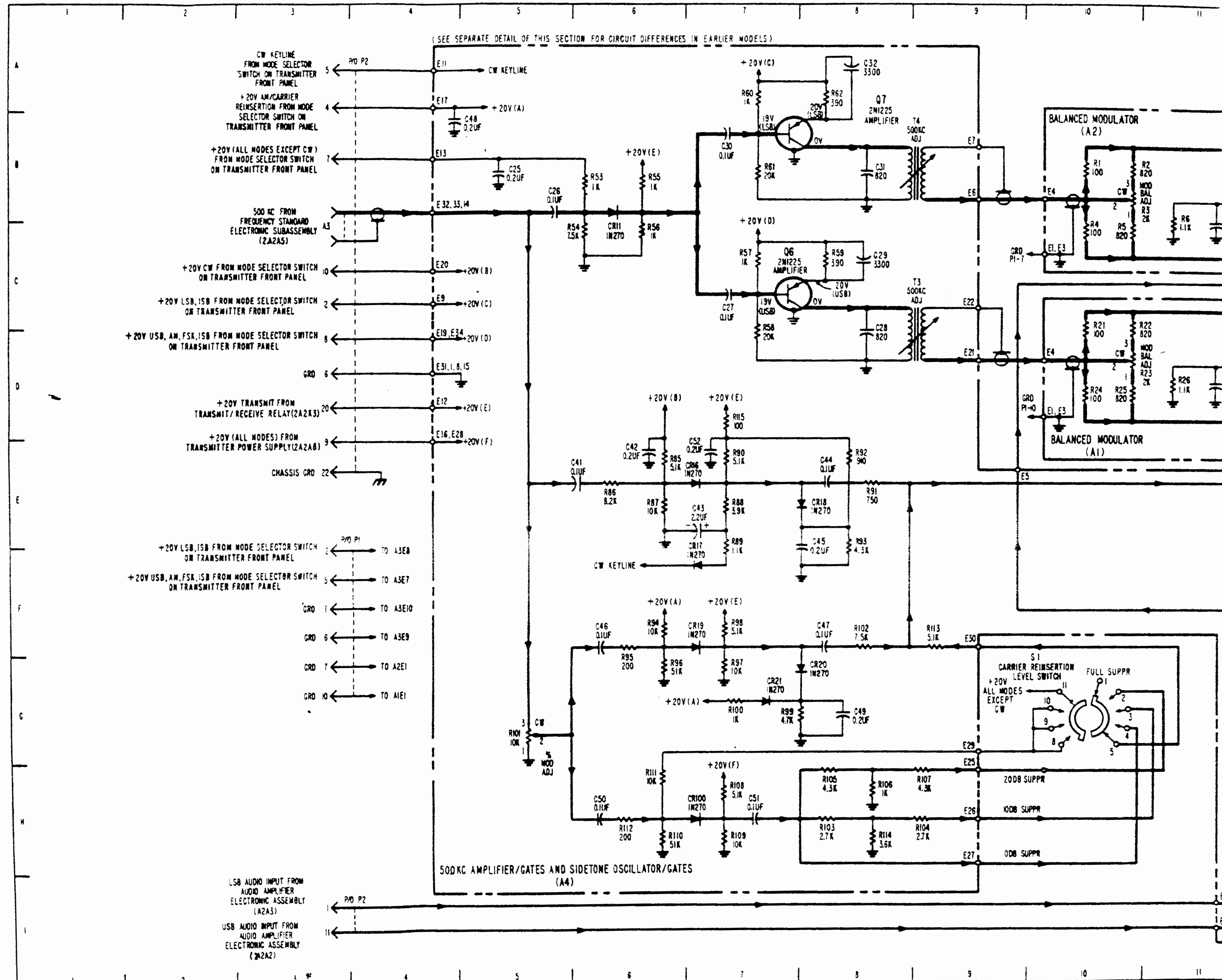
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 2A2A1 AND APPROPRIATE BOARD NUMBER, WHERE APPLICABLE.
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTANCE VALUES ARE IN OHMS K-INDICATES THOUSANDS OF OHMS
   b. ALL RESISTORS ARE 1/4 WATT, ± 5% TOL
   c. ALL CAPACITANCE VALUES ARE IN PICOFARADS, UF INDICATES MICROFARADS.
3. C10 AND C21 CAPACITANCE SELECTED ACCORDING TO COLOR CODE DOT ON FILTER:
   ORANGE - 130PF ± 2%
   YELLOW - 142PF ± 2%
   GREEN : 150PF ± 2%
4. S1 SHOWN IN FULL SUPPRESSION POSITION VIEWED FROM THE WIRED END.
5. NUMBERS ADJACENT TO WINDINGS AND TEST POINTS INDICATE DC RESISTANCE (VALUES LESS THAN 1 OHM ARE NOT SHOWN).
6. CW ON ALL POTENTIOMETERS INDICATE DIRECTION OF ROTATION WHEN VIEWED FROM SHAFT END
7. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4.
8. RESISTANCE VALUES AT SIGNIFICANT TEST POINTS ARE TO CHASSIS WITH ALL UNITS INTERCONNECTED, BUT EQUIPMENT DE-ENERGIZED.
9. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATION FOR TRANSFORMER CIRCUIT ORIENTATION.
10. THIS CHEMATIC REFLECTS THE CURRENT MODEL OF THE MODE SELECTOR ELECTRONIC ASSEMBLY. EARLIER USED CIRCUIT CONFIGURATIONS AND COMPONENTS ARE INDICATED EITHER BY SEPARATE DETAILS, WHERE REQUIRED, OR BY APPROPRIATE NOTES.
11. VARIATIONS EXIST FOR THE COMPONENTS LISTED BELOW DUE TO EQUIPMENT DESIGN CHANGES. USE THE EXISTING COMPONENT TYPE FOR REPLACEMENT PURPOSES.

COMPONENT	CURRENT MODEL	EARLIER MODELS
RESISTOR A3R19	180 OHMS	220 OHMS
RESISTOR A3R39	180 OHMS	220 OHMS
DIODE A4CR13	1N3064	1N270

Figure 5-6. Transmitter Mode Selector Electronic Assembly, Schematic Diagram

PART LOCATION INDEX

LOC	REF DESIG	LOC	REF DESIG	LOC
10B	A4C38	14I	A4R71	14H
10B	A4C39	13G	A4R72	14H
10C	A4C40	12F	A4R73	14I
10C	A4C41	6E	A4R74	15H
11B	A4C42	6E	A4R75	15G
12B	A4C43	7E	A4R76	15H
13B	A4C44	8E	A4R77	13G
12B	A4C45	8E	A4R78	14G
12C	A4C46	6F	A4R79	14G
14B	A4C47	8F	A4R80	13F
15B	A4C48	4B	A4R81	13F
14B	A4C49	8G	A4R82	13F
15B	A4C50	6H	A4R83	14F
17B	A4C51	7H	A4R84	14F
18B	A4C52	7E	A4R85	6E
18A	A4CR11	6B	A4R86	6E
17D	A4CR12	14I	A4R87	6E
18C	A4CR13	15H	A4R88	7E
18C	A4CR14	15G	A4R89	7E
17B	A4CR15	14F	A4R90	7E
17D	A4CR16	7E	A4R91	8E
16B	A4CR17	7F	A4R92	8E
17B	A4CR18	8E	A4R93	8E
17B	A4CR19	7F	A4R94	6F
17A	A4CR20	8G	A4R95	6F
17B	A4CR21	7G	A4R96	6G
18B	A4CR100	7H	A4R97	7G
16D	A4Q6	7C	A4R98	7F
17D	A4Q7	7B	A4R99	8G
17C	A4Q8	13H	A4R100	7G
17C	A4R53	6B	A4R101	5G
17C	A4R54	6C	A4R102	8F
18D	A4R55	6B	A4R103	8H
18B	A4R56	6C	A4R104	9H
18D	A4R57	7C	A4R105	8H
5B	A4R58	7D	A4R106	8H
5B	A4R59	8C	A4R107	9H
7C	A4R60	7A	A4R108	7H
8C	A4R61	7B	A4R109	7H
8C	A4R62	8A	A4R110	6H
7B	A4R63	13H	A4R111	6H
8B	A4R64	13H	A4R112	6H
8A	A4R65	13H	A4R113	9F
14H	A4R66	13H	A4R114	8H
13H	A4R67	13H	A4R115	7D
12H	A4R68	12H	A4RT1	13H
12H	A4R69	14H	A4RT3	9C, 9D
14H	A4R70	14H	A4T3	9D
			A4T4	9B
			A4T5	15E



PART LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG
C10	19B	A2R2	10B	A4C38
C11	21D	A2R3	10B	A4C39
C21	19D	A2R4	10C	A4C40
FL1	20B	A2R5	10C	A4C41
FL2	20D	A2R6	11B	A4C42
P1	3F, 3G, 16E	A2R7	12B	A4C43
P2	3A, 3B, 3C,	A2R8	13B	A4C44
	3D, 3E, 3I	A2R9	12B	A4C45
	16F, 16H, 22D	A2R10	12C	A4C46
R41	21D	A2R11	14B	A4C47
S1	10G	A2R12	15B	A4C48
T1	16B	A2R13	14B	A4C49
T2	16D	A2R14	15B	A4C50
A1C12	11D	A3C7	17B	A4C51
A1C13	13D	A3C8	18B	A4C52
A1C14	13D	A3C9	18A	A4CR11
A1C15	14D	A3C18	17D	A4CR12
A1C16	14C	A3C19	18C	A4CR13
A1C17	14D	A3C20	18C	A4CR14
A1CR5	12D	A3Q1	17B	A4CR15
A1CR6	12D	A3Q2	17D	A4CR16
A1CR7	12C	A3R15	16B	A4CR17
A1CR8	13D	A3R16	17B	A4CR18
A1R21	10C	A3R17	17B	A4CR19
A1R22	10C	A3R18	17A	A4CR20
A1R23	10D	A3R19	17B	A4CR21
A1R24	10D	A3R20	18B	A4CR100
A1R25	10D	A3R35	16D	A4Q6
A1R26	11D	A3R36	17D	A4Q7
A1R27	12C	A3R37	17C	A4Q8
A1R28	13D	A3R38	17C	A4R53
A1R29	12D	A3R39	17C	A4R54
A1R30	12D	A3R40	18D	A4R55
A1R31	14D	A3TP2	18B	A4R56
A1R32	15D	A3TP3	18D	A4R57
A1R33	14D	A4C25	5B	A4R58
A1R34	15D	A4C26	5B	A4R59
A2C1	11C	A4C27	7C	A4R60
A2C2	13B	A4C28	8C	A4R61
A2C3	13B	A4C29	8C	A4R62
A2C4	14B	A4C30	7B	A4R63
A2C5	14B	A4C31	8B	A4R64
A2C6	14C	A4C32	8A	A4R65
A2CR1	12B	A4C33	14H	A4R66
A2CR2	12C	A4C34	13H	A4R67
A2CR3	12B	A4C35	12H	A4R68
A2CR4	13B	A4C36	12H	A4R69
A2R1	10B	A4C37	14H	A4R70

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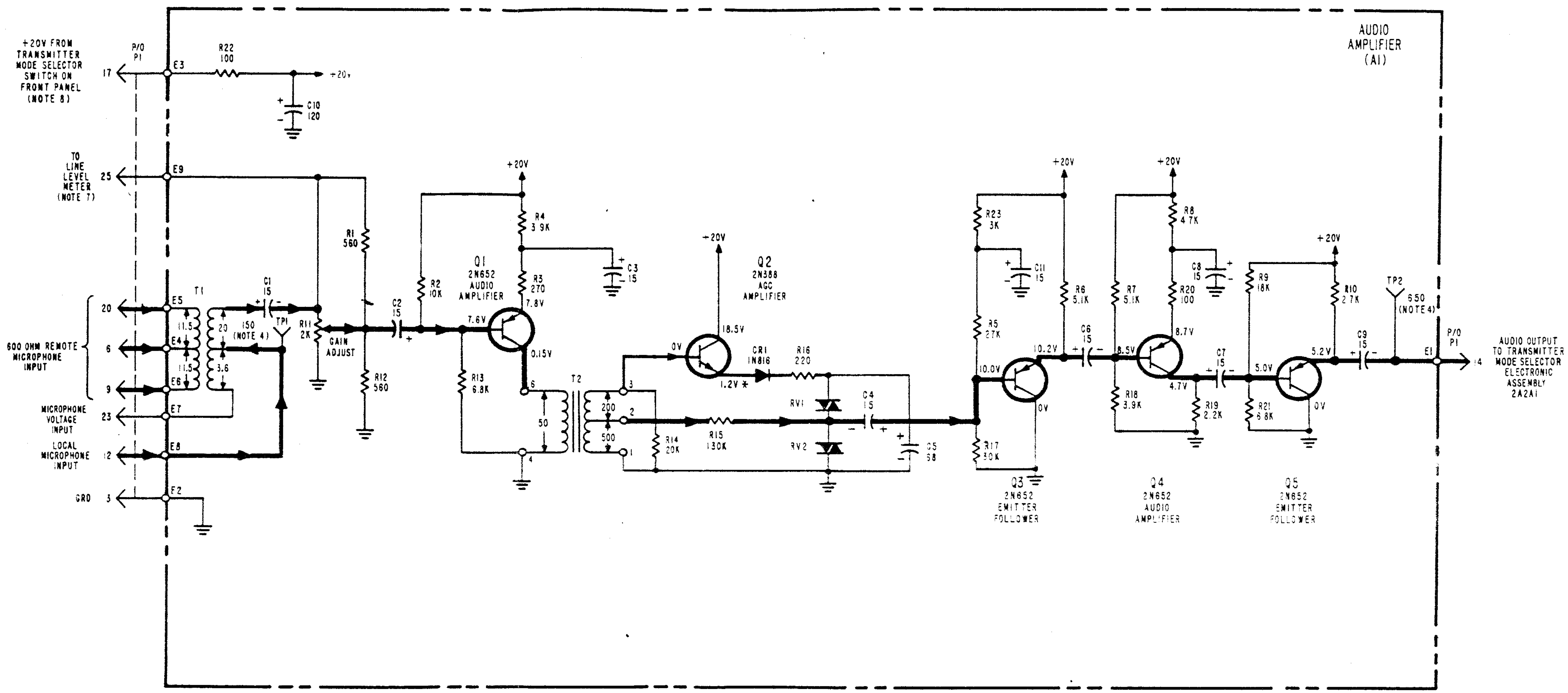
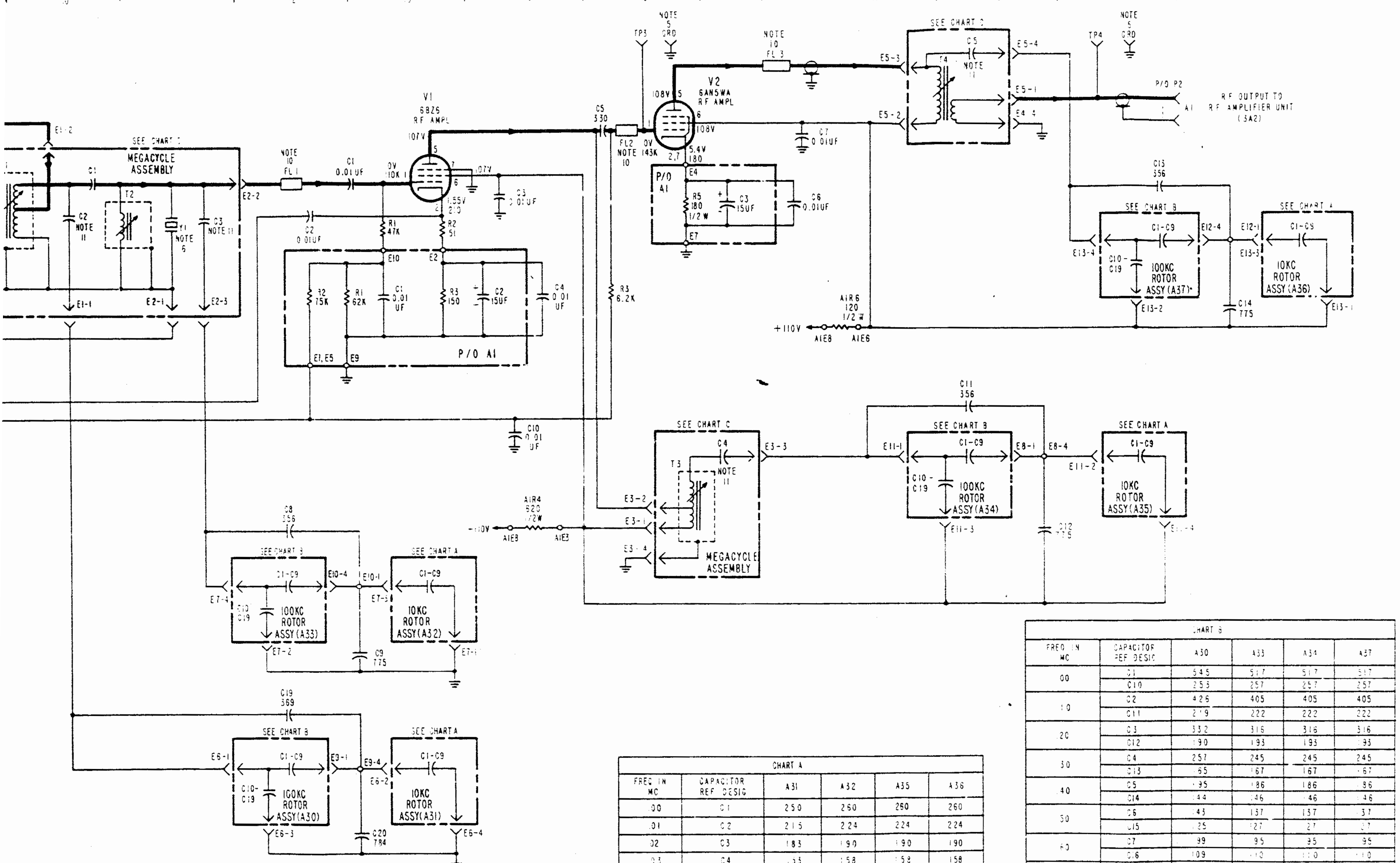


NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 2A2A2 OR 2A2A3
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTANCE VALUES ARE IN OHMS. K-INDICATES THOUSANDS OF OHMS
   b. ALL RESISTORS ARE 1/4 WATT, ± 5% TOLERENCE
   c. ALL CAPACITANCE VALUES ARE IN MICROFARADS
3. NUMBERS ADJACENT TO WINDINGS AND TEST POINTS INDICATE DC RESISTANCE (VALUES LESS THAN ONE OHM ARE NOT SHOWN).
4. RESISTANCE VALUES AT SIGNIFICANT TEST POINTS ARE TO CHASSIS WITH ALL UNITS INTERCONNECTED BUT EQUIPMENT DE-ENERGIZED.
5. * EMITTER VOLTAGE VARIES WITH INPUT. A READING OF 1.2V OBTAINED WITH A 55MV INPUT AT PINS 12 AND 23.
6. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC, TAKEN WITH MULTIMETER AN/PSM-4
7. DURING LSB OPERATION THE AUDIO LEVEL AT P1-25 IS OBSERVED ON THE LSB LINE LEVEL METER (M1) DURING USB OPERATION THE AUDIO LEVEL AT P1-25 IS OBSERVED ON THE USB LINE LEVEL METER (M2).
8. DURING LSB OPERATION +20V LSB/ISB IS PRESENT AT P1-17 DURING USB OPERATION +20V USB/AM/FSK/ISB IS PRESENT AT P1-17
9. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATION FOR TRANSFORMER CIRCUIT ORIENTATION.

Figure 5-7. Transmitter Audio Amplifier Electronic Assembly, Schematic Diagram



NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 2A2A4.
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTANCE VALUES ARE IN OHMS. K = INDICATES THOUSANDS OF OHMS.
   b. ALL RESISTORS ARE 1/4 WATT, ±5% TOL.
   c. ALL CAPACITANCE VALUES ARE IN PICOFARADS. UF INDICATES MICROFARADS.
3. NUMBERS ADJACENT TO COILS AND TEST POINTS INDICATE DC RESISTANCE. VALUES LESS THAN ONE OHM ARE NOT SHOWN.
4. ALL RESISTANCE READINGS TAKEN WITH RF AMPLIFIER ELECTRONIC ASSEMBLY REMOVED FROM CHASSIS AND REFERENCED TO GROUND.
5. DURING MEASUREMENT AT A TEST POINT USE GROUND MARKED ADJACENT TO TEST POINT.
6. CRYSTAL Y1 USED ONLY ON ASSEMBLIES A9, A10 AND A19.
7. S1 SHOWN IN 2MC POSITION.
8. P2-A2 IS WIRED BUT NOT USED IN AN/WRC-1 SYSTEM.
9. CAPACITORS IN CHARTS A, B, AND C WHICH ARE 100PF AND GREATER ARE 1/2%. CAPACITORS LESS THAN 100PF ARE 1%, EXCEPT C1 IN CHART C WHICH IS 5%.
10. FL1, FL2, AND FL3 ARE PARASITIC SUPPRESSORS.
11. NOT USED IN 2MC POSITION.
12. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC, TAKEN WITH MULTIMETER AN/PSM-4.
13. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATION FOR TRANSFORMER CIRCUIT ORIENTATION.
14. VALUE OF A38C5 IS 0.0022UF ON UNIT SER NO. 111 AND ABOVE.

CHART A

FREQ IN MC	CAPACITOR REF DESIG	A31	A32	A35	A36
.00	C1	250	260	260	260
.01	C2	215	224	224	224
.02	C3	183	190	190	190
.03	C4	153	158	158	158
.04	C5	124	128	128	128
.05	C6	96	99	99	99
.06	C7	70	72	72	72
.07	C8	45	47	47	47
.08	C9	22	23	23	23
.09	—	—	—	—	—

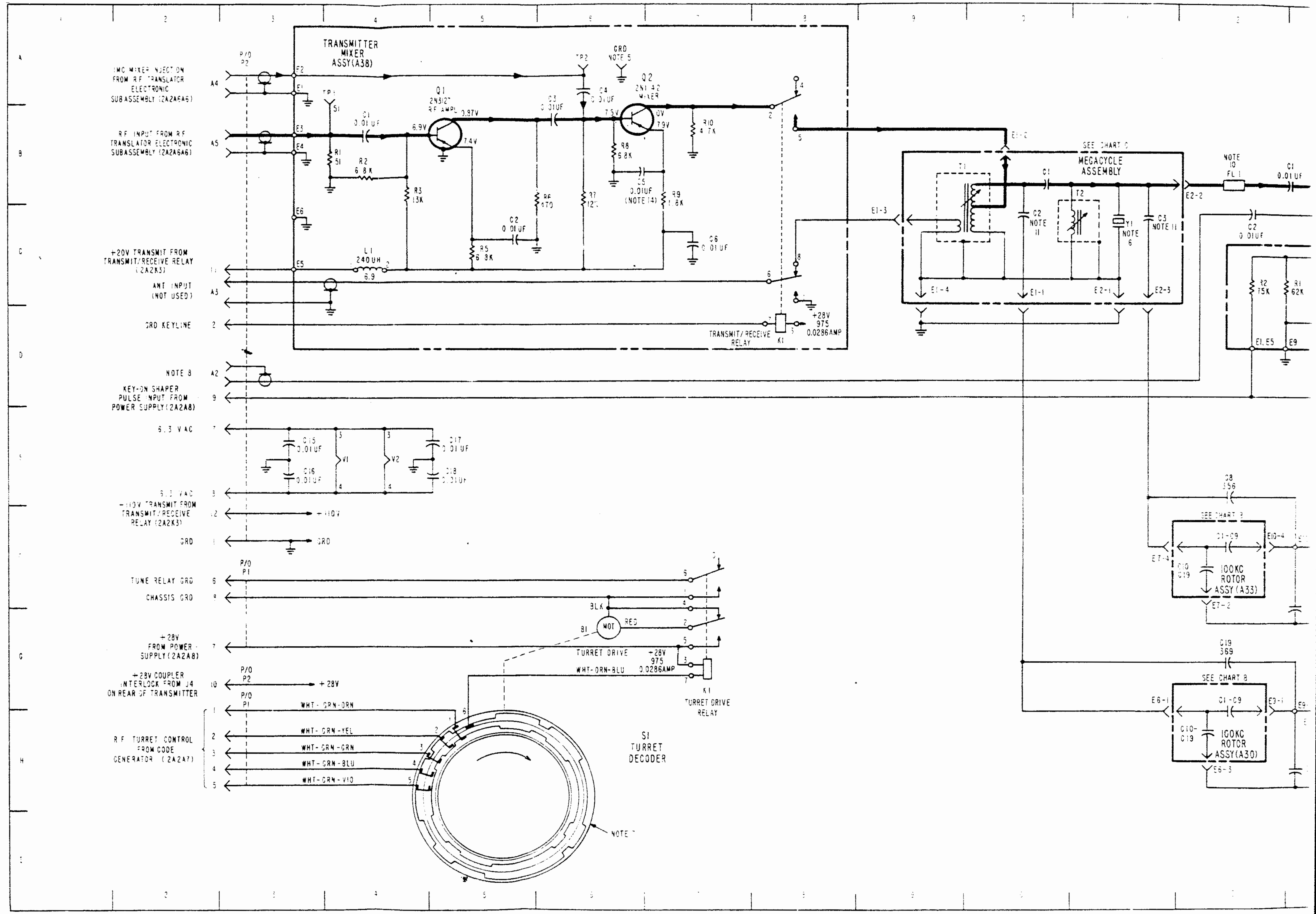
CHART B

FREQ IN MC	CAPACITOR REF DESIG	A30	A33	A34	A37
.00	C1	545	517	517	517
	C10	253	257	257	257
.10	C2	426	405	405	405
	C11	219	222	222	222
.20	C3	332	316	316	316
	C12	190	193	193	193
.30	C4	257	245	245	245
	C13	165	167	167	167
.40	C5	195	186	186	186
	C14	144	146	146	146
.50	C6	143	137	137	137
	C15	125	127	127	127
.60	C7	99	95	95	95
	C16	109	110	110	110
.70	C8	61	59	59	59
	C17	95	96	96	96
.80	C9	29	28	28	28
	C18	83	83	83	83
.90	C19	74	74	74	74

CHART C

FREQ IN MC	ON ASSY	C1	ON ASSY	C2	ON ASSY	C3	ON ASSY	C4	ON ASSY	C5
2	A20	9	A20	SHORT	A20	SHORT	A25	SHORT	A2	SHORT
3	A21	52	A21	1247	A21	1253	A26	1247	A3	253
4	A22	[illegible]	A22	623	A22	629	A27	623	A4	629
5	A23	[illegible]	A23	416	A23	422	A28	416	A5	422
6	A24	[illegible]	A24	312	A24	318	A29	312	A6	318
7	A25	[illegible]	A25	250	A25	256	A2	250	A7	256
8	A26	[illegible]	A26	208	A26	214	A3	208	A8	214
9	A27	[illegible]	A27	179	A27	185	A4	179	A9	185
10	A28	27	A28	157	A28	163	A5	[illegible]	A10	[illegible]
11	A29	24	A29	140	A29	146	A6	140	A11	146
12	A2	[illegible]	A2	126	A2	132	A7	126	A12	132
13	A3	[illegible]	A3	[illegible]	A3	120	A8	[illegible]	A13	120
14	A4	20	A4	105	A4	[illegible]	A9	105	A14	[illegible]
15	A5	[illegible]	A5	97	A5	103	A10	97	A15	103
16	A6	[illegible]	A6	91	A6	96	[illegible]	[illegible]	A16	96
17	A7	[illegible]	A7	85	A7	90	A12	85	A17	90
18	A8	[illegible]	A8	80	A8	85	A13	80	A18	85
19	A9	[illegible]	A9	75	A9	80	A14	75	A19	80
20	A10	[illegible]	A10	[illegible]	A10	76	A15	[illegible]	A20	76
21	A11	[illegible]	A11	67	A11	73	A16	67	A21	73
22	A12	[illegible]	A12	[illegible]	A12	68	A17	64	A22	68
23	A13	[illegible]	A13	61	A13	66	A18	[illegible]	A23	66
24	A14	[illegible]	A14	58	A14	63	A19	[illegible]	A24	63
25	A15	[illegible]	A15	56	A15	[illegible]	A20	[illegible]	A25	[illegible]
26	A16	[illegible]	A16	54	A16	59	[illegible]	[illegible]	A26	59
27	A17	[illegible]	A17	[illegible]	A17	[illegible]	A22	[illegible]	A27	[illegible]
28	A18	[illegible]	A18	[illegible]	A18	55	A23	[illegible]	A28	55
29	A19	[illegible]	A19	[illegible]	A19	[illegible]	A24	[illegible]	A29	[illegible]

Figure 5-8. RF Amplifier Electronic Assembly, Schematic Diagram



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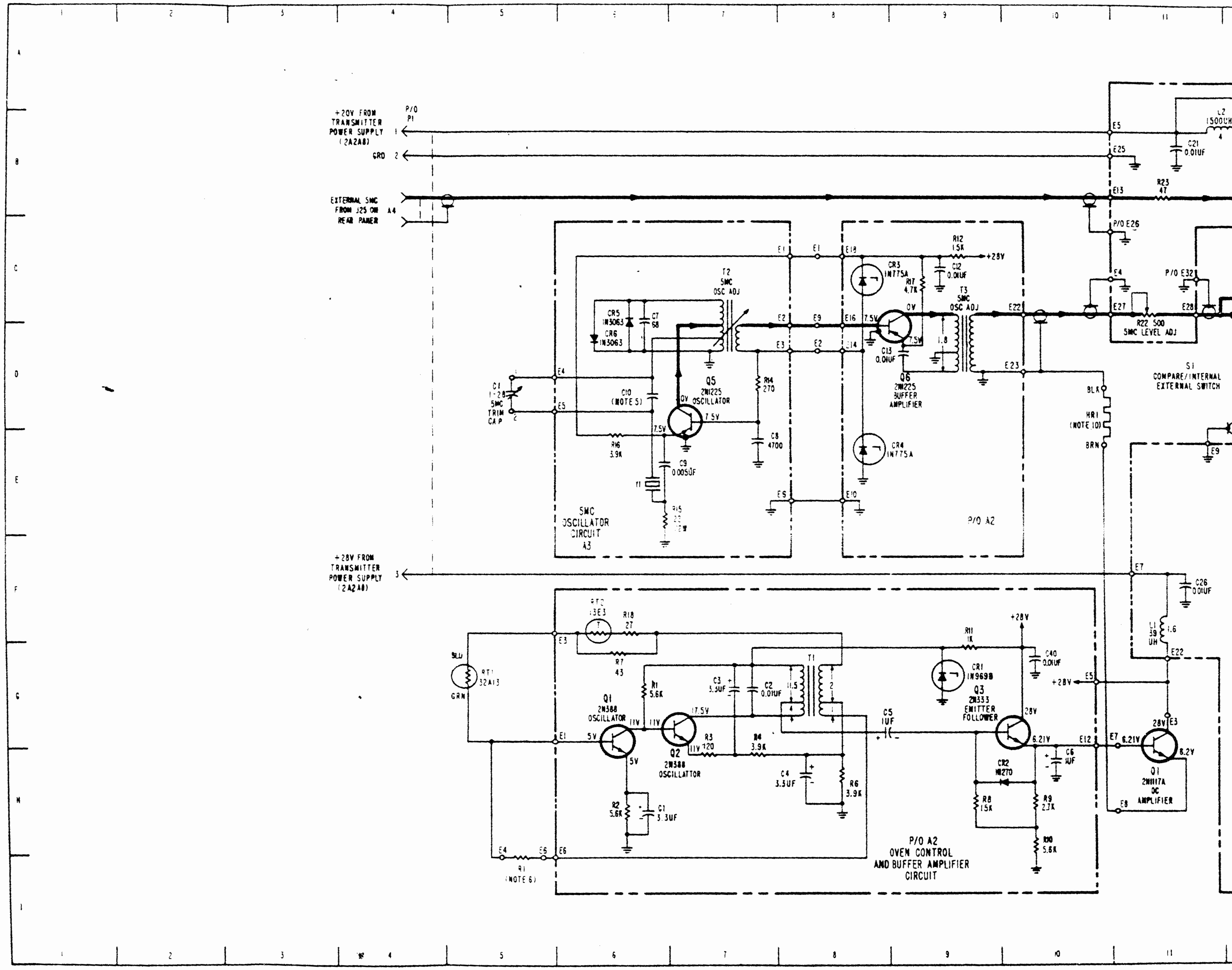
:, 4F, 21D,
1G, 21H

PART LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
A1Q5	13F	A2C3	7G
A1Q6	16D	A2C4	8H
A1Q7	15C	A2C5	8G
A1R1	19F	A2C6	10H
A1R2	18F	A2C12	9C
A1R3	19F	A2C13	9D
A1R4	18F	A2C40	10G
A1R5	15E	A2CR1	9G
A1R6	15E	A2CR2	10H
A1R7	16F	A2CR3	8C
A1R8	17E	A2CR4	8E
A1R9	16E	A2Q1	6G
A1R10	16F	A2Q2	7G
A1R11	16F	A2Q3	10G
A1R12	15F	A2Q6	9D
A1R13	16G	A2R1	6G
A1R14	13G	A2R2	6H
A1R15	12G	A2R3	7H
A1R16	12H	A2R4	7H
A1R17	13E	A2R6	8H
A1R18	13D	A2R7	6G
A1R19	12F	A2R8	9H
A1R20	13E	A2R9	10H
A1R21	12E	A2R10	10H
A1R22	11C	A2R11	9G
A1R23	11B	A2R12	9C
A1R24	13B	A2R17	9C
A1R25	13B	A2R18	6F
A1R26	16C	A2RT2	6F
A1R27	16C	A2T1	8G
A1R28	15C	A2T3	9D
A1R29	15D	A3C7	6C
A1R30	16D	A3C8	7E
A1R31	14B	A3C9	6E
A1T1	18G	A3C10	6D
A1T2	15E	A3CR5	6C
A1T3	18E	A3CR6	6D
A1T4	14H	A3Q5	7D
A1T5	14F	A3R14	7D
A1T6	14C	A3R15	6E
A1TP1	14C	A3R16	6E
A1TP2	18G	A3T2	7C
A2C1	6H	A3Y1	6E
A2C2	7G		



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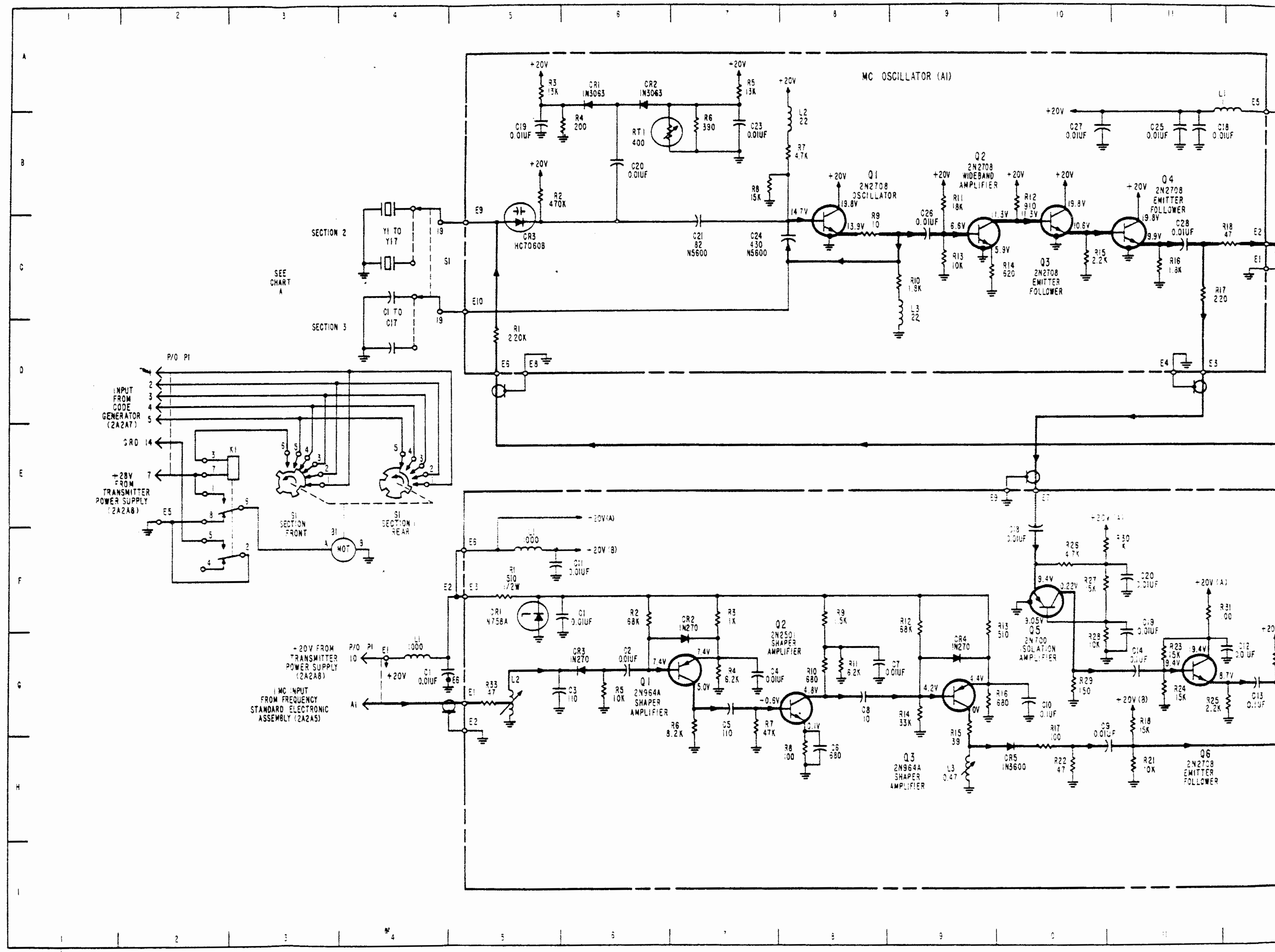
PART LOCATION INDEX

REF DESIG	LOC
C1	5D
HR1	10D
P1	4B, 4C, 4F, 21D, 21E, 21G, 21H
Q1	11H
R1	5I
RT1	5G
S1	12C
A1C1	19F
A1C2	19F
A1C3	20F
A1C4	18F
A1C5	19G
A1C6	16E
A1C7	16E
A1C8	16F
A1C9	17E
A1C10	16G
A1C11	18E
A1C12	17E
A1C13	15G
A1C14	16F
A1C15	13G
A1C16	13H
A1C17	12H
A1C18	13F
A1C19	12F
A1C20	12B
A1C21	11B
A1C22	14B
A1C23	14C
A1C24	16C
A1C25	15D
A1C26	11F
A1CR1	14C
A1CR2	16C
A1DS1	17D
A1L1	11F
A1L2	11A
A1Q1	19F
A1Q2	16E
A1Q3	16G
A1Q4	13H
A1Q5	13F
A1Q6	16D
A1Q7	15C
A1R1	19F
A1R2	18F
A1R3	19F
A1R4	18F
A1R5	15E
A1R6	15E
A1R7	16F
A1R8	17E
A1R9	16E
A1R10	16F
A1R11	16F
A1R12	15F
A1R13	16G
A1R14	13G
A1R15	12G
A1R16	12H
A1R17	13E
A1R18	13D
A1R19	12F
A1R20	13E
A1R21	12E
A1R22	11C
A1R23	11B
A1R24	13B
A1R25	13B
A1R26	16C
A1R27	16C
A1R28	15C
A1R29	15D
A1R30	16D
A1R31	14B
A1T1	18G
A1T2	15E
A1T3	18E
A1T4	14H
A1T5	14F
A1T6	14C
A1TP1	14C
A1TP2	18G
A2C1	6H
A2C2	7G

ON INDEX

REF DESIG	LOC	REF DESIG	LOC
A2R13	21G	A3L3	9H
A2R14	22G	A3L4	13G
A2R15	22F	A3Q1	7G
A2R16	22G	A3Q2	8G
A2R17	22G	A3Q3	9G
A2R18	22H	A3Q4	13G
A2R19	22H	A3Q5	10F
A2R20	22H	A3Q6	11G
A2R21	23G	A3R1	5F
A2R22	15F	A3R2	6F
A2RT1	22H	A3R3	7F
A2T1	18G	A3R4	7G
A2T2	19G	A3R5	6G
A2TP1	18G	A3R6	7G
A2TP2	21G	A3R7	7G
A2TP3	23F	A3R8	8H
A3C1	6F	A3R9	8F
A3C2	6G	A3R10	8G
A3C3	5G	A3R11	8G
A3C4	7G	A3R12	9F
A3C5	7G	A3R13	9F
A3C6	8H	A3R14	9G
A3C7	8G	A3R15	9G
A3C8	8G	A3R16	9G
A3C9	10H	A3R17	10H
A3C10	10G	A3R18	11G
A3C11	5F	A3R19	12G
A3C12	12G	A3R20	12G
A3C13	12G	A3R21	11H
A3C14	11G	A3R22	10H
A3C15	13G	A3R23	11G
A3C16	13G	A3R24	11G
A3C17	14G	A3R25	12G
A3C18	10F	A3R26	10F
A3C19	11G	A3R27	10F
A3C20	11F	A3R28	10G
A3CR1	5F	A3R29	10G
A3CR2	7G	A3R30	10F
A3CR3	6G	A3R31	11F
A3CR4	9G	A3R32	14G
A3CR5	10H	A3R33	5G
A3L1	5F	A3T1	13G
A3L2	5G	A3TP1	13F



PART LOCATION INDEX

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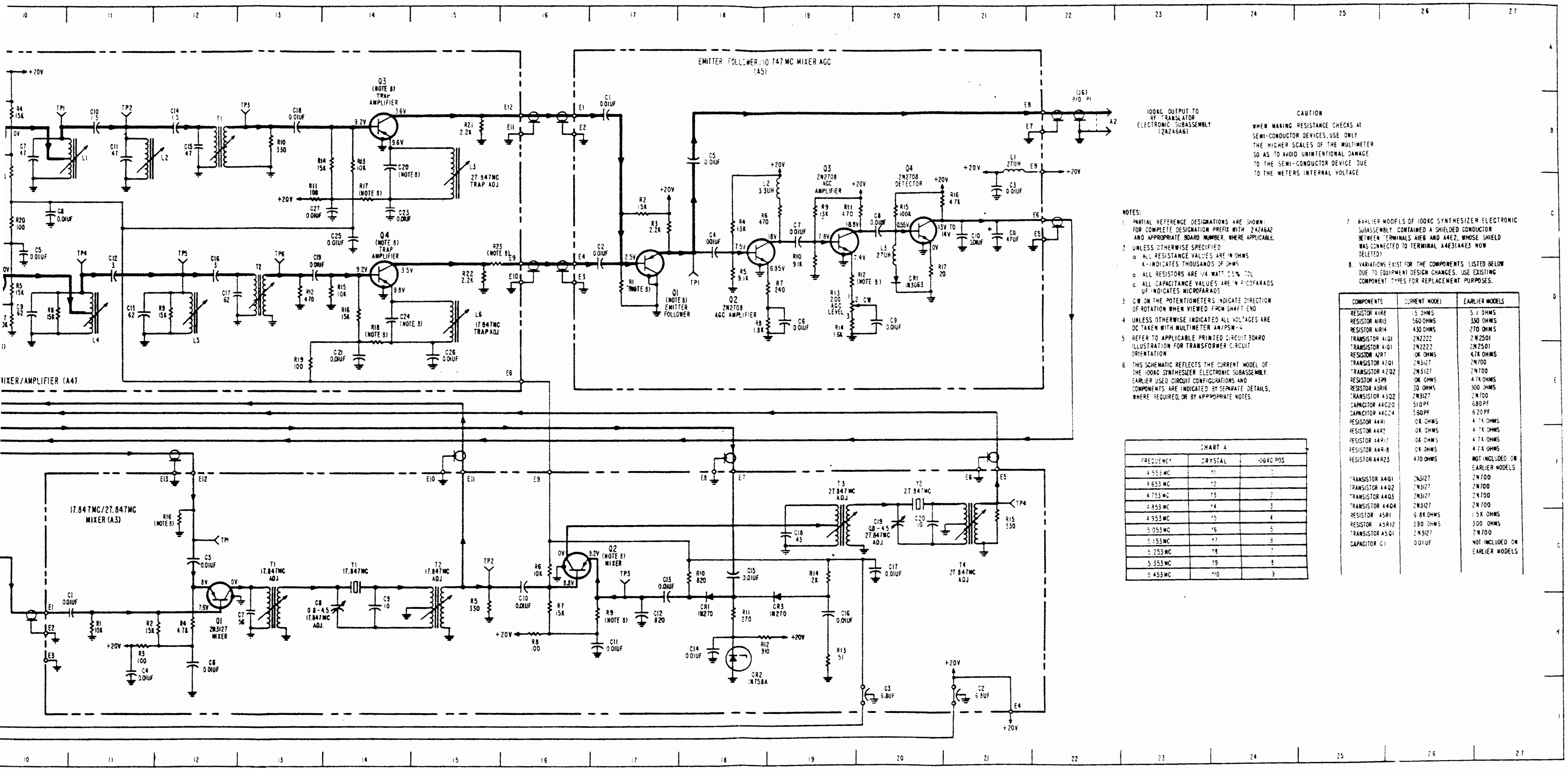
B1	3F
C1 thru C17	4C
C1	4G
C2	16E
K1	3E, 3D
L1	4G
L2	15E
P1	2D, 2E, 4G, 12C
S1	3E, 4C, 4E
Y1 thru Y17	4C
A1C18	11B
A1C19	5B
A1C20	6B
A1C21	7C
A1C23	7B
A1C24	8C
A1C25	11B
A1C26	9C
A1C27	10B
A1C28	11C
A1CR1	6A
A1CR2	6A
A1CR3	5C
A1L1	11A
A1L2	8B
A1L3	9C
A1Q1	8C
A1Q2	9C
A1Q3	10C
A1Q4	11C
A1R1	5D
A1R2	5B
A1R3	5A
A1R4	6B
A1R5	7A
A1R6	7B
A1R7	8B
A1R8	7B
A1R9	8C
A1R10	9C
A1R11	9B
A1R12	10B
A1R13	9C
A1R14	9C
A1R15	10C
A1R16	11C
A1R17	11C
A1R18	12C
A1RT1	6B
A2C1	15G
A2C2	16F
A2C3	16G
A2C4	16F
A2C5	19G
A2C6	19G
A2C7	21G
A2C8	21G
A2C9	21H
A2C10	21F
A2C11	22H
A2C12	18G
A2C13	20G
A2C14	15F
A2CR1	20G
A2J1	23G
A2J2	22F
A2L1	20G
A2L2	21G
A2L3	21G
A2L4	21H
A2P1	23G
A2P2	22F
A2Q1	16G
A2Q2	19G
A2Q3	22G
A2R1	16F
A2R2	16G
A2R3	16F
A2R4	16F
A2R5	16G
A2R6	17G
A2R7	18G
A2R8	18G
A2R9	19F
A2R10	19G
A2R11	19G
A2R12	20G
A2R13	21G
A2R14	22G
A2R15	22F
A2R16	22G
A2R17	22G
A2R18	22H
A2R19	22H
A2R20	22H
A2R21	23G
A2R22	15F
A2RT1	22H
A2T1	18G
A2T2	19G
A2TP1	18G
A2TP2	21G
A2TP3	23F
A3C1	6F
A3C2	6G
A3C3	5G
A3C4	7G
A3C5	7G
A3C6	8H
A3C7	8G
A3C8	8G
A3C9	10H
A3C10	10G
A3C11	5F
A3C12	12G
A3C13	12G
A3C14	11G
A3C15	13G
A3C16	13G
A3C17	14G
A3C18	10F
A3C19	11G
A3C20	11F
A3CR1	5F
A3CR2	7G
A3CR3	6G
A3CR4	9G
A3CR5	10H
A3L1	5F
A3L2	5G



CAUTION

WHEN MAKING RESISTANCE CHECKS AT SEMI-CONDUCTOR DEVICES, USE ONLY THE HIGHER SCALES OF THE MULTIMETER SO AS TO AVOID UNINTENTIONAL DAMAGE TO THE SEMI-CONDUCTOR DEVICE DUE TO THE METERS INTERNAL VOLTAGE.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH 2A2A6A2 AND APPROPRIATE BOARD NUMBER, WHERE APPLICABLE.
2. UNLESS OTHERWISE SPECIFIED
   a. ALL RESISTANCE VALUES ARE IN OHMS K-INDICATES THOUSANDS OF OHMS
   b. ALL RESISTORS ARE 1/4 WATT, ±5% TOL
   c. ALL CAPACITANCE VALUES ARE IN PICOFARADS UF INDICATES MICROFARADS
3. CW ON THE POTENTIOMETERS INDICATE DIRECTION OF ROTATION WHEN VIEWED FROM SHAFT END
4. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4
5. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATION FOR TRANSFORMER CIRCUIT ORIENTATION
6. THIS SCHEMATIC REFLECTS THE CURRENT MODEL OF THE 100KC SYNTHESIZER ELECTRONIC SUBASSEMBLY. EARLIER USED CIRCUIT CONFIGURATIONS AND COMPONENTS ARE INDICATED BY SEPARATE DETAILS, WHERE REQUIRED, OR BY APPROPRIATE NOTES.
7. EARLIER MODELS OF 100KC SYNTHESIZER ELECTRONIC SUBASSEMBLY CONTAINED A SHIELDED CONDUCTOR BETWEEN TERMINALS A1E6 AND A4E2, WHOSE SHIELD WAS CONNECTED TO TERMINAL A4E3 (A4E3 NOW DELETED)
8. VARIATIONS EXIST FOR THE COMPONENTS LISTED BELOW DUE TO EQUIPMENT DESIGN CHANGES. USE EXISTING COMPONENT TYPES FOR REPLACEMENT PURPOSES.

COMPONENTS	CURRENT MODEL	EARLIER MODELS
RESISTOR A1R8	15 OHMS	5.1 OHMS
RESISTOR A1R13	560 OHMS	330 OHMS
RESISTOR A1R14	430 OHMS	270 OHMS
TRANSISTOR A1Q1	2N2222	2N2501
TRANSISTOR A1Q1	2N2222	2N2501
RESISTOR A2R7	10K OHMS	47K OHMS
TRANSISTOR A2Q1	2N3127	2N700
TRANSISTOR A2Q2	2N3127	2N700
RESISTOR A3R9	10K OHMS	4.7K OHMS
RESISTOR A3R16	30 OHMS	300 OHMS
TRANSISTOR A3Q2	2N3127	2N700
CAPACITOR A4C20	510PF	680PF
CAPACITOR A4C24	560PF	620PF
RESISTOR A4R1	10K OHMS	4.7K OHMS
RESISTOR A4R2	10K OHMS	4.7K OHMS
RESISTOR A4R17	10K OHMS	4.7K OHMS
RESISTOR A4R18	10K OHMS	4.7K OHMS
RESISTOR A4R23	470 OHMS	NOT INCLUDED ON EARLIER MODELS
TRANSISTOR A4Q1	2N3127	2N700
TRANSISTOR A4Q2	2N3127	2N700
TRANSISTOR A4Q3	2N3127	2N700
TRANSISTOR A4Q4	2N3127	2N700
RESISTOR A5R1	6.8K OHMS	1.5K OHMS
RESISTOR A5R12	390 OHMS	300 OHMS
TRANSISTOR A5Q1	2N3127	2N700
CAPACITOR C1	0.01UF	NOT INCLUDED ON EARLIER MODELS

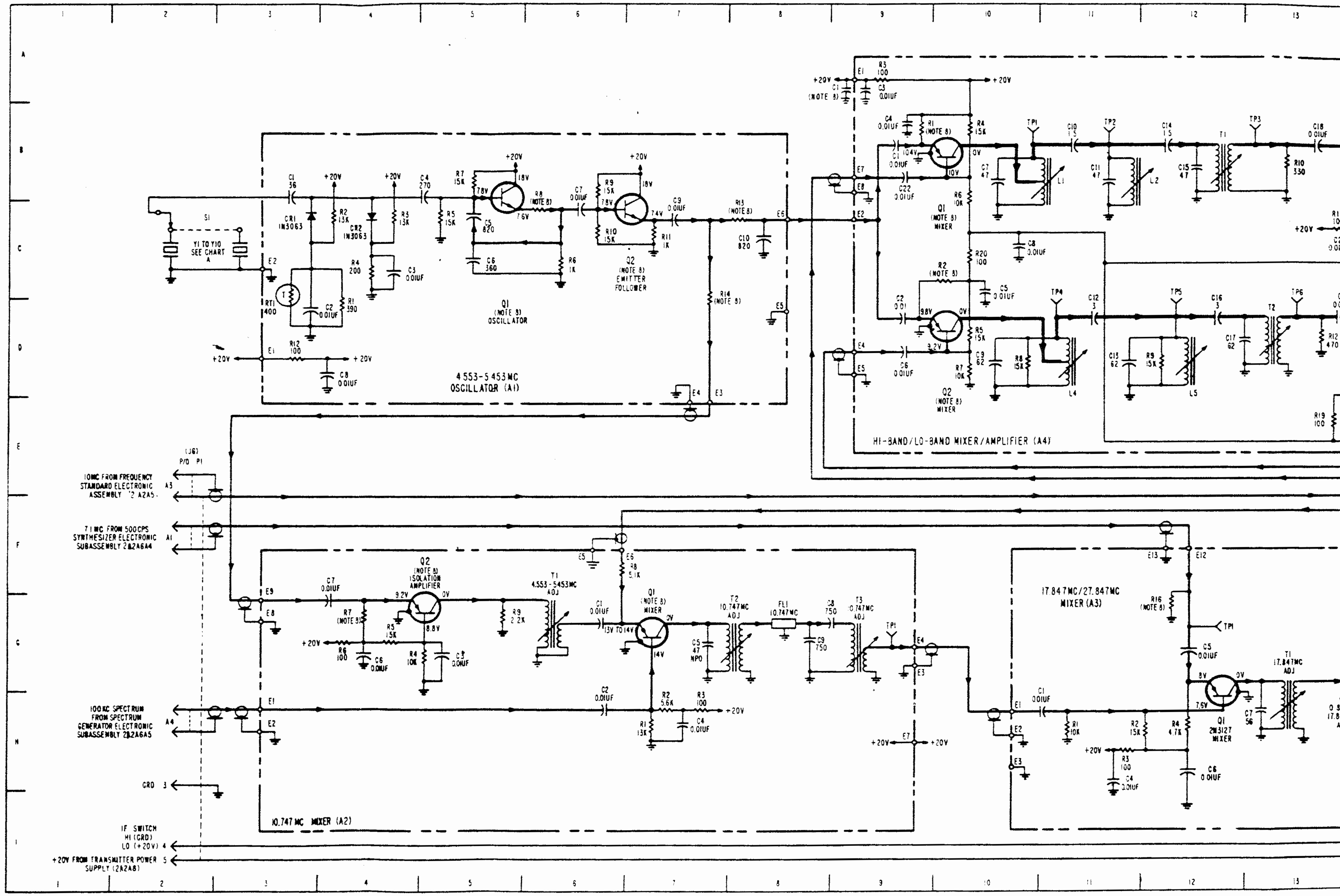
CHART A

FREQUENCY	CRYSTAL	100KC POS
4.553 MC	Y1	0
4.653 MC	Y2	1
4.753 MC	Y3	2
4.853 MC	Y4	3
4.953 MC	Y5	4
5.053 MC	Y6	5
5.153 MC	Y7	6
5.253 MC	Y8	7
5.353 MC	Y9	8
5.453 MC	Y10	9

Figure 5-11. 100 KC Synthesizer Electronic Subassembly, Schematic Diagram

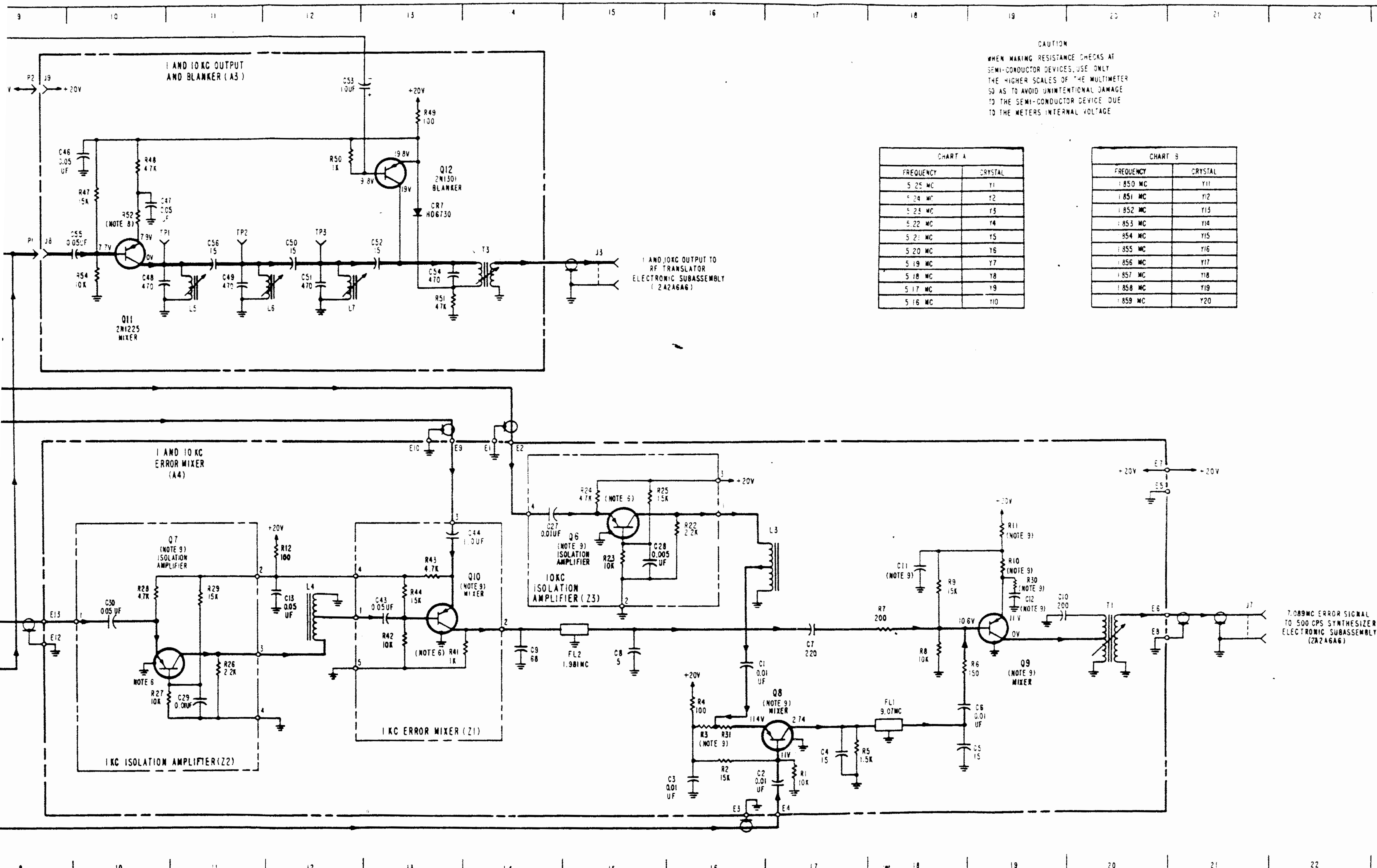
TION INDEX

LOC	REF DESIG	LOC	REF DESIG	LOC
18H	A4L5	12D	A5C8	20C
18H	A3L6	15D	A5C9	20D
19H	A4Q1	10B	A5C10	21C
19G	A4Q2	10D	A5C11	21C
21G	A4Q3	14B	A5CR1	20D
12G	A4Q4	14D	A5L1	21B
13H	A4R1	9B	A5L2	19C
15H	A4R2	10C	A5L3	20C
19G	A4R3	9A	A5Q1	17D
21G	A4R4	10B	A5Q2	18C
12G	A4R5	10D	A5Q3	19C
15G	A4R6	10B	A5Q4	20C
17G	A4R7	10D	A5R1	17D
21F	A4R8	10D	A5R2	17C
14G	A4R9	12D	A5R3	17C
20F	A4R10	13B	A5R4	18C
9B	A4R11	13C	A5R5	18D
9D	A4R12	13D	A5R6	19C
9A	A4R13	14B	A5R7	19D
9B	A4R14	14B	A5R8	19D
10C	A4R15	14D	A5R9	19C
9D	A4R16	14D	A5R10	19D
10B	A4R17	14C	A5R11	20C
10C	A4R18	14E	A5R12	19D
10D	A4R19	13E	A5R13	19D
11B	A4R20	10C	A5R14	19D
11B	A4R21	15B	A5R15	20C
11D	A4R22	15D	A5R16	21C
11D	A4R23	15C	A5R17	20D
12B	A4T1	12B	A5TP1	18D
12B	A4T2	13D		
12D	A4TP1	10B		
12D	A4TP2	11B		
13B	A4TP3	13B		
13D	A4TP4	11D		
14B	A4TP5	12D		
14E	A4TP6	13D		
9B	A5C1	17B		
14C	A5C2	17D		
14D	A5C3	21C		
14C	A5C4	18C		
15E	A5C5	18B		
14C	A5C6	19D		
11B	A5C7	19C		
11B				
15B				
11D				



PART LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	8A	A2R2	7H	A3R11	18H	A4L5	12D	A5C8	20C
P1	2E, 2F	A2R3	7H	A3R12	18H	A3L6	15D	A5C9	20D
	2H, 2I,	A2R4	5G	A3R13	19H	A4Q1	10B	A5C10	21C
	22B	A2R5	4G	A3R14	19G	A4Q2	10D	A5C11	21C
S1	2C	A2R6	4G	A3R15	21G	A4Q3	14B	A5CR1	20D
Y1 thru Y10	2C	A2R7	4G	A3R16	12G	A4Q4	14D	A5L1	21B
A1C1	3C	A2R8	6F	A3T1	13H	A4R1	9B	A5L2	19C
A1C2	3D	A2R9	5G	A3T2	15H	A4R2	10C	A5L3	20C
A1C3	4C	A2T1	6G	A3T3	19G	A4R3	9A	A5Q1	17D
A1C4	5C	A2T2	8G	A3T4	21G	A4R4	10B	A5Q2	18C
A1C5	5C	A2T3	9G	A3TP1	12G	A4R5	10D	A5Q3	19C
A1C6	5C	A2TP1	9G	A3TP2	15G	A4R6	10B	A5Q4	20C
A1C7	6C	A3C1	11H	A3TP3	17G	A4R7	10D	A5R1	17D
A1C8	4D	A3C2	21I	A3TP4	21F	A4R8	10D	A5R2	17C
A1C9	7C	A3C3	20I	A3Y1	14G	A4R9	12D	A5R3	17C
A1C10	8C	A3C4	11H	A3Y2	20F	A4R10	13B	A5R4	18C
A1CR1	3C	A3C5	12G	A4C1	9B	A4R11	13C	A5R5	18D
A1CR2	4C	A3C6	12H	A4C2	9D	A4R12	13D	A5R6	19C
A1Q1	5C	A3C7	13H	A4C3	9A	A4R13	14B	A5R7	19D
A1Q2	7C	A3C8	14H	A4C4	9B	A4R14	14B	A5R8	19D
A1R1	4C	A3C9	14H	A4C5	10C	A4R15	14D	A5R9	19C
A1R2	4C	A3C10	16G	A4C6	9D	A4R16	14D	A5R10	19D
A1R3	4C	A3C11	17H	A4C7	10B	A4R17	14C	A5R11	20C
A1R4	4C	A3C12	17H	A4C8	10C	A4R18	14E	A5R12	19D
A1R5	5C	A3C13	17G	A4C9	10D	A4R19	13E	A5R13	19D
A1R6	6C	A3C14	18H	A4C10	11B	A4R20	10C	A5R14	19D
A1R7	5B	A3C15	18G	A4C11	11B	A4R21	15B	A5R15	20C
A1R8	6C	A3C16	19H	A4C12	11D	A4R22	15D	A5R16	21C
A1R9	6B	A3C17	20G	A4C13	11D	A4R23	15C	A5R17	20D
A1R10	6C	A3C18	19G	A4C14	12B	A4T1	12B	A5TP1	18D
A1R11	7C	A3C19	20G	A3C15	12B	A4T2	13D		
A1R12	3D	A3C20	20G	A4C16	12D	A4TP1	10B		
A1R13	8C	A3CR1	18H	A4C17	12D	A4TP2	11B		
A1R14	7C	A3CR2	18H	A4C18	13B	A4TP3	13B		
A1RT1	3C	A3CR3	19H	A4C19	13D	A4TP4	11D		
A2C1	6G	A3Q1	12H	A4C20	14B	A4TP5	12D		
A2C2	6H	A3Q2	16G	A4C21	14E	A4TP6	13D		
A2C3	5G	A3R1	11H	A3C22	9B	A5C1	17B		
A2C4	7H	A3R2	12H	A4C23	14C	A5C2	17D		
A2C5	7G	A3R3	11H	A4C24	14D	A5C3	21C		
A2C6	4G	A3R4	12H	A4C25	14C	A5C4	18C		
A2C7	4G	A3R5	15H	A4C26	15E	A5C5	18B		
A2C8	9G	A3R6	16G	A4C27	14C	A5C6	19D		
A2C9	8G	A3R7	16H	A4L1	11B	A5C7	19C		
A2FL1	8G	A3R8	16H	A4L2	11B				
A2Q1	7G	A3R9	17H	A4L3	15B				
A2Q2	5G	A3R10	18G	A4L4	11D				
A2R1	7H								



CAUTION

WHEN MAKING RESISTANCE CHECKS AT SEMI-CONDUCTOR DEVICES, USE ONLY THE HIGHER SCALES OF THE MULTIMETER SO AS TO AVOID UNINTENTIONAL DAMAGE TO THE SEMI-CONDUCTOR DEVICE DUE TO THE METERS INTERNAL VOLTAGE

CHART A

FREQUENCY	CRYSTAL
5.25 MC	Y1
5.24 MC	Y2
5.23 MC	Y3
5.22 MC	Y4
5.21 MC	Y5
5.20 MC	Y6
5.19 MC	Y7
5.18 MC	Y8
5.17 MC	Y9
5.16 MC	Y10

CHART B

FREQUENCY	CRYSTAL
1.850 MC	Y11
1.851 MC	Y12
1.852 MC	Y13
1.853 MC	Y14
1.854 MC	Y15
1.855 MC	Y16
1.856 MC	Y17
1.857 MC	Y18
1.858 MC	Y19
1.859 MC	Y20

NOTES

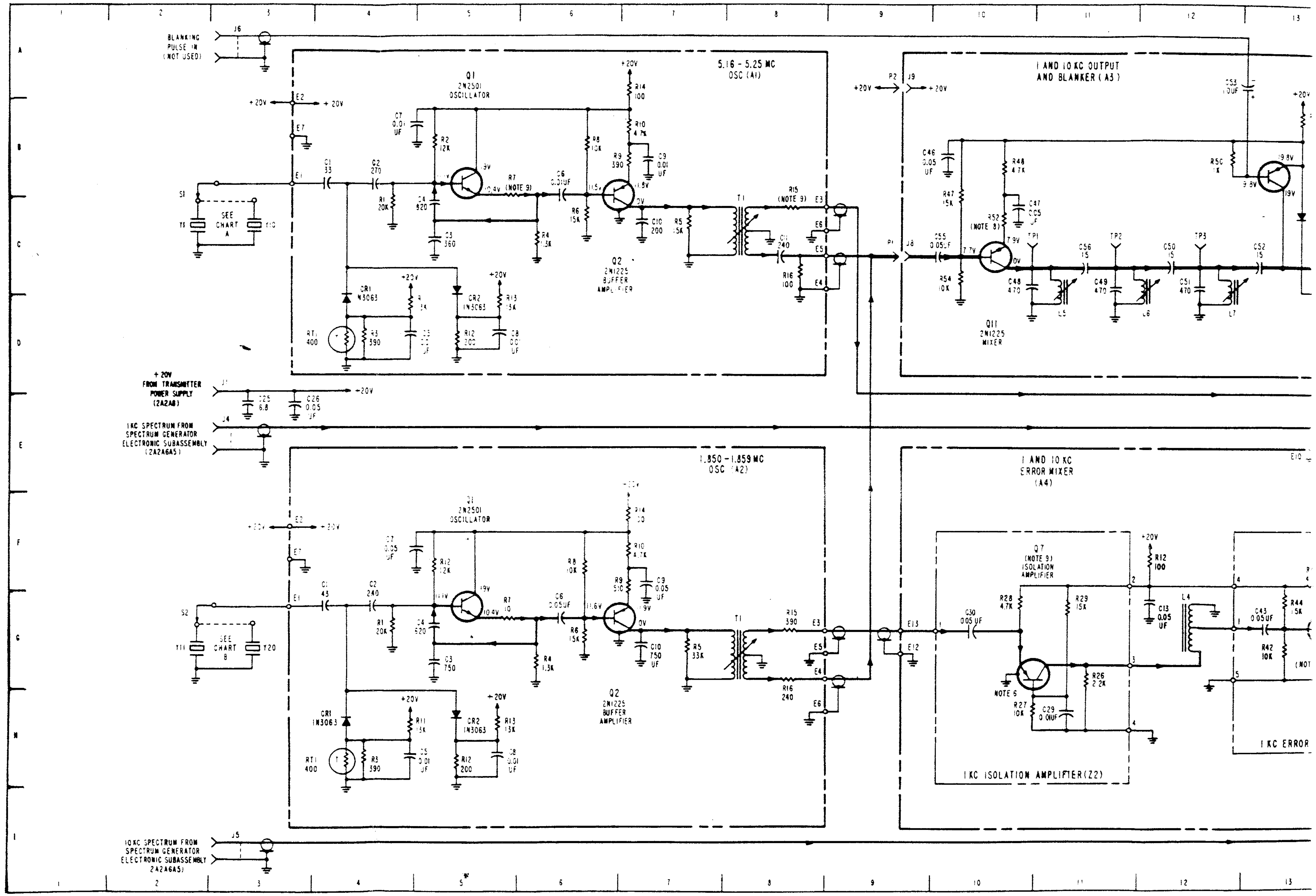
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH 2A2A6A3 AND APPROPRIATE BOARD NUMBER WHERE APPLICABLE
2. UNLESS OTHERWISE SPECIFIED
   a. ALL RESISTANCE VALUES ARE IN OHMS; K INDICATES THOUSANDS OF OHMS
   b. ALL RESISTORS ARE 1/4 WATT, ± 5% TOL
   c. ALL CAPACITANCE VALUES ARE IN PICOFARADS; UF INDICATES MICROFARADS
3. NUMBERS ADJACENT TO WINDINGS, COILS, AND TEST POINTS INDICATE DC RESISTANCE (VALUES LESS THAN ONE OHM ARE NOT SHOWN)
4. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4
5. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATION FOR TRANSFORMER CIRCUIT ORIENTATION
6. CIRCUITS Z1, Z2 AND Z3 IN A4 ARE ENCAPSULATED; TRANSISTORS A4Z1Q10, A4Z2Q7 AND A4Z3Q6 ARE THEREFORE INACCESSIBLE AND NO VOLTAGE READING FOR THESE TRANSISTORS ARE AVAILABLE
7. THIS SCHEMATIC REFLECTS THE CURRENT MODEL OF 1 AND 10 KC SYNTHESIZER ELECTRONIC SUBASSEMBLY. EARLIER USED CIRCUIT CONFIGURATIONS AND COMPONENTS ARE INDICATED BY SEPARATE DETAILS, WHERE REQUIRED OR BY APPROPRIATE NOTES
8. VALUE OF RESISTOR A3R52 IS SELECTED AT TIME OF ASSEMBLY BETWEEN 12 AND 39 OHMS
9. VARIATIONS EXIST FOR THE COMPONENTS LISTED BELOW DUE TO EQUIPMENT DESIGN CHANGES. USE EXISTING COMPONENT TYPES FOR REPLACEMENT PURPOSES.

COMPONENT	CURRENT MODEL	EARLIER MODELS
RESISTOR A1R7	5.1 OHMS	15 OHMS
RESISTOR A1R15	820 OHMS	620 OHMS
RESISTOR A4R3	10K OHMS	4.7K OHMS
RESISTOR A4R10	10K OHMS	4.7K OHMS
RESISTOR A4R11	470 OHMS	100 OHMS
RESISTOR A4R30	15 OHMS	NOT INCLUDED ON EARLIER MODELS
RESISTOR A4R31	62 OHMS	NOT INCLUDED ON EARLIER MODELS
CAPACITOR A4C11	0.01 UF	0.05 UF
CAPACITOR A4C12	0.01 UF	0.05 UF
TRANSISTOR A4Q8	2N3127	EARLIER MODELS USED 2N700 UNMARKED BUT SELECTED FOR LOW GAIN; LATER MODELS USED 2N700 MARKED WITH BLUE DOT, STILL LATER MODELS USED SM2059
TRANSISTOR A4Q9	2N3127	2N700
TRANSISTOR A4Z1Q10	2N3127	2N700
TRANSISTOR A4Z2Q7	2N3127	2N700
TRANSISTOR A4Z3Q6	2N3127	2N700

Figure 5-12. 1 and 10 KC Synthesizer Electronic Subassembly, Schematic Diagram

NDEX

F SIG	LOC	REF DESIG	LOC
CR7	13C	A4R7	18G
J8	9C	A4R8	18G
J9	9A	A4R9	18F
J10	9D	A4R10	19F
L5	11C	A4R11	19F
L6	12C	A4R12	12F
L7	12C	A4R30	19F
Q11	10C	A4R31	16H
Q12	13B	A4T1	20G
R47	10B	A4Z1C43	13G
R48	10B	A4Z1C44	13F
R49	13B	A4Z1Q10	13G
R50	12B	A4Z1R41	13G
R51	13D	A4Z1R42	13G
R52	10C	A4Z1R43	13F
R54	10C	A4Z1R44	13G
T3	14C	A4Z2C29	11H
TP1	10C	A4Z2C30	10G
TP2	11C	A4Z2Q7	10G
TP3	12C	A4Z2R26	11G
C1	16G	A4Z2R27	10H
C2	17I	A4Z2R28	10G
C3	16I	A4Z2R29	11G
C4	17H	A4Z3C27	14F
C5	19H	A4Z3C28	15F
C6	19H	A4Z3Q6	15F
C7	17G	A4Z3R22	16F
C8	15G	A4Z3R23	15F
C9	14G	A4Z3R24	15F
C10	19G	A4Z3R25	15F
C11	18F		
C12	19G		
C13	12G		
FL1	18H		
FL2	15G		
L3	17F		
L4	12G		
Q8	17H		
Q9	19G		
R1	17I		
R2	16H		
R3	16H		
R4	16H		
R5	17H		
R6	19H		



PART LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C25	3E	A1RT1	4D	A3CR7	13C
C26	3E	A1T1	8C	A3J8	9C
J1	3D	A2C1	4G	A3J9	9A
J3	15C	A2C2	4G	A3J10	9D
J4	3E	A2C3	5G	A3L5	11C
J5	3I	A2C4	5G	A3L6	12C
J6	3A	A2C5	4H	A3L7	12C
J7	21G	A2C6	6G	A3Q11	10C
P1	9C	A2C7	4F	A3Q12	13B
P2	9A	A2C8	5H	A3R47	10B
S1	2B	A2C9	7F	A3R48	10B
S2	2G	A2C10	7G	A3R49	13B
Y1 thru Y10	2C, 3C	A2CR1	4H	A3R50	12B
Y11 thru Y20	2G, 3G	A2CR2	5H	A3R51	13D
A1C1	4B	A2Q1	5G	A3R52	10C
A1C2	4B	A2Q2	6G	A3R54	10C
A1C3	5C	A2R1	4G	A3T3	14C
A1C4	5C	A2R2	5F	A3TP1	10C
A1C5	4D	A2R3	4H	A3TP2	11C
A1C6	6B	A2R4	6G	A3TP3	12C
A1C7	4B	A2R5	7G	A4C1	16G
A1C8	5D	A2R6	6G	A4C2	17I
A1C9	7B	A2R7	5G	A4C3	16I
A1C10	7C	A2R8	6F	A4C4	17H
A1C11	8C	A2R9	7F	A4C5	19H
A1CR1	4C	A2R10	7F	A4C6	19H
A1CR2	5C	A2R11	4H	A4C7	17G
A1Q1	5B	A2R12	5H	A4C8	15G
A1Q2	6B	A2R13	5H	A4C9	14G
A1R1	4B	A2R14	7F	A4C10	19G
A1R2	5B	A2R15	8G	A4C11	18F
A1R3	4D	A2R16	8G	A4C12	19G
A1R4	6C	A2RT1	4H	A4C13	12G
A1R5	7C	A2T1	8G	A4FL1	18H
A1R6	6C	A3C46	10B	A4 FL2	15G
A1R7	5B	A3C47	10C	A4L3	17F
A1R8	6B	A3C48	10C	A4L4	12G
A1R9	7B	A3C49	11C	A4Q8	17H
A1R10	7B	A3C50	12C	A4Q9	19G
A1R11	4D	A3C51	12C	A4 R1	17I
A1R12	5D	A3C52	13C	A4R2	16H
A1R13	5C	A3C53	13A	A4R3	16H
A1R14	7A	A3C54	13C	A4R4	16H
A1R15	8C	A3C55	10C	A4R5	17H
A1R16	8C	A3C56	11C	A4R6	19H

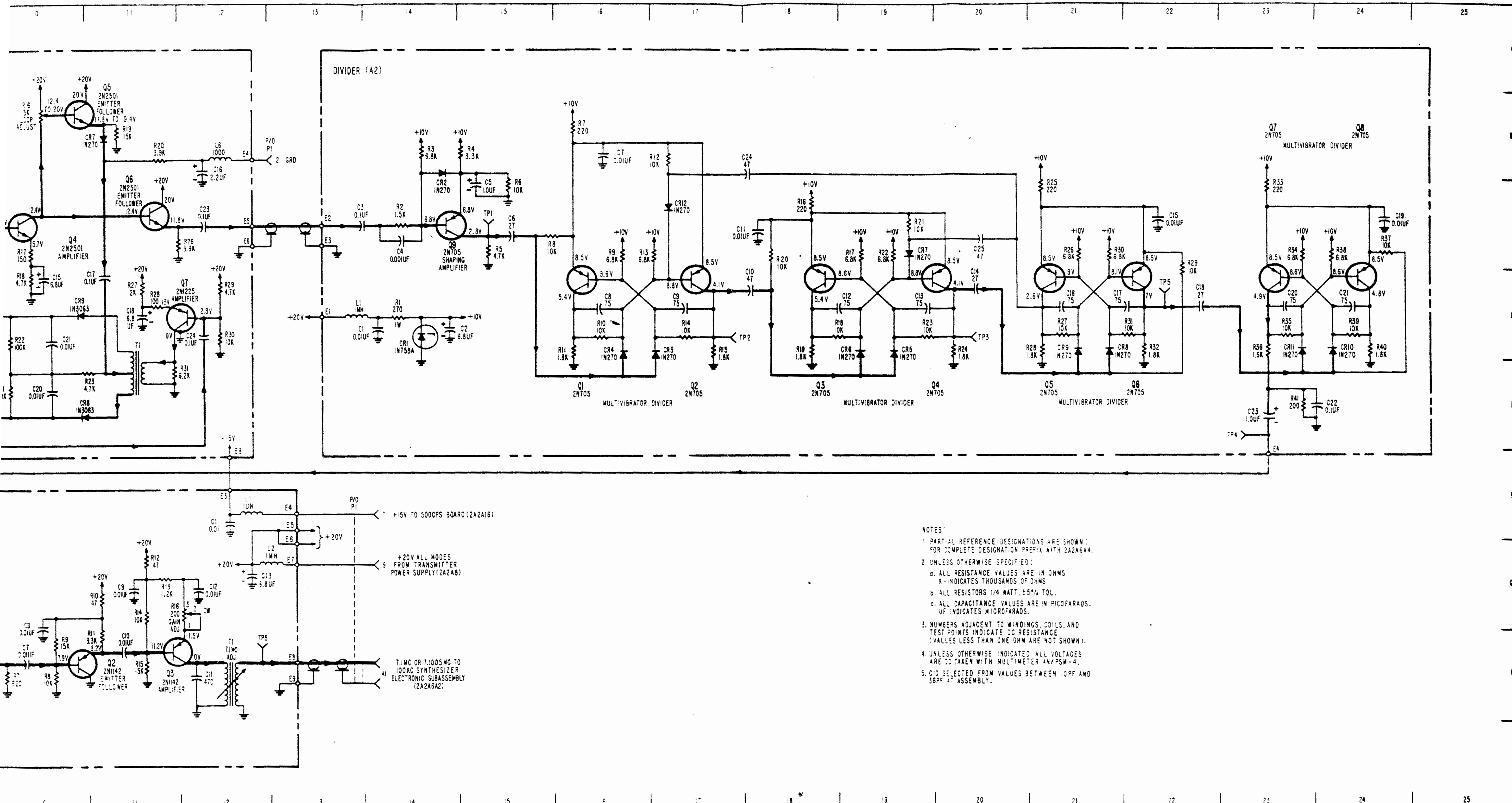
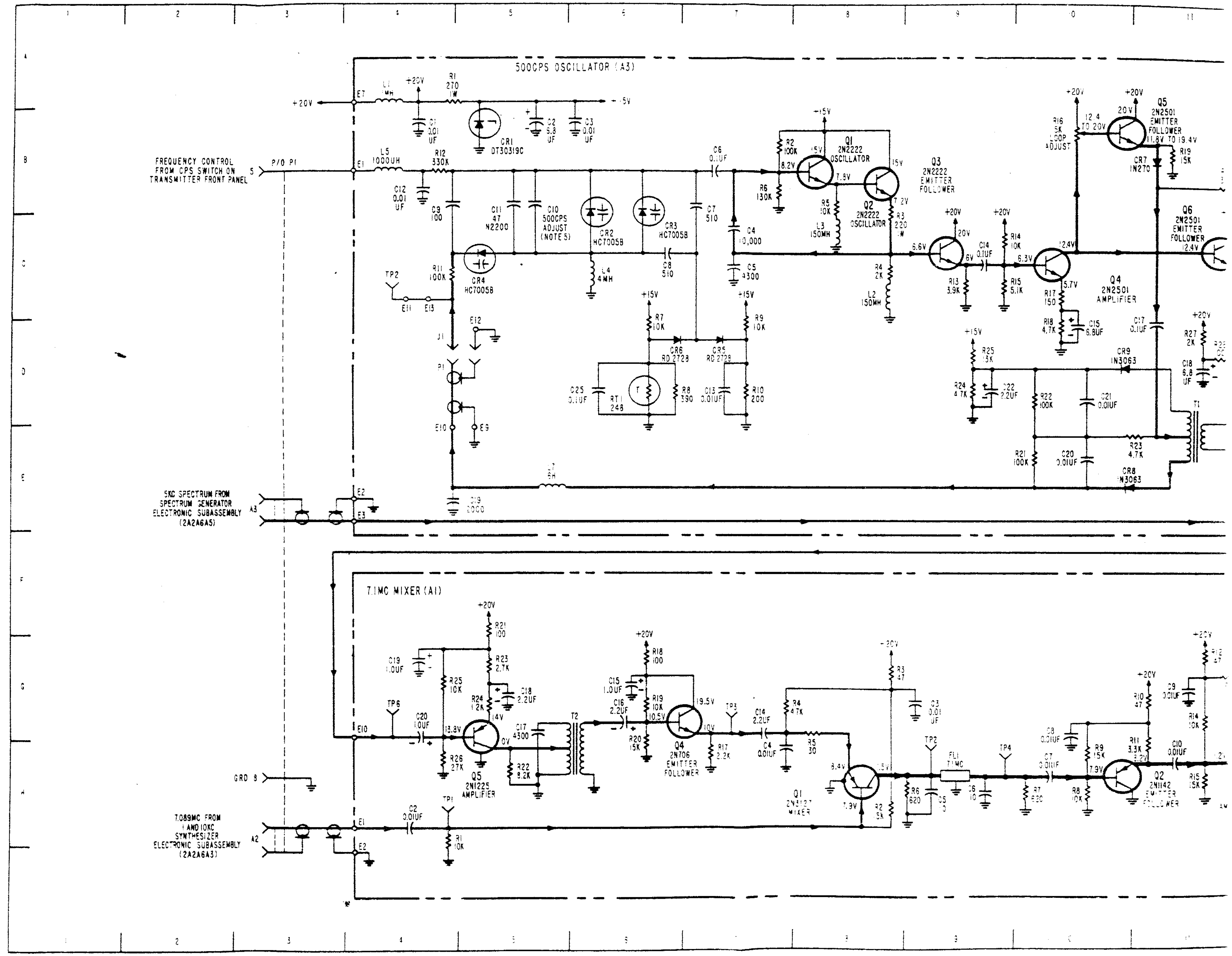


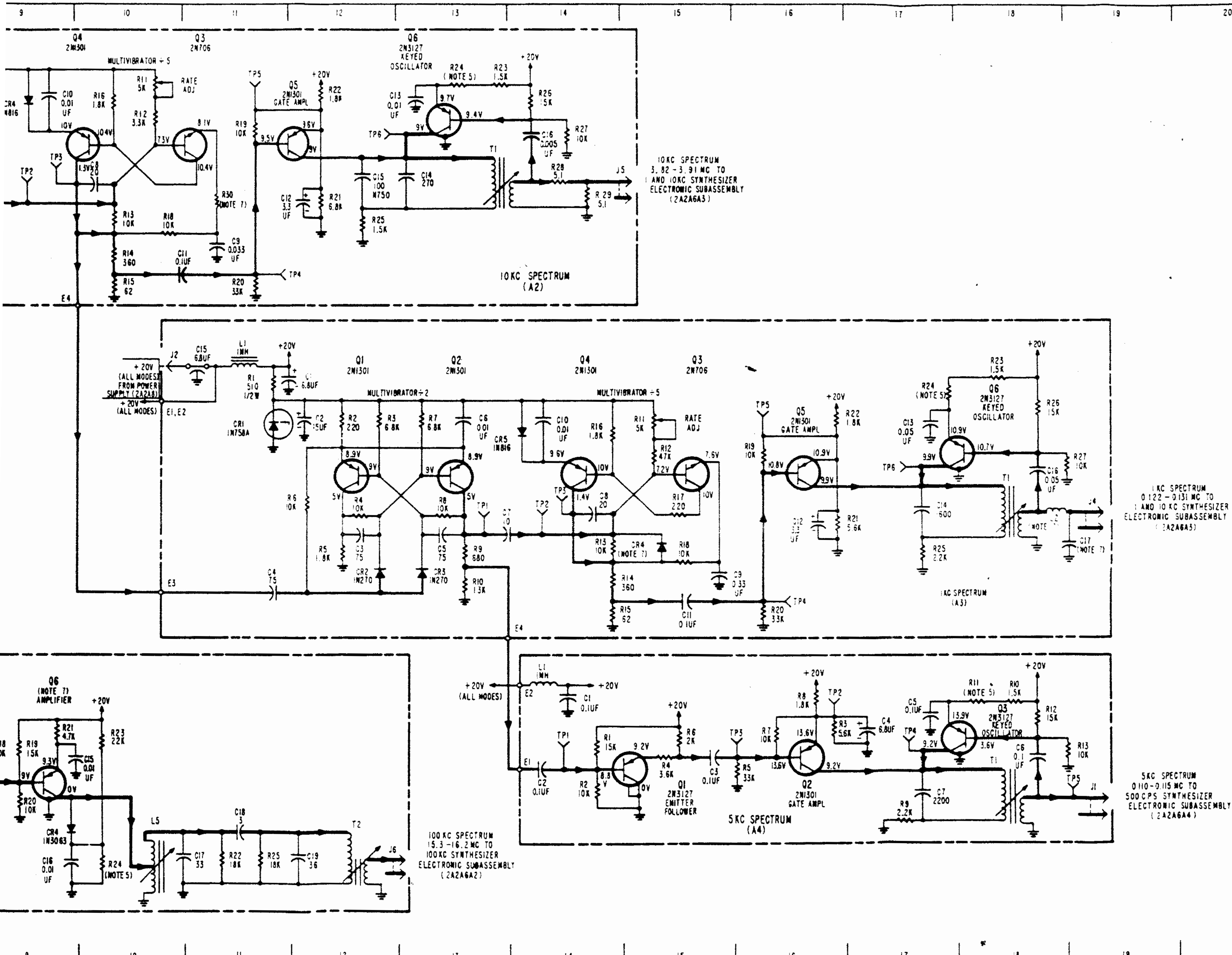
Figure 5-13. 500 CPS Synthesizer Electronic Subassembly, Schematic Diagram

REF DESIG	LOC
A3C19	4E
A3C20	10E
A3C21	10D
A3C22	9D
A3C23	12C
A3C24	12D
A3C25	6D
A3CR1	5B
A3CR2	6B
A3CR3	6B
A3CR4	5C
A3CR5	7D
A3CR6	6D
A3CR7	11B
A3CR8	10E
A3CR9	10D
A3J1	4D
A3L1	4A
A3L2	8C
A3L3	8C
A3L4	6C
A3L5	4B
A3L6	12B
A3L7	5E
A3P1	4D
A3Q1	8B
A3Q2	8B
A3Q3	9C
A3Q4	10C
A3Q5	10B
A3Q6	11C
A3Q7	11D
A3R1	4A
A3R2	7B
A3R3	8C
A3R4	8C
A3R5	8B
A3R6	7B
A3R7	5D
A3R8	5D
A3R9	7D
A3R10	7D
A3R11	4C
A3R12	4B

REF DESIG	LOC
A3R13	9C
A3R14	9C
A3R15	9C
A3R15	10B
A3R17	10C
A3R18	10D
A3R19	11B
A3R20	11B
A3R21	10E
A3R22	10D
A3R23	10E
A3R24	9D
A3R25	9D
A3R26	11C
A3R27	11D
A3R28	11D
A3R29	12D
A3R30	12D
A3R31	11E
A3RT1	6D
A3T1	11D, 11E
A3TP2	4C



REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG
P1	3B, 3E, 3H, 13B,	A1R14	11G	A2C24	18B	A2R21
	14F, 14G, 14H	A1R15	11H	A2C26	20C	A2R22
A1C1	12F	A1R16	12G	A2CR1	14D	A2R23
A1C2	4H	A1R17	7H	A2CR2	14B	A2R24
A1C3	9G	A1R18	6G	A2CR3	17D	A2R25
A1C4	7H	A1R19	6G	A2CR4	16D	A2R26
A1C5	9H	A1R20	6G	A2CR5	19D	A2R27
A1C6	9H	A1R21	5F	A2CR6	19D	A2R28
A1C7	10H	A1R22	5H	A2CR7	19C	A2R29
A1C8	10G	A1R23	5G	A2CR8	21D	A2R30
A1C9	11G	A1R24	5G	A2CR9	21D	A2R31
A1C10	11H	A1R25	4G	A2CR10	24D	A2R32
A1C11	12H	A1R26	4H	A2CR11	23D	A2R33
A1C12	12G	A1T1	12H	A2CR12	17C	A2R34
A1C13	12G	A1T2	6G	A2L1	13D	A2R35
A1C14	7G	A1TP1	4H	A2Q1	16D	A2R36
A1C15	6G	A1TP2	9H	A2Q2	17D	A2R37
A1C16	6G	A1TP3	7G	A2Q3	18D	A2R38
A1C17	5G	A1TP4	9H	A2Q4	19D	A2R39
A1C18	5G	A1TP5	12H	A2Q5	21D	A2R40
A1C19	4G	A1TP6	4G	A2Q6	22D	A2R41
A1C20	4G	A2C1	14D	A2Q7	23D	A2TP1
A1FL1	9H	A2C2	14D	A2Q8	24D	A2TP2
A1L1	12F	A2C3	13C	A2Q9	14C	A2TP3
A1L2	12G	A2C4	14C	A2R1	14D	A2TP4
A1Q1	8H	A2C5	15C	A2R2	14C	A2TP5
A1Q2	10H	A2C6	15C	A2R3	14B	A3C1
A1Q3	11H	A2C7	16B	A2R4	15B	A3C2
A1Q4	6G	A2C8	16D	A2R5	15C	A3C3
A1Q5	5G	A2C9	17D	A2R6	15C	A3C4
A1R1	4H	A2C10	18D	A2R7	16B	A3C5
A1R2	8H	A2C11	18C	A2R8	16C	A3C6
A1R3	8G	A2C12	18D	A2R9	16C	A3C7
A1R4	7G	A2C13	19D	A2R10	16D	A3C8
A1R5	8G	A2C14	20D	A2R11	16D	A3C9
A1R6	9H	A2C15	22C	A2R12	17B	A3C10
A1R7	10H	A2C16	21D	A2R13	17C	A3C11
A1R8	10H	A2C17	22D	A2R14	17D	A3C12
A1R9	10H	A2C18	22D	A2R15	17D	A3C13
A1R10	11G	A2C19	24C	A2R16	18C	A3C14
A1R11	11H	A2C20	23D	A2R17	19C	A3C15
A1R12	11G	A2C21	24D	A2R18	18D	A3C16
A1R13	11G	A2C22	24E	A2R19	18D	A3C17
		A2C23	23E	A2R20	18C	A3C18



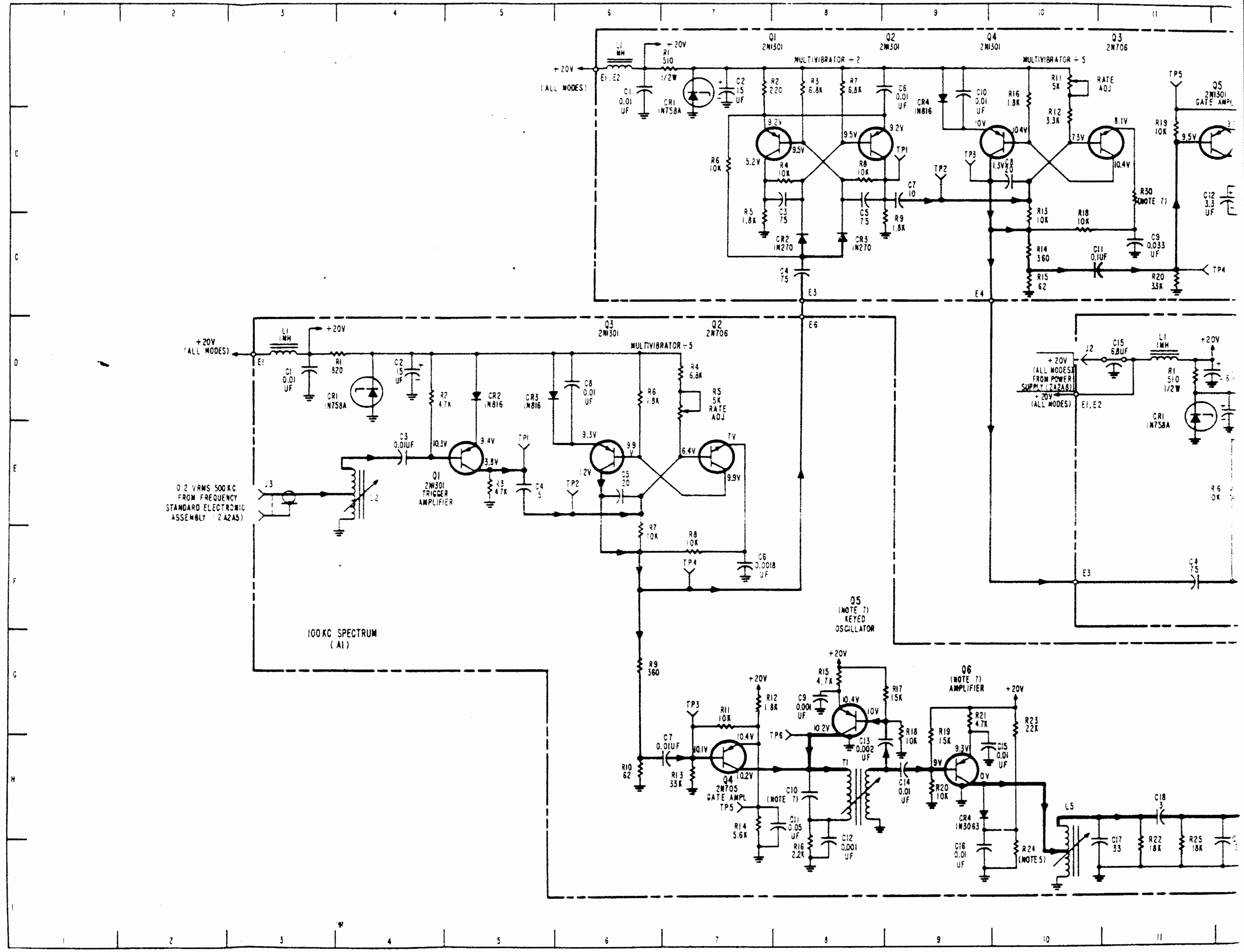
CAUTION

WHEN MAKING RESISTANCE CHECKS AT SEMI-CONDUCTOR DEVICES, USE ONLY THE HIGHER SCALES OF THE MULTIMETER SO AS TO AVOID UNINTENTIONAL DAMAGE TO THE SEMI-CONDUCTOR DEVICE DUE TO THE METERS INTERNAL VOLTAGE.

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH 2A2A6A5 AND APPROPRIATE BOARD NUMBER, WHERE APPLICABLE.
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTANCE VALUES ARE IN OHMS, K-INDICATES THOUSANDS OF OHMS.
   b. ALL RESISTORS ARE 1/4 WATT, ±5% TOL.
   c. ALL CAPACITANCE VALUES ARE IN PICOFARADS, UF INDICATES MICROFARADS.
3. UNLESS OTHERWISE INDICATED ALL ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4.
4. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATIONS FOR TRANSFORMER CIRCUIT ORIENTATION
5. VALUES OF RESISTORS A1R24, A2R24 A3R24 AND A4R11 SELECTED AT TIME OF ASSEMBLY FROM BETWEEN 1.0K AND 8.2K OHMS.
6. THIS SCHEMATIC REFLECTS THE CURRENT MODEL OF THE SPECTRUM GENERATOR ELECTRONIC SUBASSEMBLY. EARLIER USED CIRCUIT CONFIGURATIONS AND COMPONENTS ARE INDICATED BY SEPARATE DETAILS, WHERE REQUIRED, OR BY APPROPRIATE NOTES.
7. VARIATIONS EXIST FOR THE COMPONENTS LISTED BELOW DUE TO EQUIPMENT DESIGN CHANGES. CURRENT MODEL COMPONENTS MAY BE USED FOR REPLACEMENT PURPOSES IN EARLIER MODELS

COMPONENT	CURRENT MODEL	EARLIER MODELS
CAPACITOR A1C10	120 PF	150 PF
TRANSISTOR A1Q6	2N3127	2N700
RESISTOR A2R30	VALUE SELECTED AT TIME OF ASSEMBLY FROM BETWEEN 5.1 AND 47 OHMS.	NOT INCLUDED ON EARLIER MODELS.
CAPACITOR A3C17	0.005 UF	NOT INCLUDED ON EARLIER MODELS.
DIODE A3CR4	1N3063	1N816
INDUCTOR A3L2	27UH	NOT INCLUDED ON EARLIER MODELS.

Figure 5-14. Spectrum Generator Electronic Subassembly, Schematic Diagram


MULTIVIBRATOR ÷ 2
MULTIVIBRATOR ÷ 5
RATE ADJ
+20V (ALL MODES)
0.2 VRMS 500KC FROM FREQUENCY STANDARD ELECTRONIC ASSEMBLY (2A2A5)
Q1 2N301 TRIGGER AMPLIFIER
100KC SPECTRUM (A1)
Q5 (NOTE 7) KEYED OSCILLATOR
Q6 (NOTE 7) AMPLIFIER
Q4 2N705 GATE AMPL
+20V (ALL MODES) FROM POWER SUPPLY (2A2A8)

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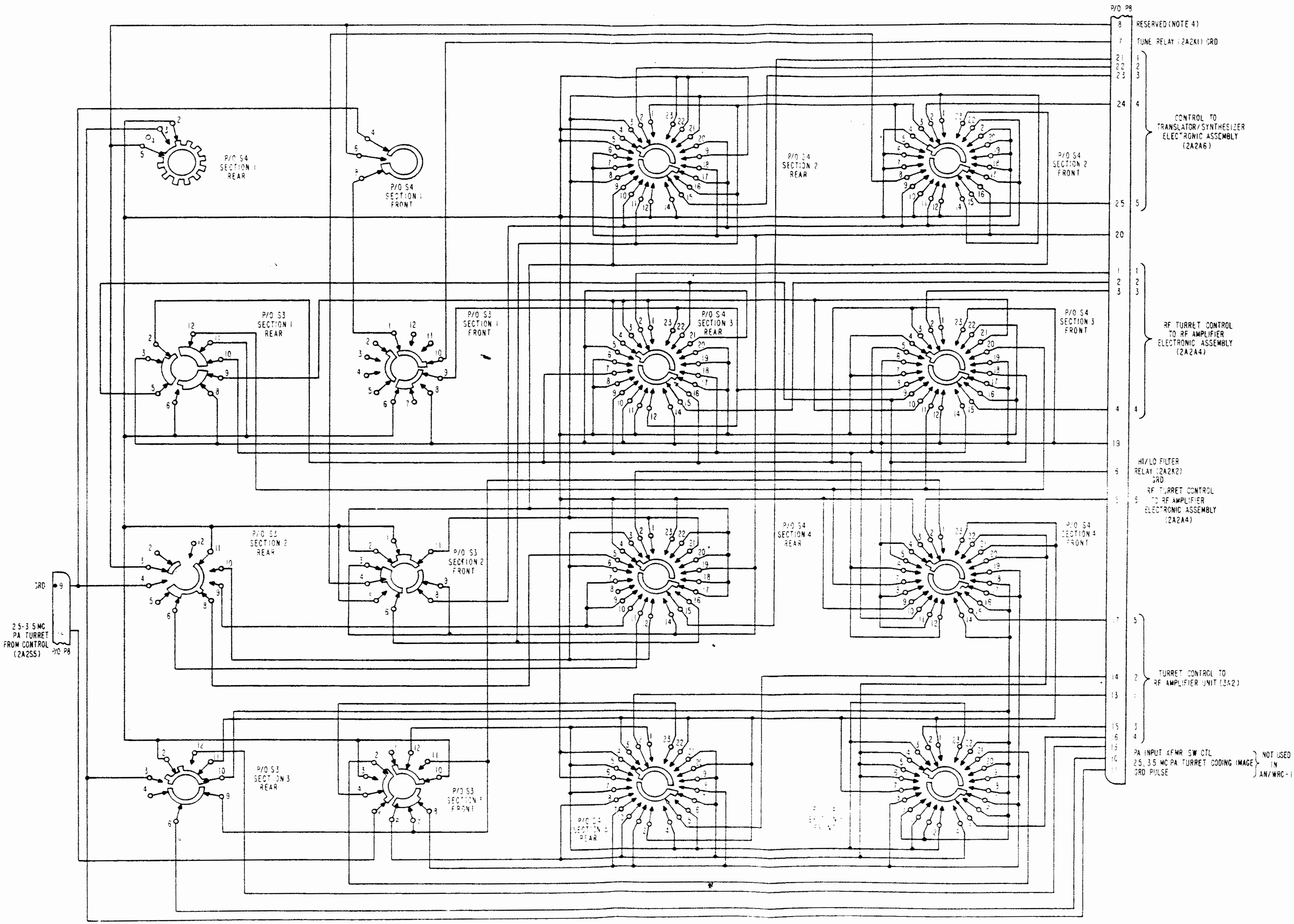


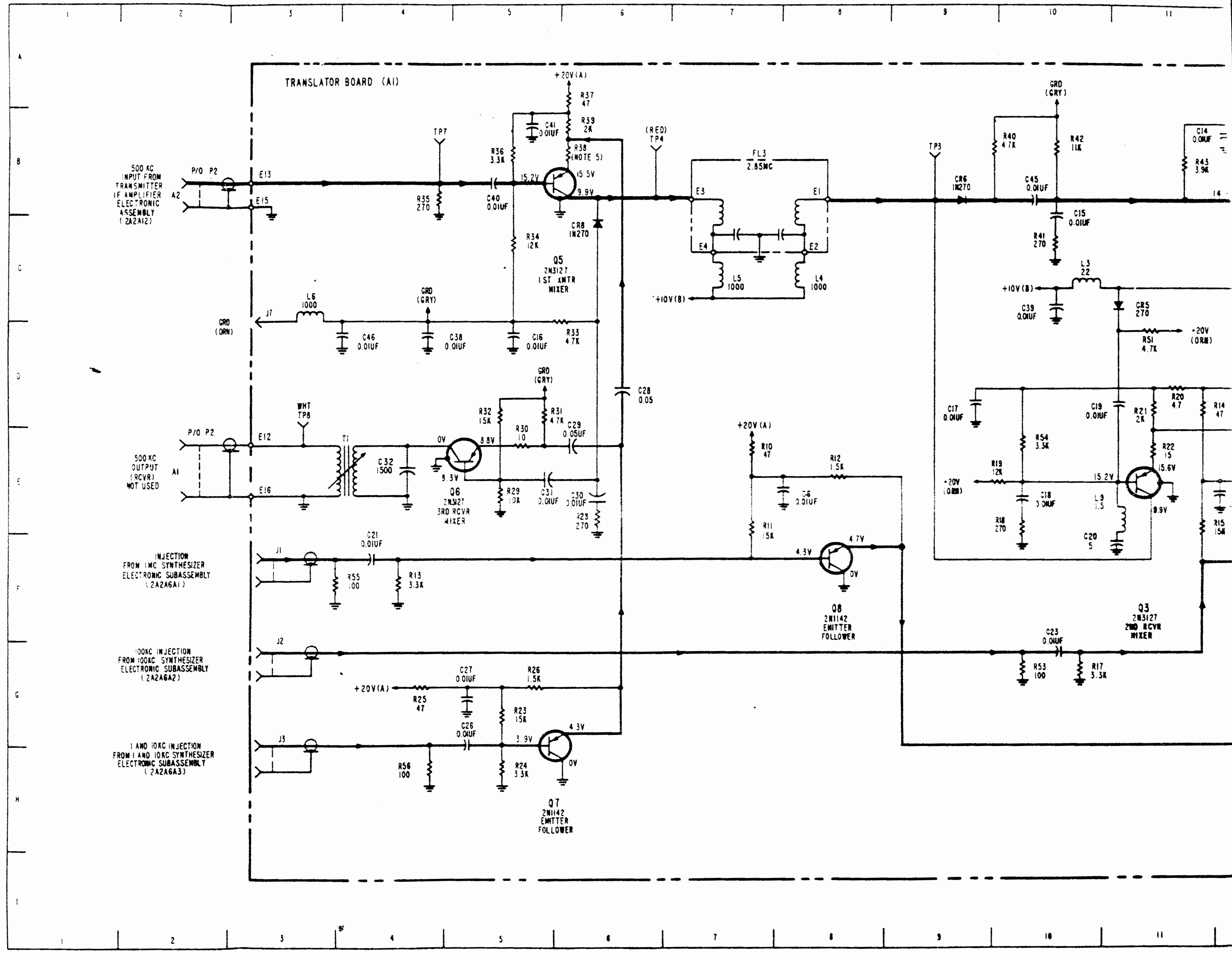
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH 2A2A7
2. SWITCH SECTIONS VIEWS ARE SHOWN FROM THE REAR AND ARE IN 00 MC POSITION.
3. ROTATION IN ALL VIEWS IS CCW IN 30 DEGREE THROWS TO MAXIMUM POSITION OF 29MC.
4. OPERATE GRD LINE IS DISABLED IN POSITIONS 00 AND 01 MC, NOT USED IN AN/WRC-1

Figure 5-16. Code Generator Electronic Assembly, Schematic Diagram

PART LOCATION INDEX

LOC	REF DESIG	LOC	REF DESIG	LOC
18B	A1CR4	13B	A1R15	11E
17C	A1CR5	11C	A1R16	12E
17B	A1CR6	9B	A1R17	10G
14F	A1CR7	13C	A1R18	10E
17F	A1CR8	6C	A1R19	10E
8E	A1CR9	18E	A1R20	11D
16G	A1CR10	17E	A1R21	11D
15G	A1CR11	16H	A1R22	11E
14B	A1FL1	14B	A1R23	5G
14C	A1FL2	14C	A1R24	5H
13B	A1FL3	7B	A1R25	4G
13C	A1J1	3F	A1R26	5G
18D	A1J2	3G	A1R27	16H
11B	A1J3	3G	A1R28	6E
10B	A1J4	18D	A1R29	5E
5D	A1J5	18B	A1R30	5E
9D	A1J6	18H	A1R31	5D
10E	A1J7	23C	A1R32	5D
11D	A1L1	18D	A1R33	5C
11F	A1L2	16E	A1R34	5C
4F	A1L3	10C	A1R35	4B
11E	A1L4	8C	A1R36	5B
10G	A1L5	7C	A1R37	6A
12D	A1L6	3C	A1R38	6B
12E	A1L7	18B	A1R39	6B
5G	A1L8	18H	A1R40	9B
5G	A1L9	11E	A1R41	10C
6D	A1P2	2B, 2E	A1R42	10B
6E	A1P3	19B, 19F, 19H	A1R43	11B
6E	A1Q1	17B	A1R44	12A
5E	A1Q2	16E	A1R45	12B
4E	A1Q3	11E	A1R46	12B
17H	A1Q4	12B	A1R47	13C
17H	A1Q5	5B	A1R48	14C
17H	A1Q6	5E	A1R49	14C
17H	A1Q7	5G	A1R50	13C
18B	A1Q8	8F	A1R51	11D
4D	A1Q9	12F	A1R52	18F
10C	A1R1	18B	A1R53	10G
5B	A1R2	17B	A1R54	10E
5B	A1R3	17C	A1R55	3F
17D	A1R4	17F	A1R56	4H
17D	A1R5	17F	A1T1	4E
10B	A1R6	14E	A1TP1	16B
3D	A1R7	15E	A1TP2	12B
17B	A1R8	14E	A1TP3	9B
16C	A1R9	15F	A1TP4	6B
16B	A1R10	7E	A1TP5	18B
	A1R11	7E	A1TP6	18B
	A1R12	8E	A1TP7	4B
	A1R13	4F	A1TP8	3E
	A1R14	11D		



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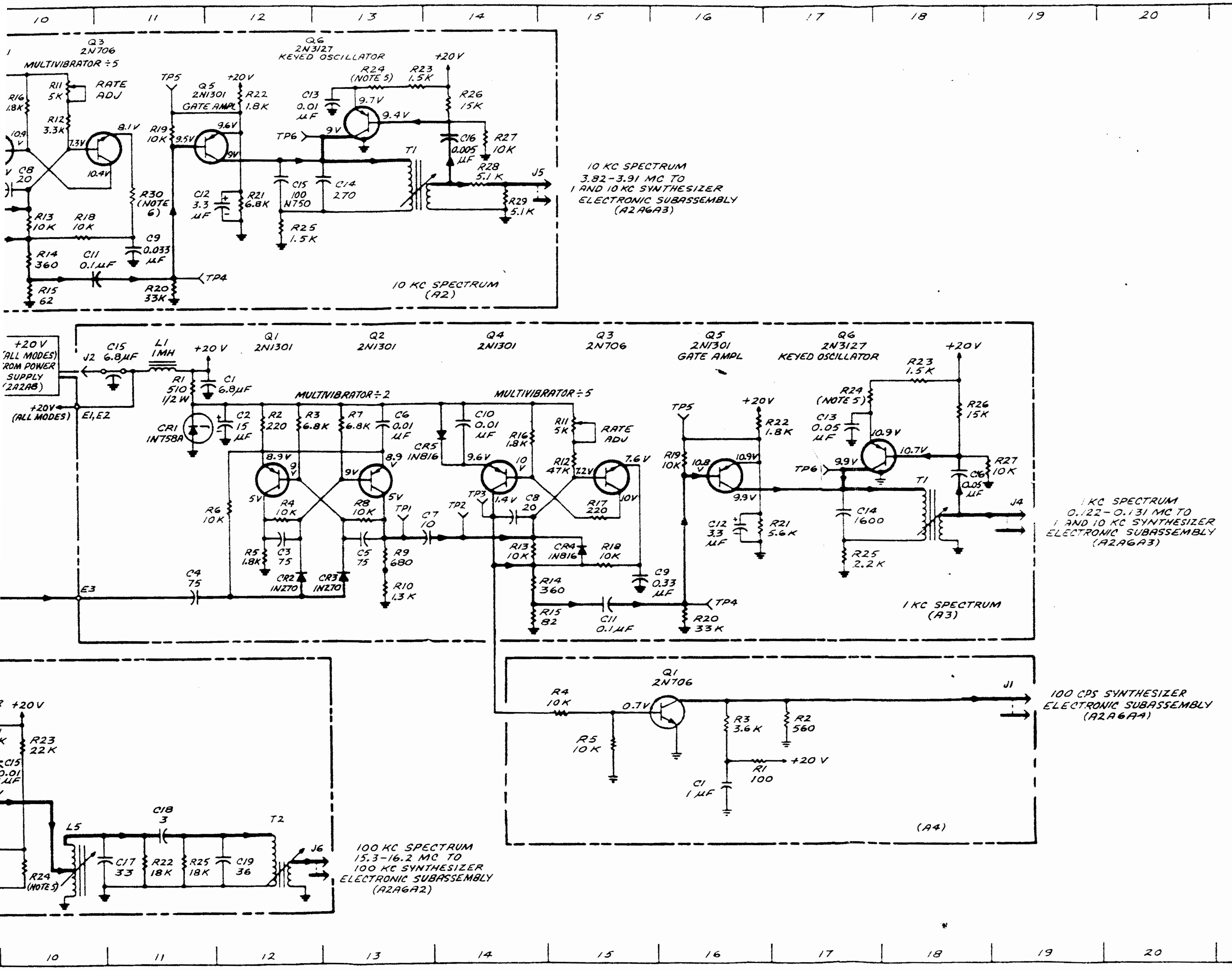
PART LOCATION INDEX

REF DESIG	LOC
A1C1	18B
A1C2	17C
A1C3	17B
A1C4	14F
A1C5	17F
A1C6	8E
A1C7	16G
A1C8	15G
A1C9	14B
A1C10	14C
A1C11	13B
A1C12	13C
A1C13	18D
A1C14	11B
A1C15	10B
A1C16	5D
A1C17	9D
A1C18	10E
A1C19	11D
A1C20	11F
A1C21	4F
A1C22	11E
A1C23	10G
A1C24	12D
A1C25	12E
A1C26	5G
A1C27	5G
A1C28	6D
A1C29	6E
A1C30	6E
A1C31	5E
A1C32	4E
A1C33	17H
A1C34	17H
A1C35	17H
A1C36	17H
A1C37	18B
A1C38	4D
A1C39	10C
A1C40	5B
A1C41	5B
A1C42	17D
A1C43	17D
A1C45	10B
A1C46	3D
A1CR1	17B
A1CR2	16C
A1CR3	16B

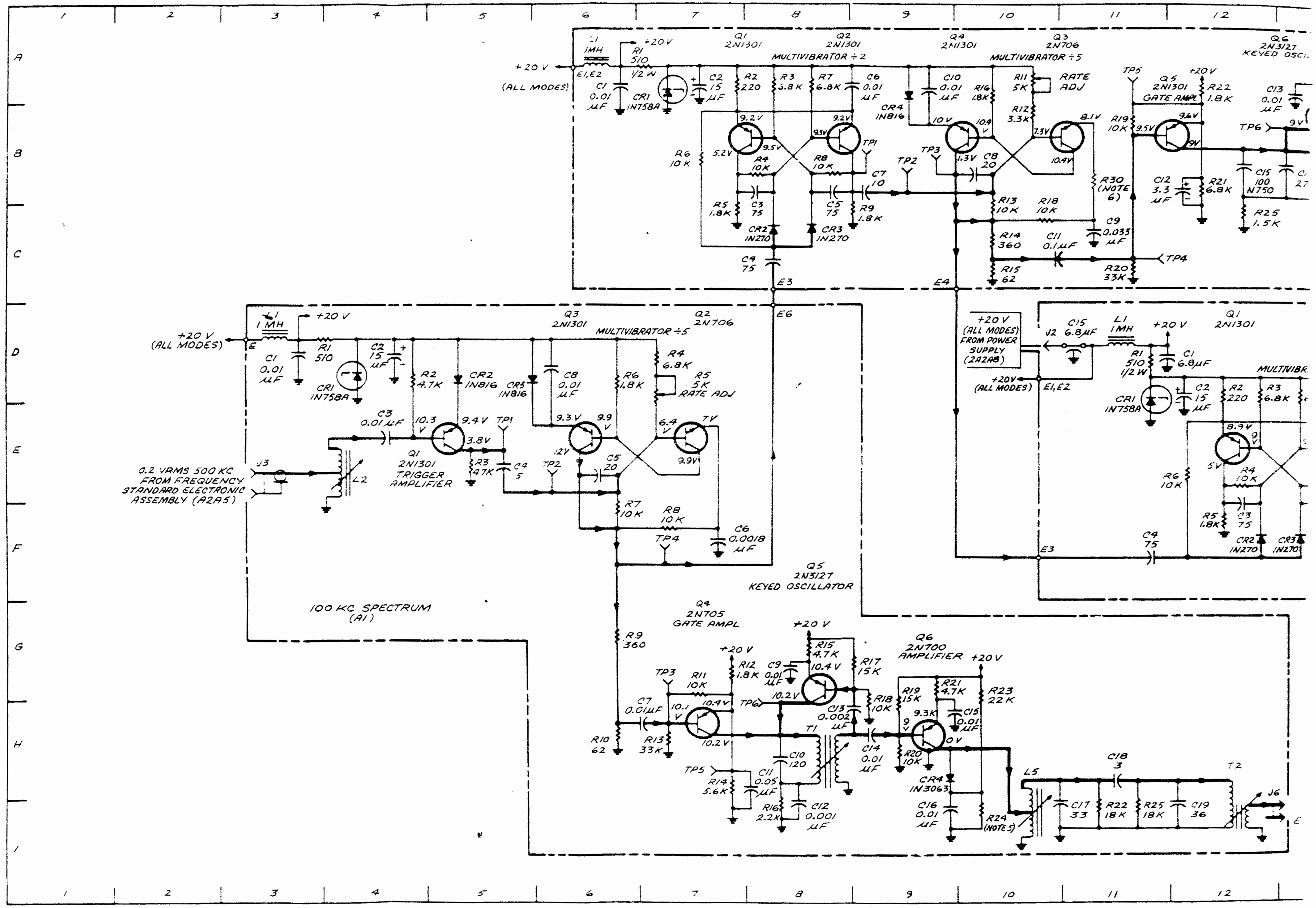
REF DESIG	LOC
A1CR4	13B
A1CR5	11C
A1CR6	9B
A1CR7	13C
A1CR8	6C
A1CR9	18E
A1CR10	17E
A1CR11	16H
A1FL1	14B
A1FL2	14C
A1FL3	7B
A1J1	3F
A1J2	3G
A1J3	3G
A1J4	18D
A1J5	18B
A1J6	18H
A1J7	23C
A1L1	18D
A1L2	16E
A1L3	10C
A1L4	8C
A1L5	7C
A1L6	3C
A1L7	18B
A1L8	18H
A1L9	11E
A1P2	2B, 2E
A1P3	19B, 19
A1Q1	17B
A1Q2	15E
A1Q3	11E
A1Q4	12B
A1Q5	5B
A1Q6	5E
A1Q7	5G
A1Q8	8F
A1Q9	12F
A1R1	18B
A1R2	17B
A1R3	17C
A1R4	17F
A1R5	17F
A1R6	14E
A1R7	15E
A1R8	14E
A1R9	15F
A1R10	7E
A1R11	7E
A1R12	8E
A1R13	4F
A1R14	11D



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH A2A6A5.
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTANCE VALUES ARE IN OHMS, K=INDICATES THOUSANDS OF OHMS.
   b. ALL RESISTORS ARE 1/4 WATT, ±5% TOL.
   c. ALL CAPACITANCE VALUES ARE IN PICOFARADS, μF INDICATES MICROFARADS.
3. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4.
4. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATIONS FOR TRANSFORMER CIRCUIT ORIENTATION.
5. R11 AND R24 SELECTED AT ASSEMBLY.
6. R30-VALUE BETWEEN 5.1 AND 47 OHMS.

Figure 5-10. Spectrum Generator Electronic Subassembly, Schematic Diagram



+20 V
(ALL MODES)
L1 1MH
E1, E2
R1 510 1/2 W
C1 0.01 µF
CR1 1N758A
C2 15 µF
Q1 2N1301
Q2 2N1301
MULTIVIBRATOR ÷ 2
Q4 2N1301
Q3 2N706
MULTIVIBRATOR ÷ 5
R11 5K RATE ADJ
Q5 2N1301 GATE AMPL
Q6 2N3127 KEYED OSC
TP1
TP2
TP3
TP4
TP5
TP6
E3
E4
E6
+20 V (ALL MODES) FROM POWER SUPPLY (2A2A8)
J2
C15 6.8 µF
MULTIVIBR
0.2 VRMS 500 KC FROM FREQUENCY STANDARD ELECTRONIC ASSEMBLY (A2A5)
J3
L2
Q1 2N1301 TRIGGER AMPLIFIER
Q3 2N1301
Q2 2N706
MULTIVIBRATOR ÷ 5
R5 5K RATE ADJ
100 KC SPECTRUM (A1)
Q5 2N3127 KEYED OSCILLATOR
Q4 2N705 GATE AMPL
Q6 2N700 AMPLIFIER
T1
T2
L5
J6
CR4 1N3063
R24 (NOTE 5)
R30 (NOTE 6)

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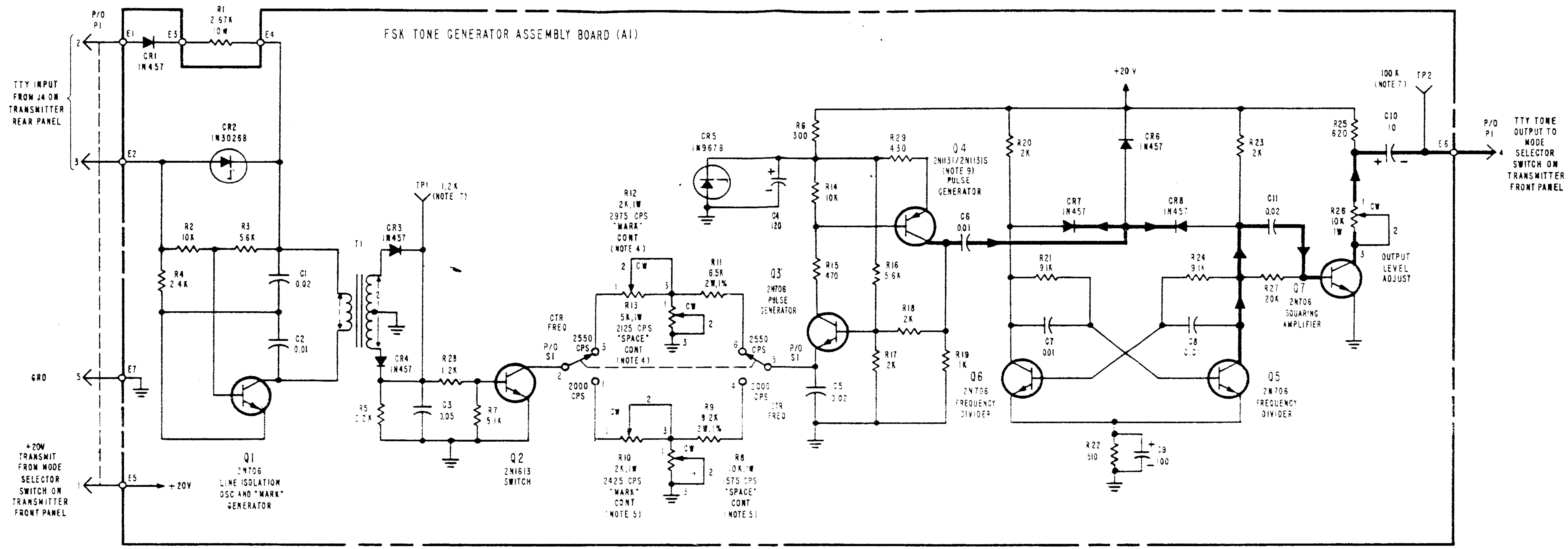

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH 2A2A9
2. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTANCE VALUES ARE IN OHMS. K - INDICATES THOUSANDS OF OHMS.
   B. ALL RESISTORS ARE 1/4 WATT, ±5% TOL
   C. ALL CAPACITANCE VALUES ARE IN MICROFARADS
3. CW ON ALL POTENTIOMETERS INDICATE DIRECTION OF ROTATION WHEN VIEWED FROM SHAFT END.
4. A1R12 ADJUSTED FOR 2550 CPS CENTER FREQ "MARK" (2975 CPS)
   A1R13 ADJUSTED FOR 2550 CPS CENTER FREQ "SPACE" (2125 CPS)
5. A1R10 ADJUSTED FOR 2000 CPS CENTER FREQ "MARK" (2425 CPS)
   A1R8 ADJUSTED FOR 2000 CPS CENTER FREQ "SPACE" (1575 CPS)
6. NUMBERS ADJACENT TO WINDINGS AND TEST POINTS INDICATE DC RESISTANCE
7. RESISTANCE VALUES AT SIGNIFICANT TEST POINTS ARE TO CHASSIS WITH ALL UNITS INTERCONNECTED, BUT EQUIPMENT DE-ENERGIZED
8. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATION FOR TRANSFORMER CIRCUIT ORIENTATION
9. Q4 IS REPLACED WITH 2N1131 OR 2N1131S REPLACEMENT TRANSISTOR MUST HAVE FOLLOWING PARAMETERS:
   f [illegible] 1KC/S V_{CE} [illegible]0V DC
   I_c 2MADC h_{fe} < 42

Figure 5-17. FSK Tone Generator Electronic Assembly, Schematic Diagram

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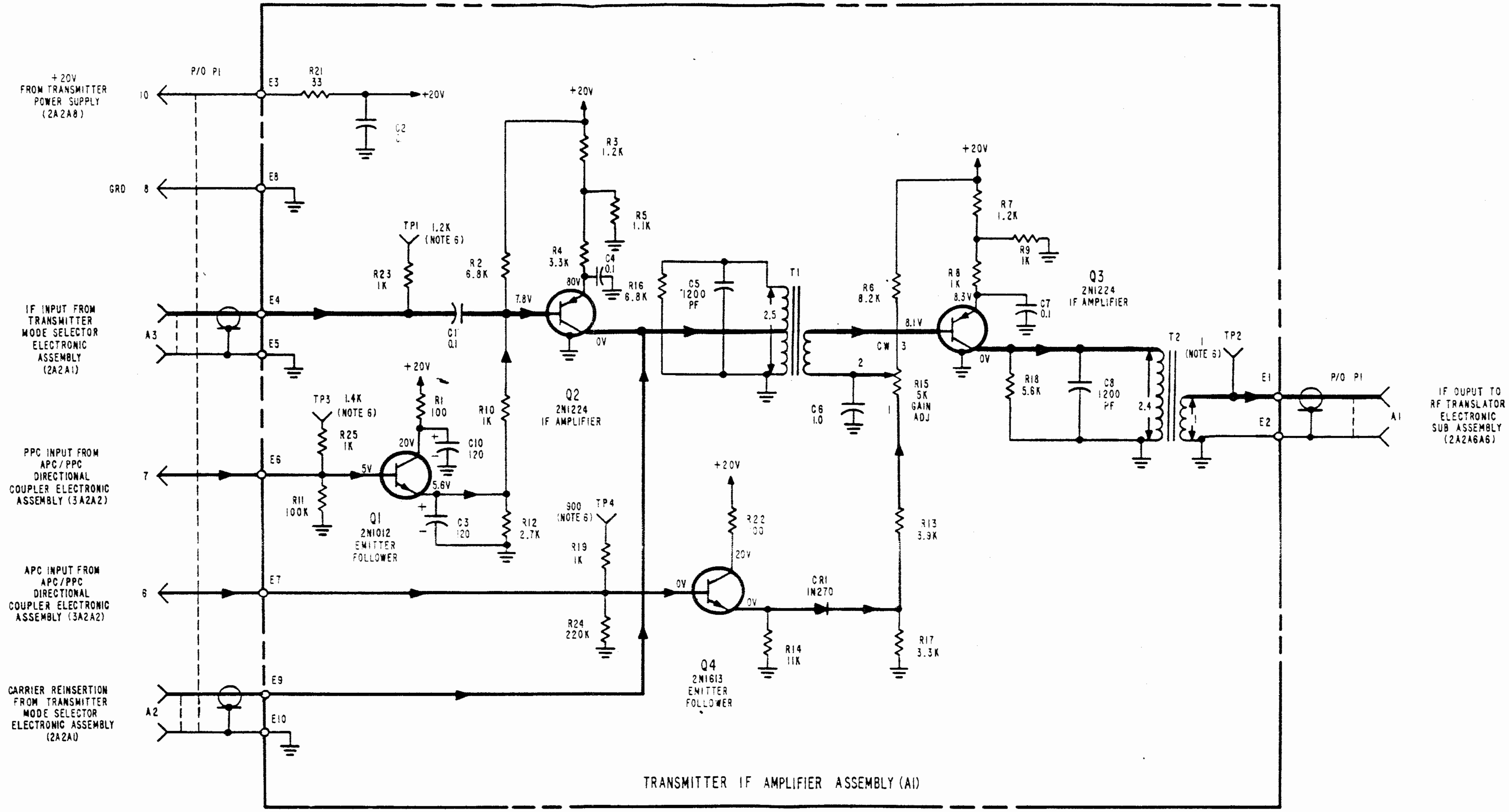

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH 2A2A12.
2. UNLESS OTHERWISE SPECIFIED:
   a- ALL RESISTANCE VALUES ARE IN OHMS K-INDICATES THOUSANDS OF OHMS.
   b- ALL RESISTORS ARE 1/4 WATT, ±5% TOL.
   c- ALL CAPACITANCE VALUES ARE IN MICROFARADS, PF INDICATES PICOFARADS.
3. NUMBERS ADJACENT TO WINDINGS AND TEST POINTS INDICATE DC RESISTANCE (VALUES LESS THAN ONE OHM ARE NOT SHOWN).
4. CW ON ALL POTENTIOMETERS INDICATE DIRECTION OF ROTATION WHEN VIEWED FROM SHAFT END.
5. UNLESS OTHERWISE INDICATED ALL VOLTAGES ARE DC TAKEN WITH MULTIMETER AN/PSM-4
6. RESISTANCE VALUES AT SIGNIFICANT TEST POINTS ARE TO CHASSIS WITH ALL UNITS INTERCONNECTED, BUT EQUIPMENT DE-ENERGIZED.
7. REFER TO APPLICABLE PRINTED CIRCUIT BOARD ILLUSTRATION FOR TRANSFORMER CIRCUIT ORIENTATION.

Figure 5-18. Transmitter IF. Amplifier Electronic Assembly, Schematic Diagram

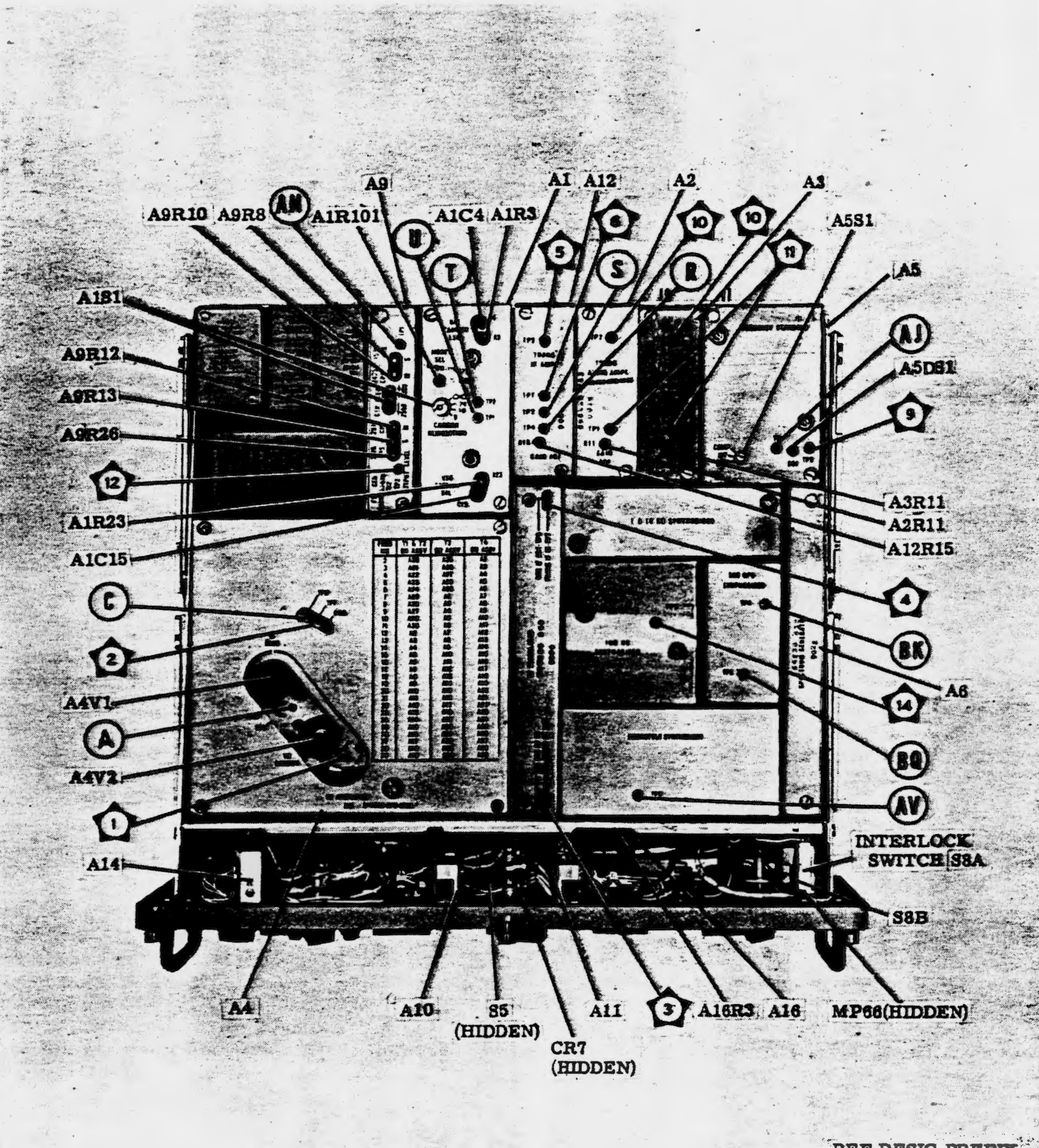

Figure 5-24. Radio Transmitter T-827/URT, Top View, Case Removed, Component and Test Point Location

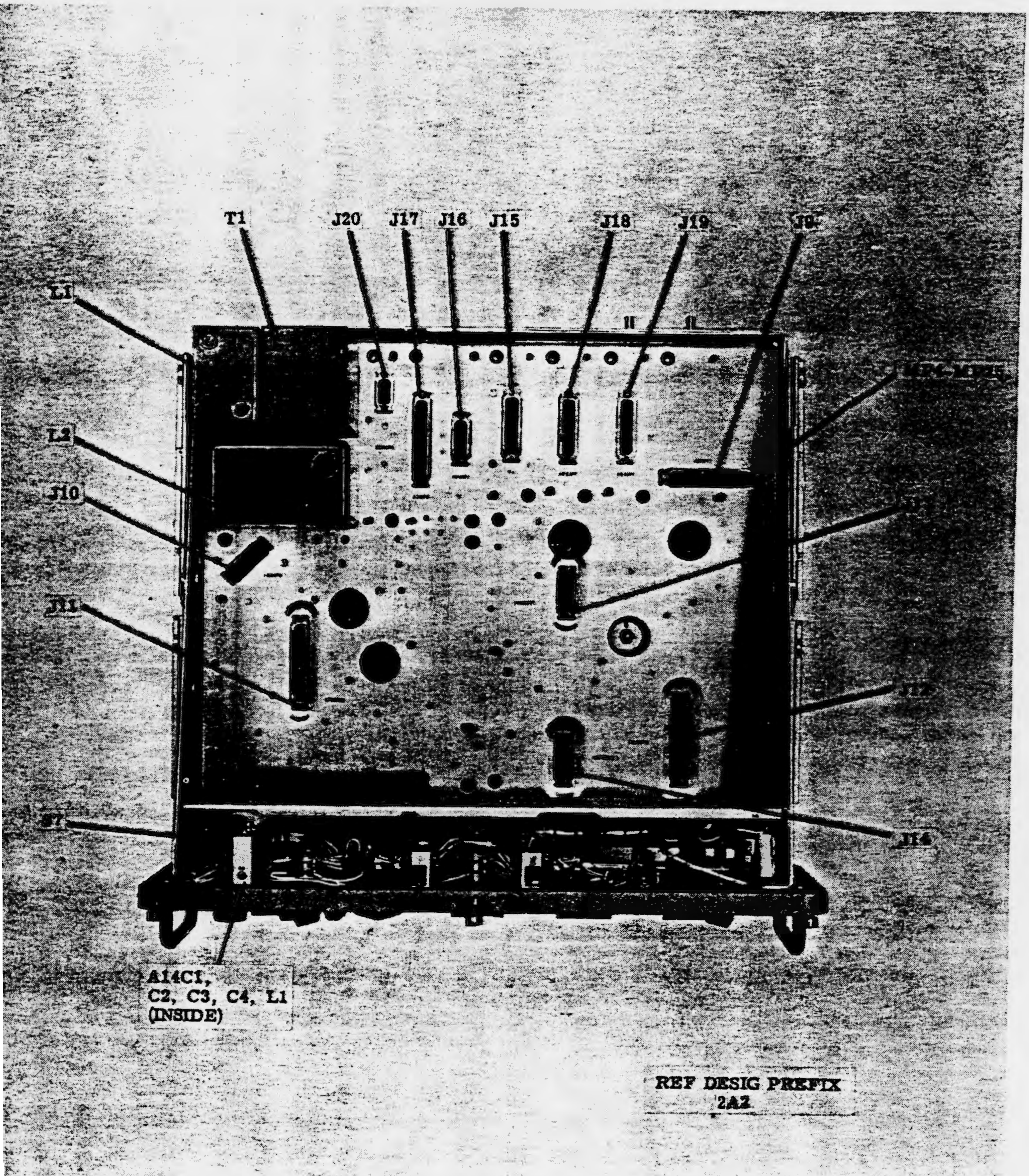

Figure 5-25. Radio Transmitter T-827 URT, Chassis, Top View

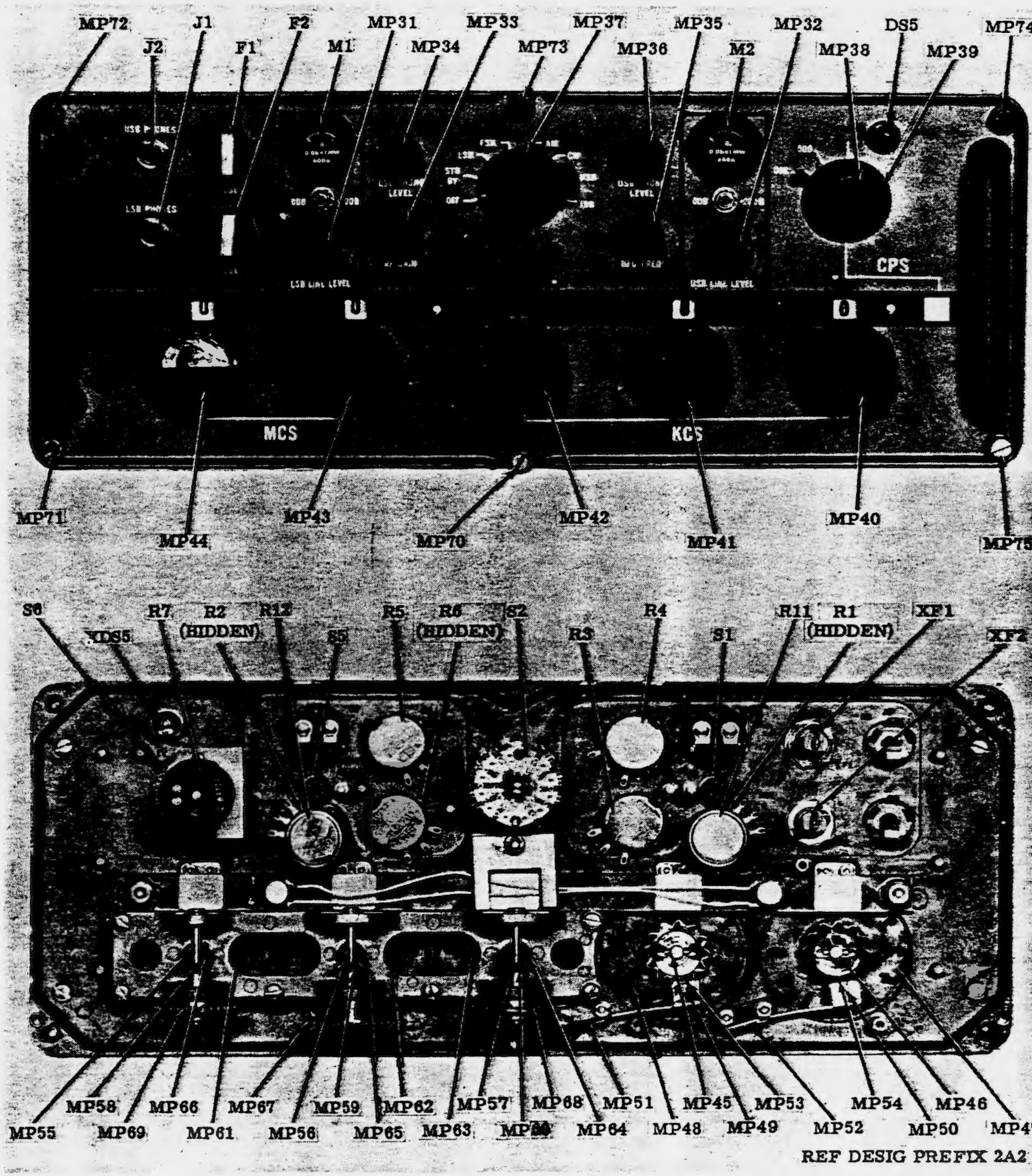

Figure 5-25a. Radio Transmitter T-827 URT, Front Panel Assembly, Component Location

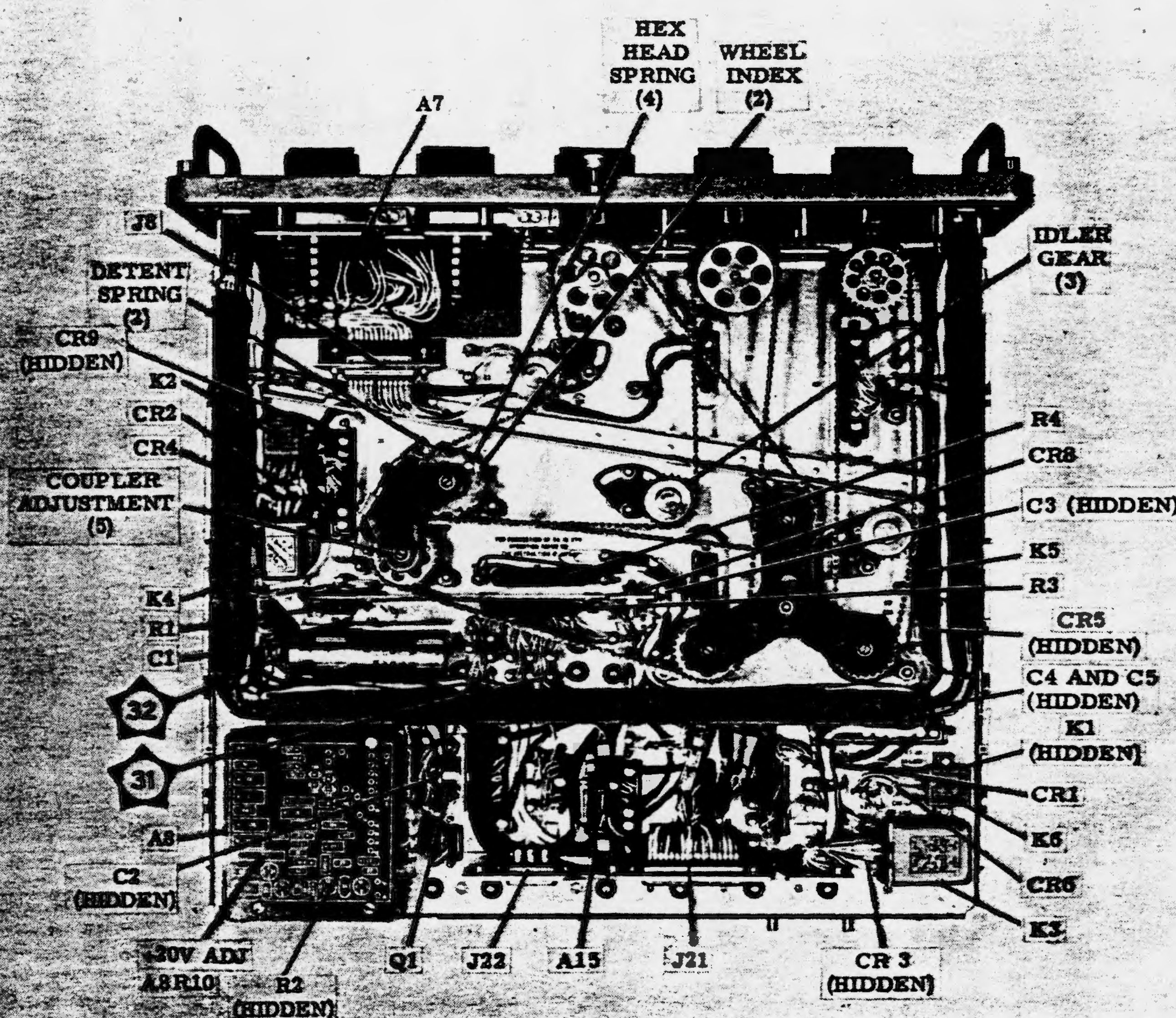

Figure 5-26. Radio Transmitter T-827/URT, Bottom View, Component and Test Point Location (Sheet 1 of 2)

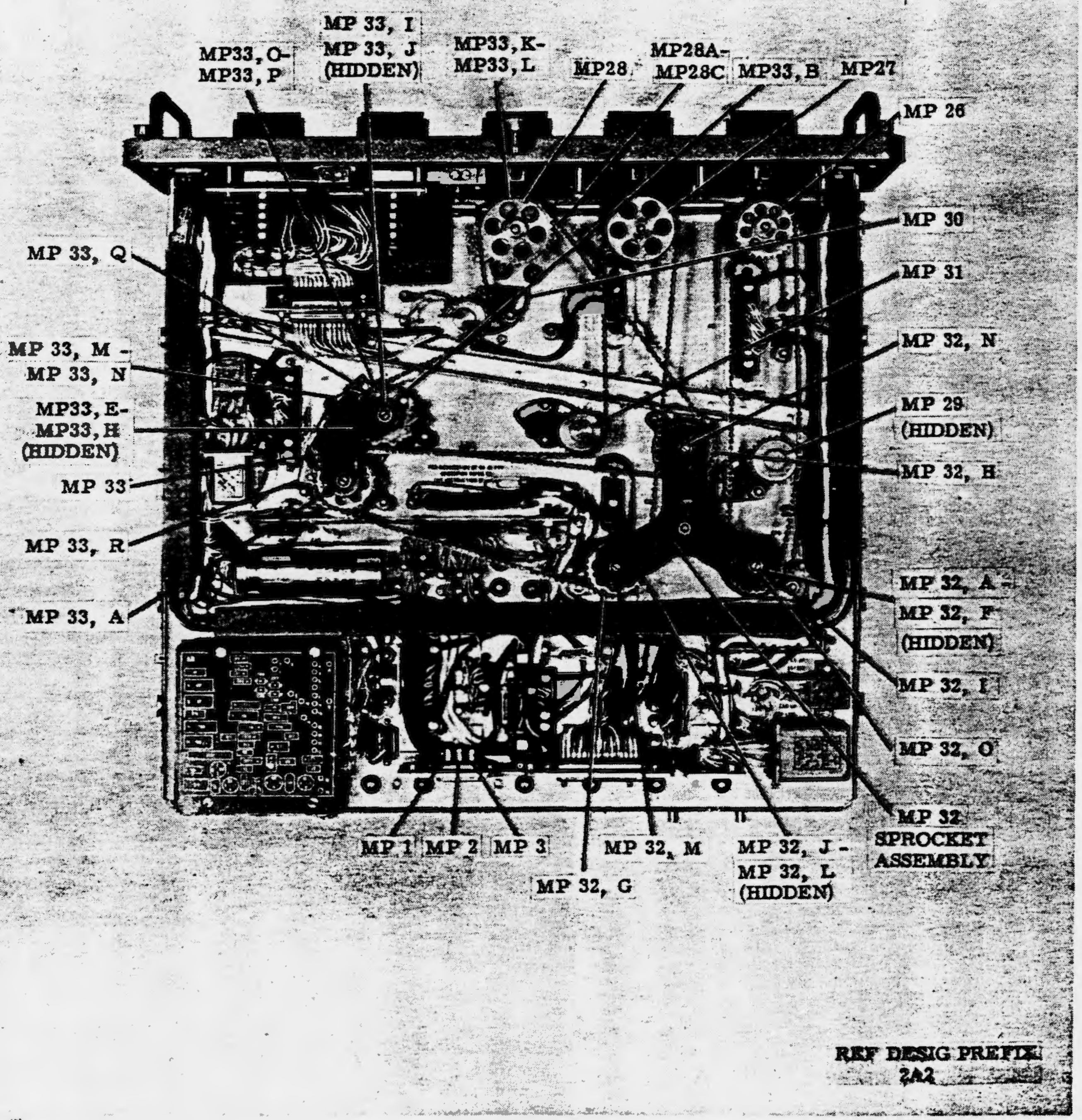

Figure 5-26. Radio Transmitter T-827/URT, Bottom View, Component and Test Point Location (Sheet 2 of 2)

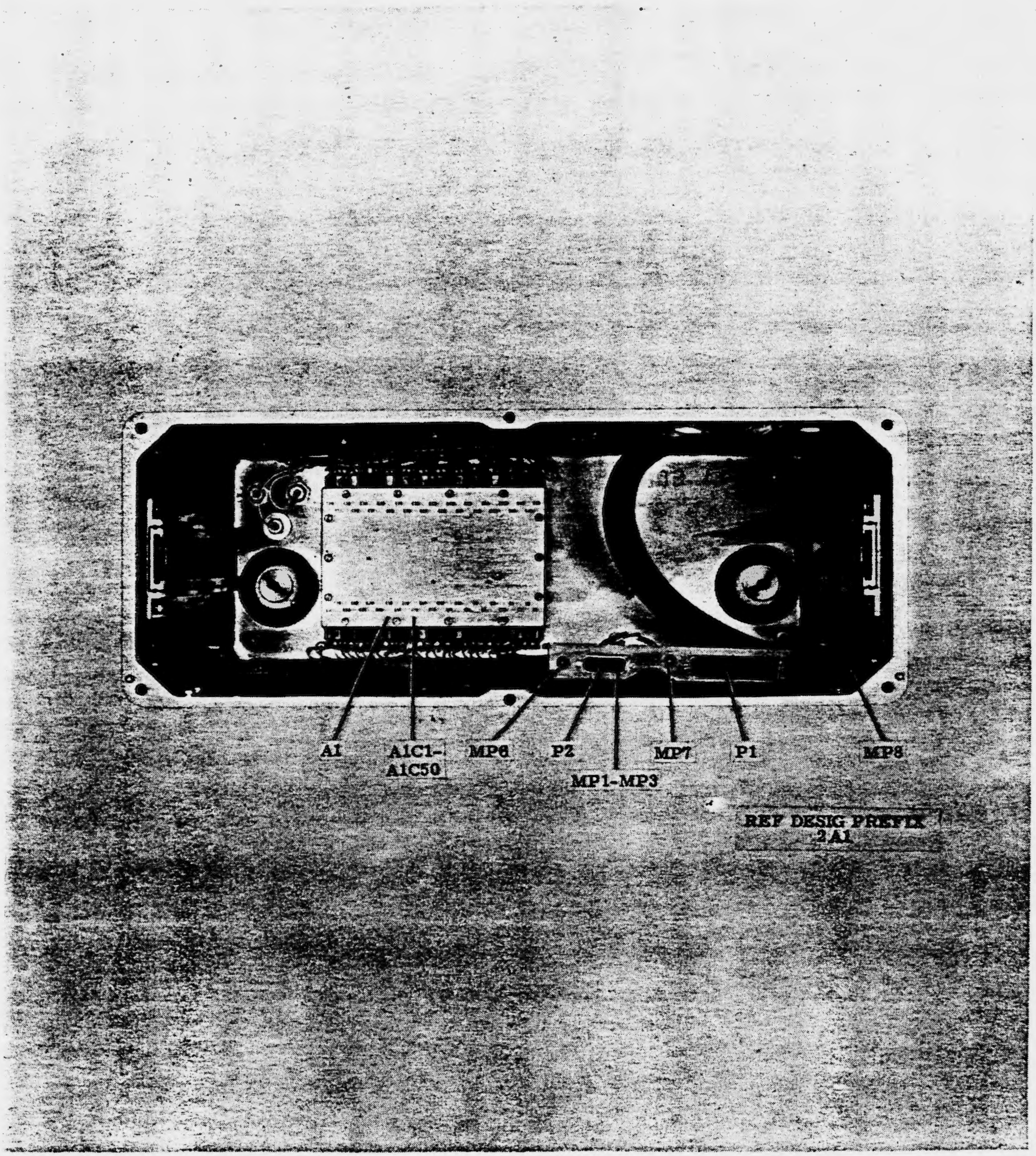

Figure 5-27. Radio Transmitter T-827/URT, Case, Inside View, Component Location

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NOTE:
REF. DESIG. PREFIX 2A2.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	5B	CR12	8E	E21	2H
C2	4B	CR13	8D	Q1	9F
C3	8G	E1	2F	Q2	9E
C4	9E	E2	2F	Q3	9C
C5	8B	E3	2F	Q4	8C
C6	7B	E4	2G	R1	3B
C7	7F	E5	3G	R2	8G
C8	6D	E6	3G	R3	8F
C9	6D	E7	4G	R4	9D
C10	6B	E8	4G	R5	8D
C11	5D	E9	5F	R6	9D
CR1	2E	E10	5G	R7	9C
CR2	2E	E11	5G	R8	8D
CR3	2E	E12	5H	R9	8A
CR4	2E	E13	6G	R10	7B
CR5	4F	E14	6G	R11	7C
CR6	4E	E15	6G	R12	7D
CR7	4F	E16	7G	R13	7G
CR8	3E	E17	7G	R14	6F
CR9	5F	E18	8G	R15	6F
CR10	7D	E19	9H	R16	5B
CR11	9D	E20	9H		

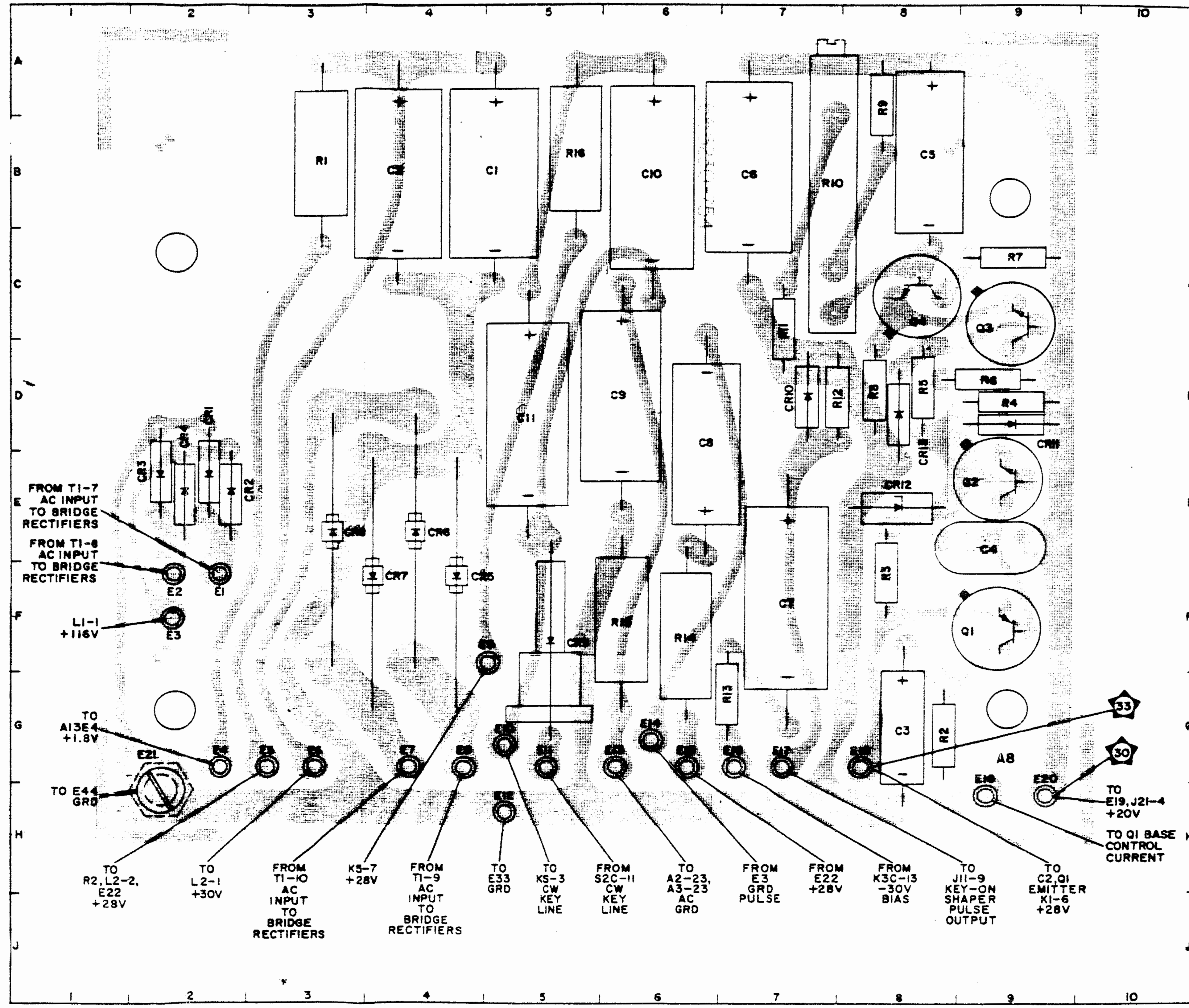
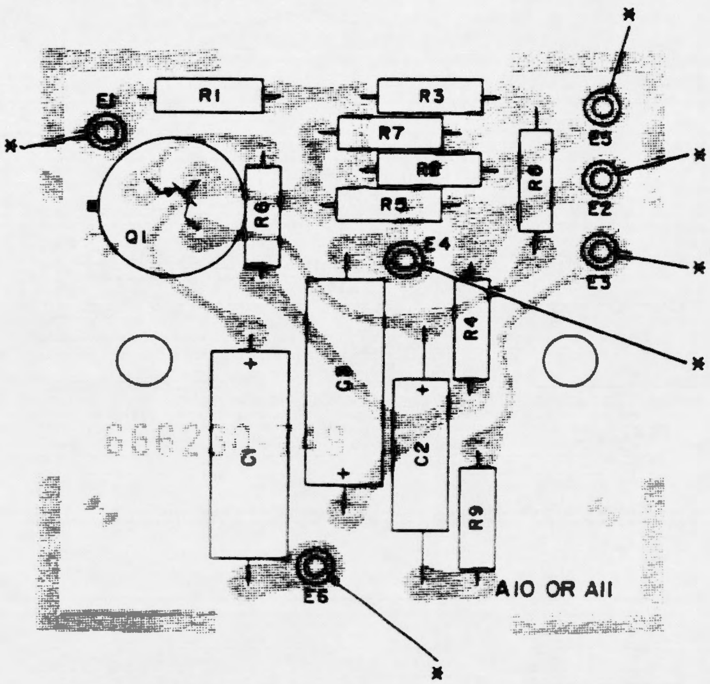


Figure 5-29. Transmitter Power Supply (Foil Side Up), Component and Test Point Location



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NOTES:
1. REF. DESIG. PREFIX 2A2.
2. * REFER TO TABLE BELOW FOR THESE CONNECTIONS

A10	ORIGIN/DESTINATION	A11	ORIGIN/DESTINATION
E1	LSB AUDIO OUTPUT TO S10-6	E1	USB AUDIO OUTPUT TO S11-6
E2	+20V FROM A8	E2	+20V FROM A8
E3	OUTPUT TO M1-1, 0.744VRMS FOR METER FULL SCALE DEFLECTION.	E3	OUTPUT TO M2-1, 0.744VRMS FOR METER FULL SCALE DEFLECTION
E4	TO E40 GROUND	E4	TO E37 GROUND
E5	LSB AUDIO INPUT FROM S10-1	E5	USB AUDIO INPUT FROM S11-1
E6	LSB AUDIO INPUT FROM S10-3	E6	USB AUDIO INPUT FROM S11-3

Figure 5-30. Meter Amplifier (Foil Side Up), Component Location

TE:
REF. DESIG. PREFIX 2A2.

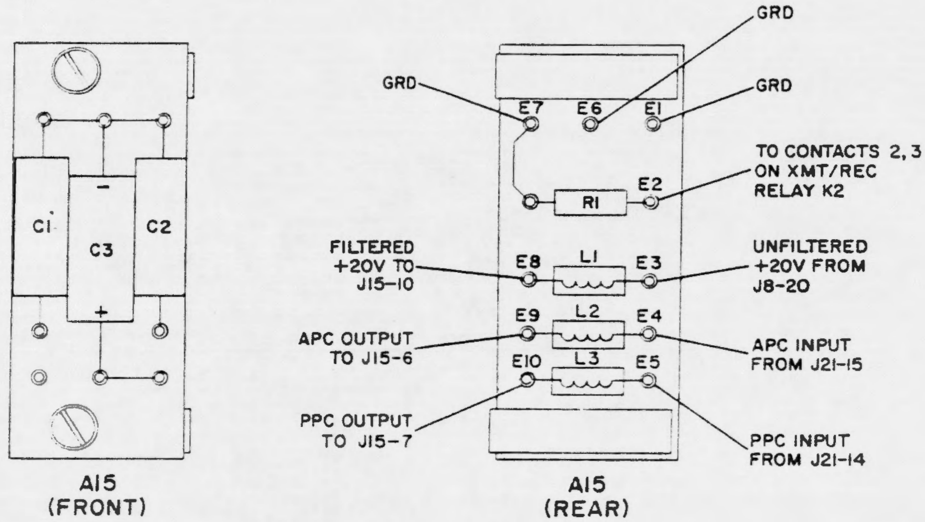
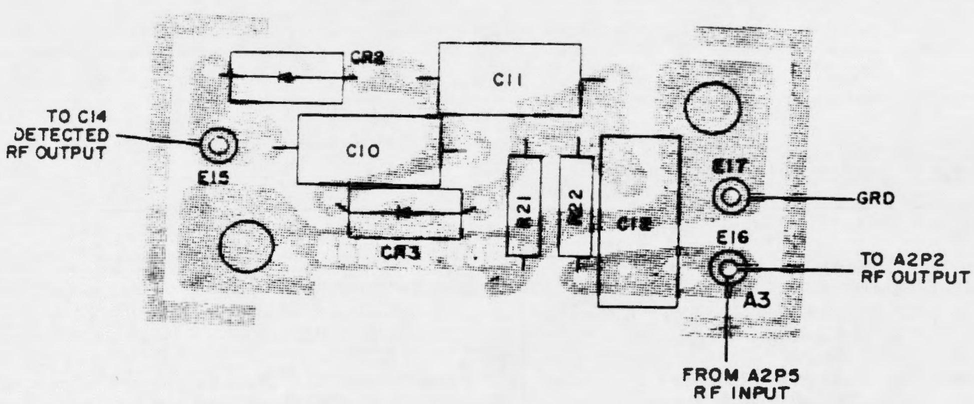


Figure 5-31. Transmitter IF. Filter (Foil Side Up), Component Location



NOTE:
REF. DESIG. PREFIX 3A2A2.

Figure 5-32. Transmitter 500 CPS Control (Foil Side Up), Component Location

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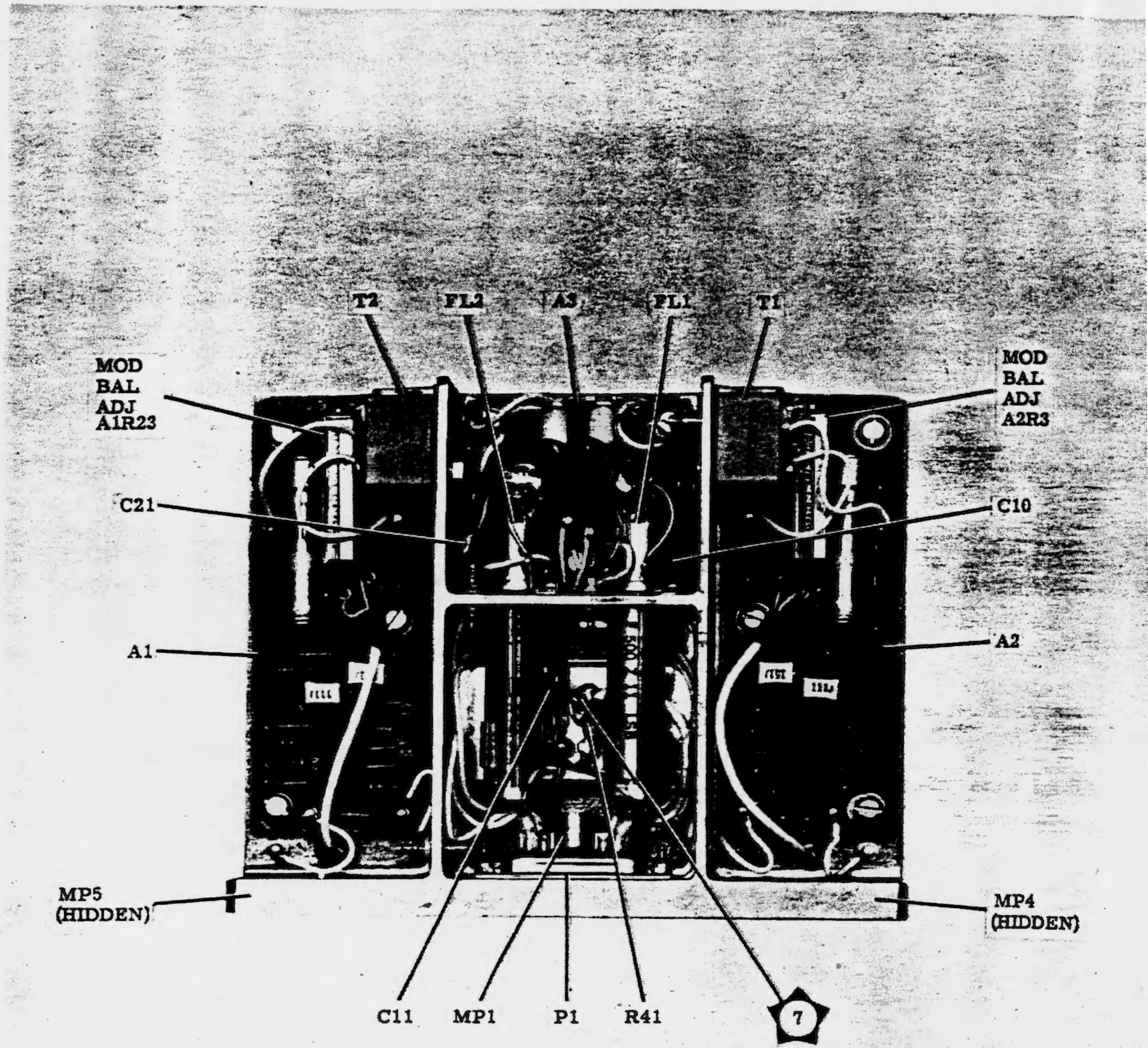
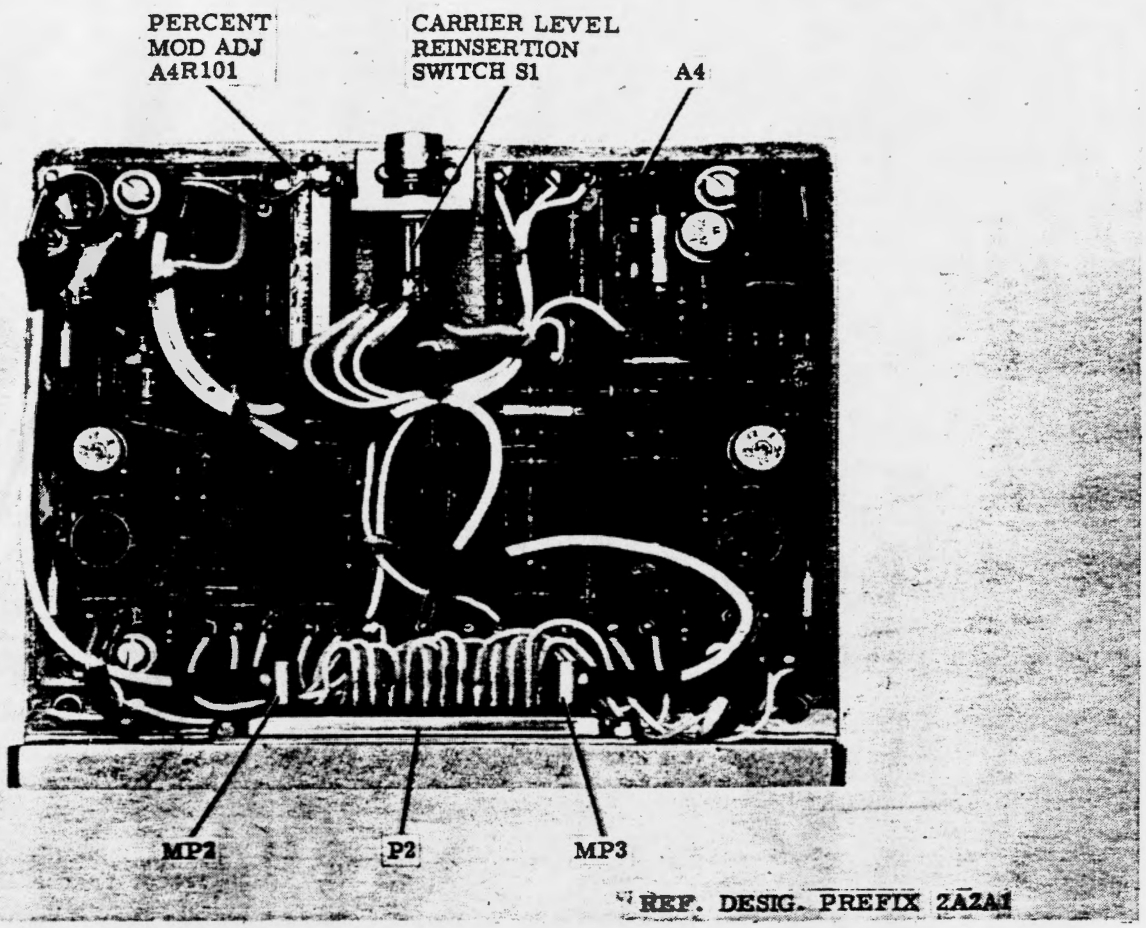


REF. DESIG. PREFIX 2A2A1

Figure 5-33. Transmitter Mode Selector Electronic Assembly, Right Side, Component Location



ure 5-34. Transmitter Mode Selector Electronic Assembly, Left Side, Component Location

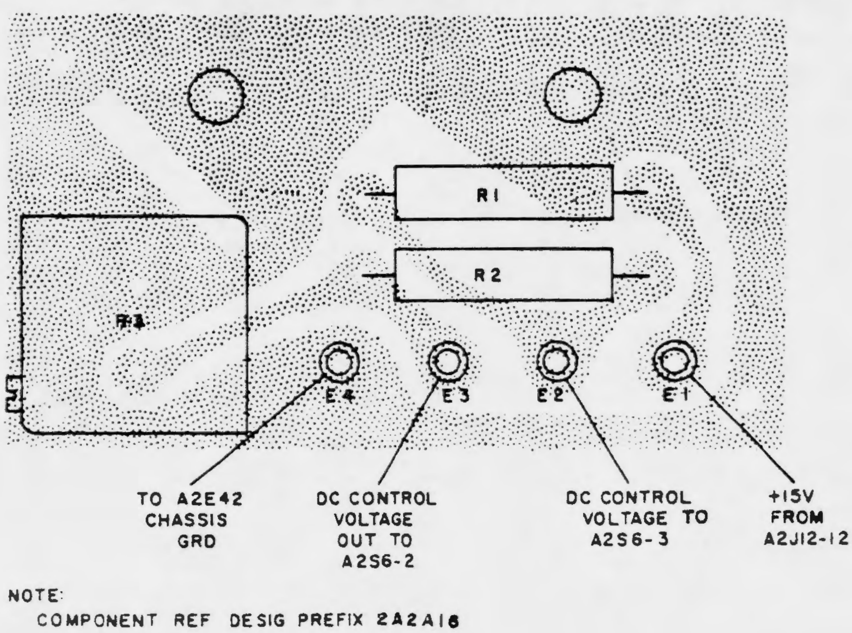


Figure 5-35. Transmitter 500 CPS Control (Foil Side Up), Component Location

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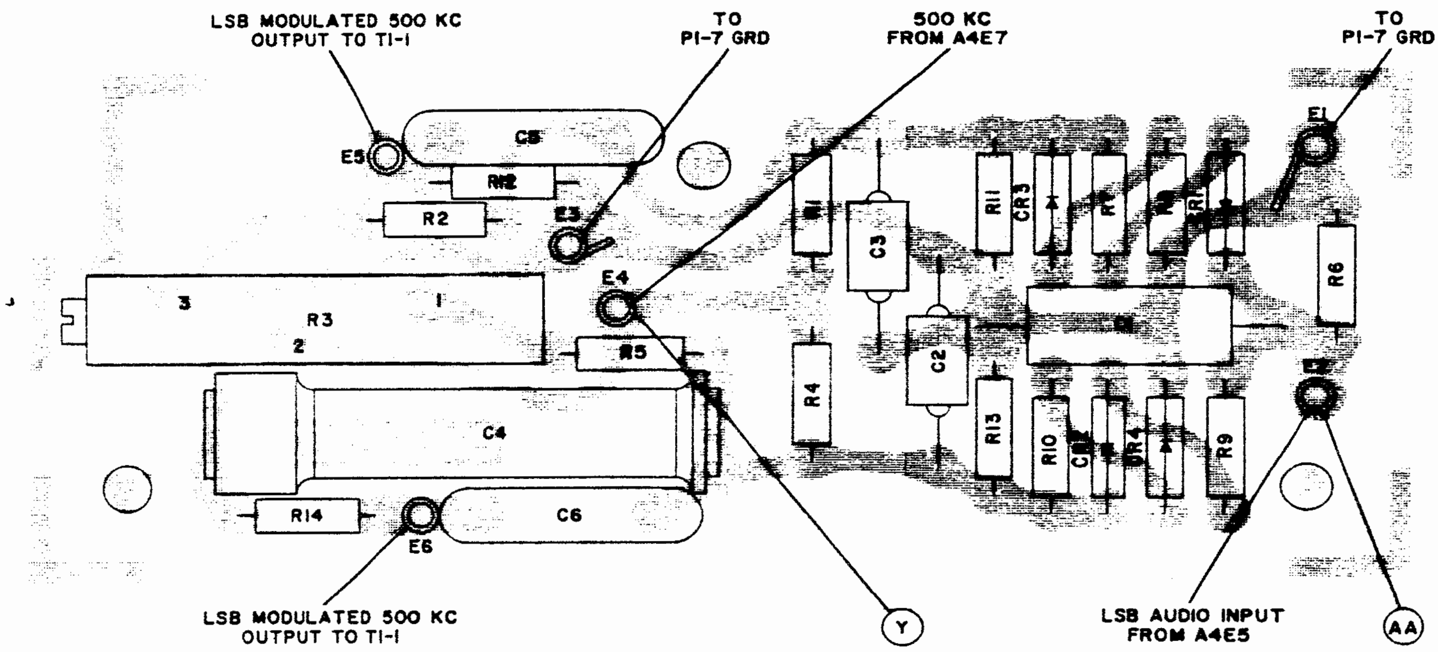
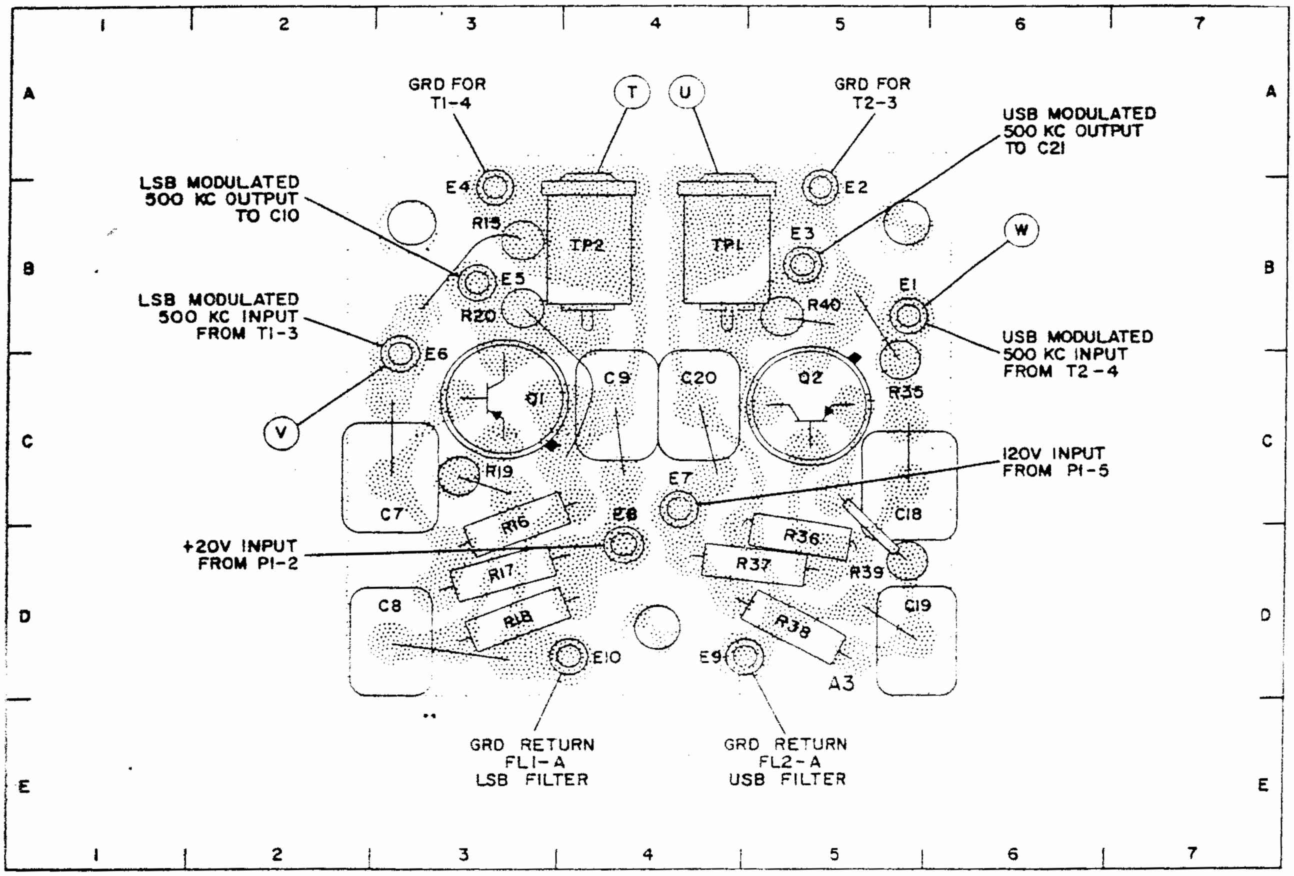


NOTE:
REF. DESIG. PREFIX 2A2A1.

Figure 5-36. LSB Balanced Modulator (Foil Side Up), Component and Test Point Location



NOTE:
REF. DESIG. PREFIX 2A2A1.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C7	3C	E3	5B	Q1	3C	R35	5C
C8	3D	E4	3B	Q2	5C	R36	5D
C9	4C	E5	3B	R15	3B	R37	5D
C18	6C	E6	3C	R16	3D	R38	5D
C19	6D	E7	4C	R17	3D	R39	5D
C20	4C	E8	4D	R18	3D	R40	5B
E1	5B	E9	5D	R19	3C	TP1	4B
E2	5B	E10	4D	R20	3B	TP2	4B

Figure 5-37. Isolation Amplifiers (Foil Side Up), Component and Test Point Location

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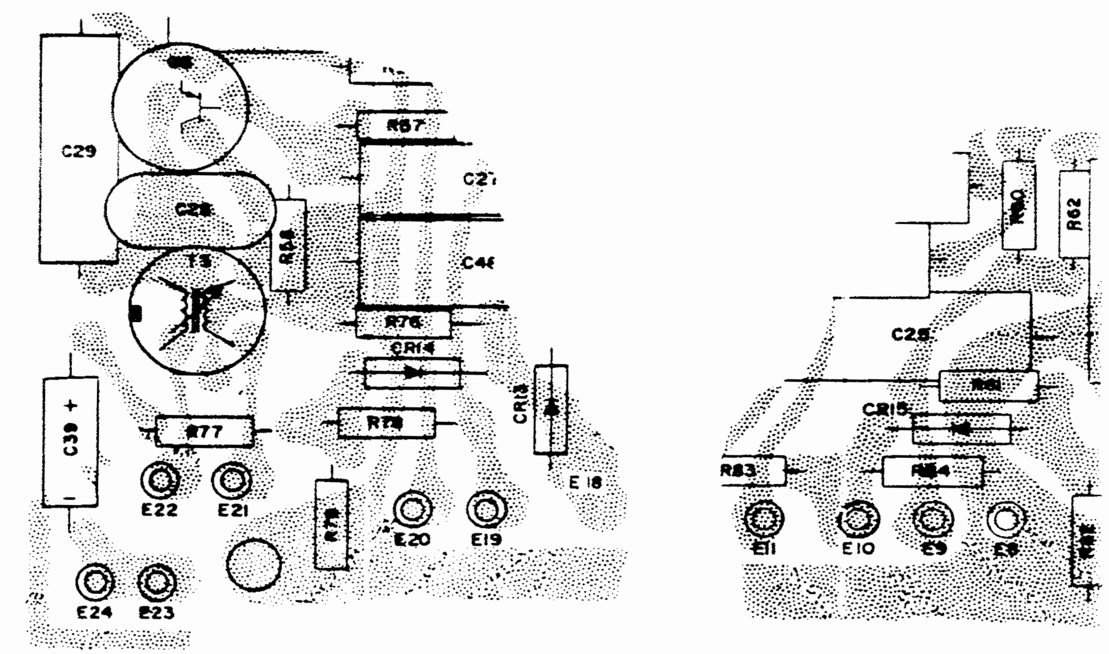
NOTES:

1. COMPONENT REF. DESIG. PREFIX 2A2A1A4.
2. THIS DRAWING REFLECTS THE CURRENT MODEL OF THE 500 KC AMPLIFIERS/GATES AND SIDETONE OSCILLATOR/GATES. EARLIER CIRCUITS WHERE ALTERATIONS HAVE OCCURRED ARE SHOWN IN THEIR ORIGINAL FORM IN SEPARATE DETAILS.

PARTS LOCATION INDEX

REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.
C25	9F	CR18	9C	E33	7E	R85	8E
C26	8F	CR19	6E	Q6	2E	R86	10E
C27	4E	CR20	6D	Q7	10E	R87	10D
C28	3F	CR21	5E	Q8	3B	R88	10C
C29	2E	E1	8A	R53	7F	R89	10C
C30	8F	E2	11B	R54	7F	R90	9C
C31	10F	E3	11B	R55	7F	R91	9B
C32	10F	E4	11H	R56	6G	R92	9D
C33	4C	E5	10H	R57	4E	R93	9D
C34	3C	E6	10G	R58	3F	R94	6F
C35	2B	E7	10G	R59	4E	R95	7E
C36	3B	E8	9G	R60	9E	R96	5E
C37	4D	E9	9G	R61	11F	R97	6D
C38	5E	E10	8G	R62	9E	R98	8E
C39	2G	E11	8G	R63	3C	R99	5E
C40	11G	E12	7G	R64	3C	R100	5F
C41	8F	E13	7G	R65	4A	R101	8C
C42	3E	E14	6G	R66	3D	R102	8C
C43	11D	E15	6G	R67	2D	R103	4B
C44	10C	E16	5G	R68	2D	R104	4C
C45	9B	E17	5G	R69	3D	R105	5B
C46	7E	E18	5G	R70	2D	R106	5C
C47	8D	E19	4G	R71	5G	R107	5C
C48	4F	E20	4G	R72	4D	R108	5B
C49	6F	E21	3G	R73	5D	R109	5C
C50	7D	E22	3G	R74	4D	R110	5D
C51	5C	E23	3H	R75	5G	R111	6B
C52	9D	E24	2H	R76	4F	R112	6C
CR10	5C	E25	5D	R77	3G	R113	9B
CR11	6F	E26	4D	R78	4G	R114	4C
CR12	8E	E27	4B	R79	3G	R115	8C
CR13	5G	E28	5B	R80	10G	RT1	4B
CR14	4G	E29	5B	R81	9F	T3	3F
CR15	9G	E30	9B	R82	9G	T4	10F
CR16	10D	E31	9B	R83	8G	T5	10B
CR17	10D	E32	8B	R84	9G		



EARLIER MODEL DETAILS
(NOTE 2)

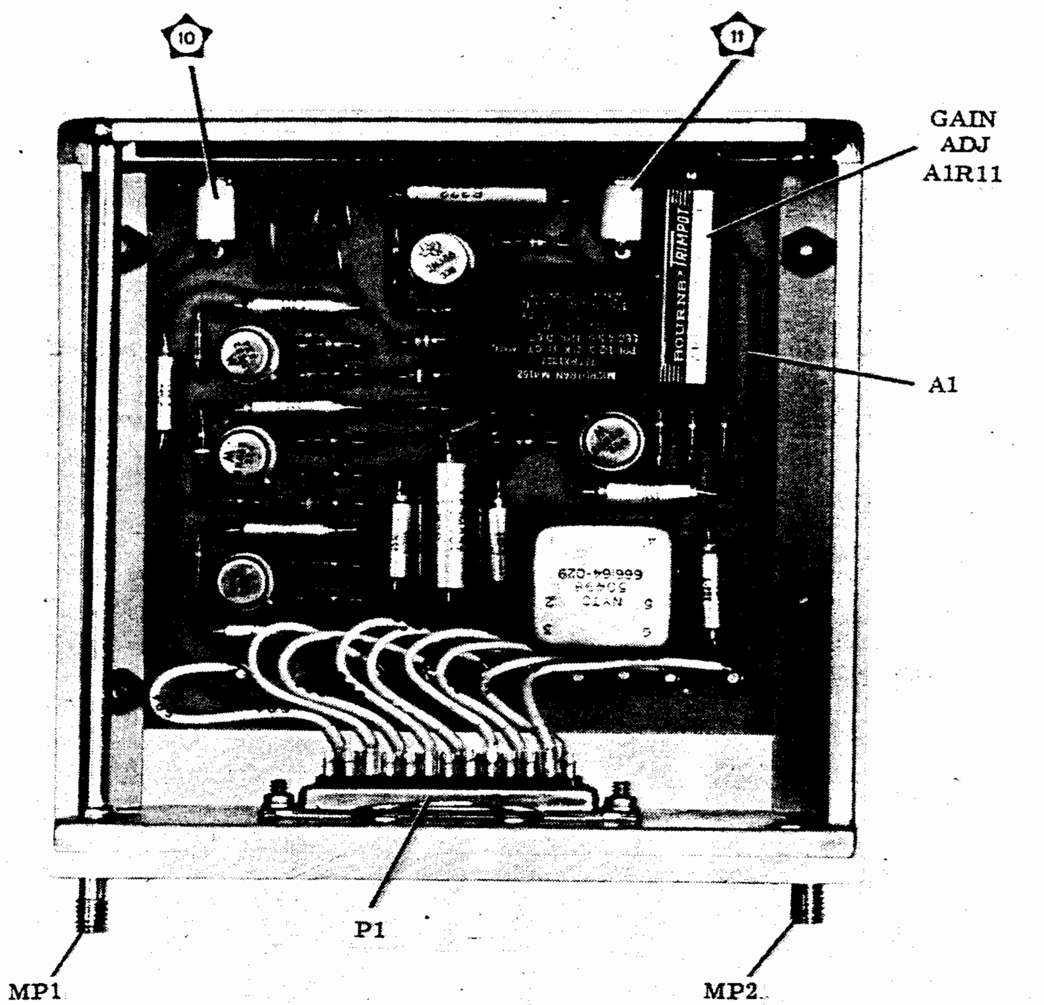


Figure 5-39. Transmitter Audio Amplifier Electronic Assembly, Component Location

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PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
C1	2F	R3	5D
C2	3E	R4	6D
C3	5F	R5	7D
C4	7C	R6	6D
C5	5B	R7	7E
C6	7D	R8	7F
C7	7F	R9	7F
C8	6F	R10	7G
C9	7G	R11	3C
C10	5F	R12	3E
C11	9D	R13	3E
CR1	6C	R14	4B
E1	8H	R15	6D
E2	6H	R16	6C
E3	6H	R17	8D
E4	5H	R18	8E
E5	4H	R19	8F
E6	4H	R20	7E
E7	3H	R21	8F
E8	2H	R22	6G
E9	3H	R23	7D
Q1	4E	RV1	7B
Q2	5C	RV2	7B
Q3	8D	T1	4F
Q4	8E	T2	4C
Q5	8F	TP1	3B
R1	2E	TP2	8B
R2	5E		

NOTES:

1. REF. DESIG. PREFIX 2A2.
2. ⚠1 THESE TEST POINTS ARE THE SAME FOR BOTH 2A2A2A1 AND 2A2A3A1.

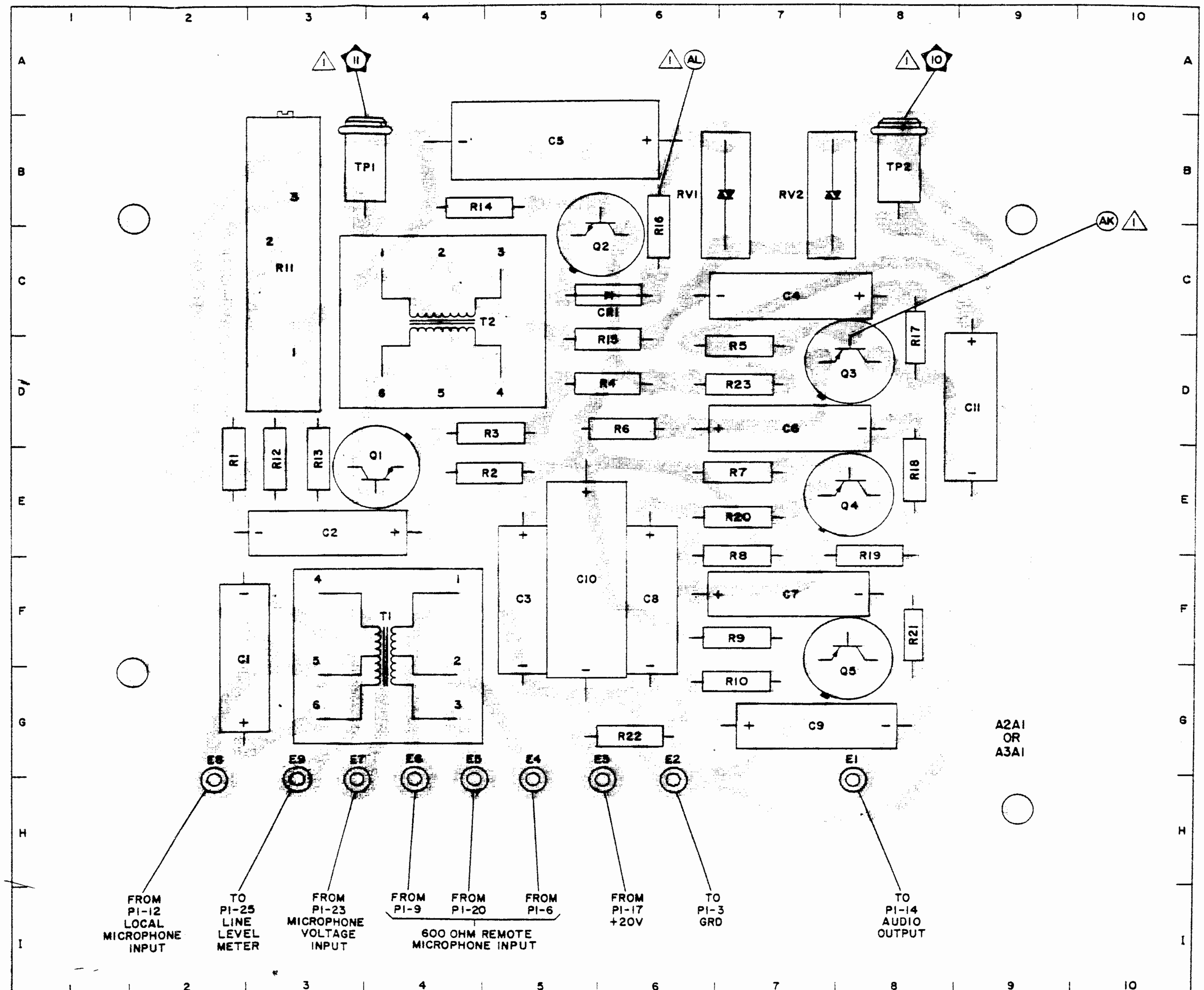
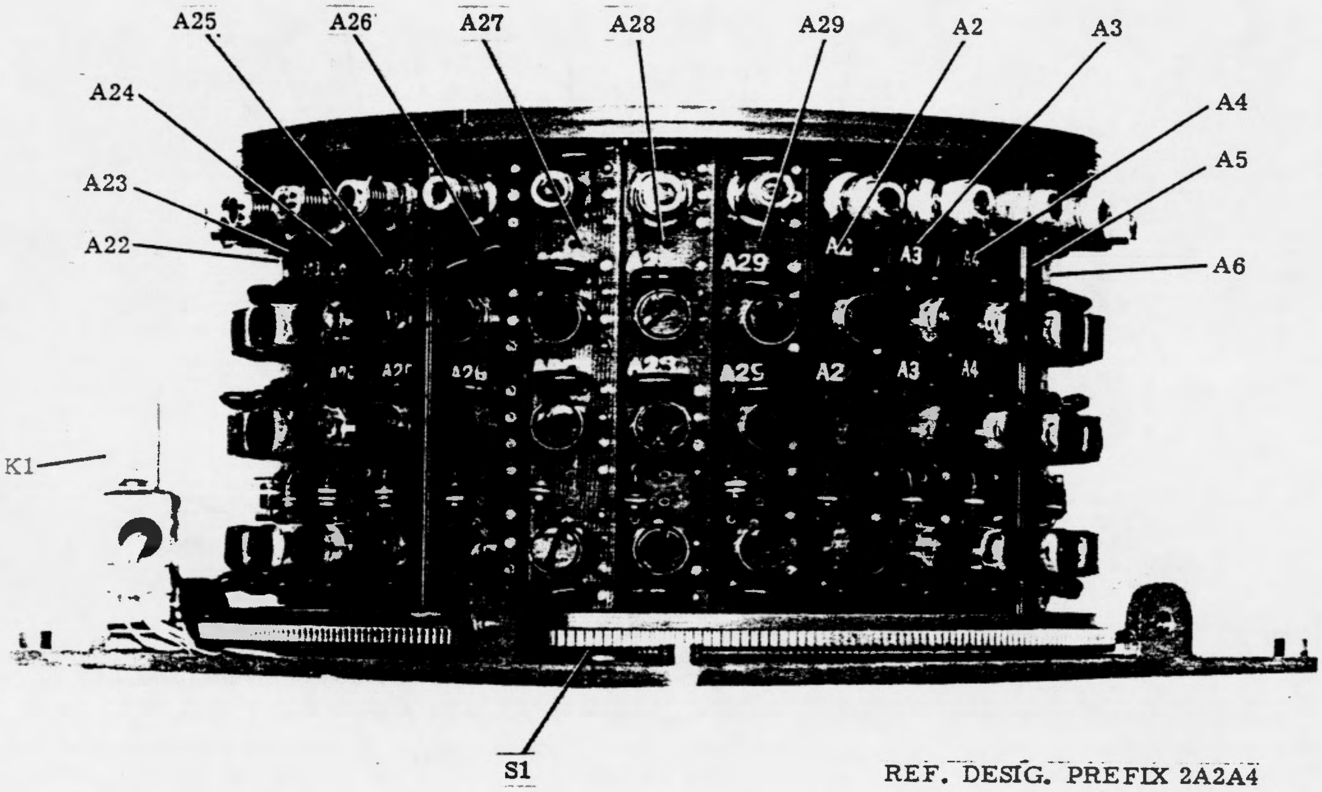
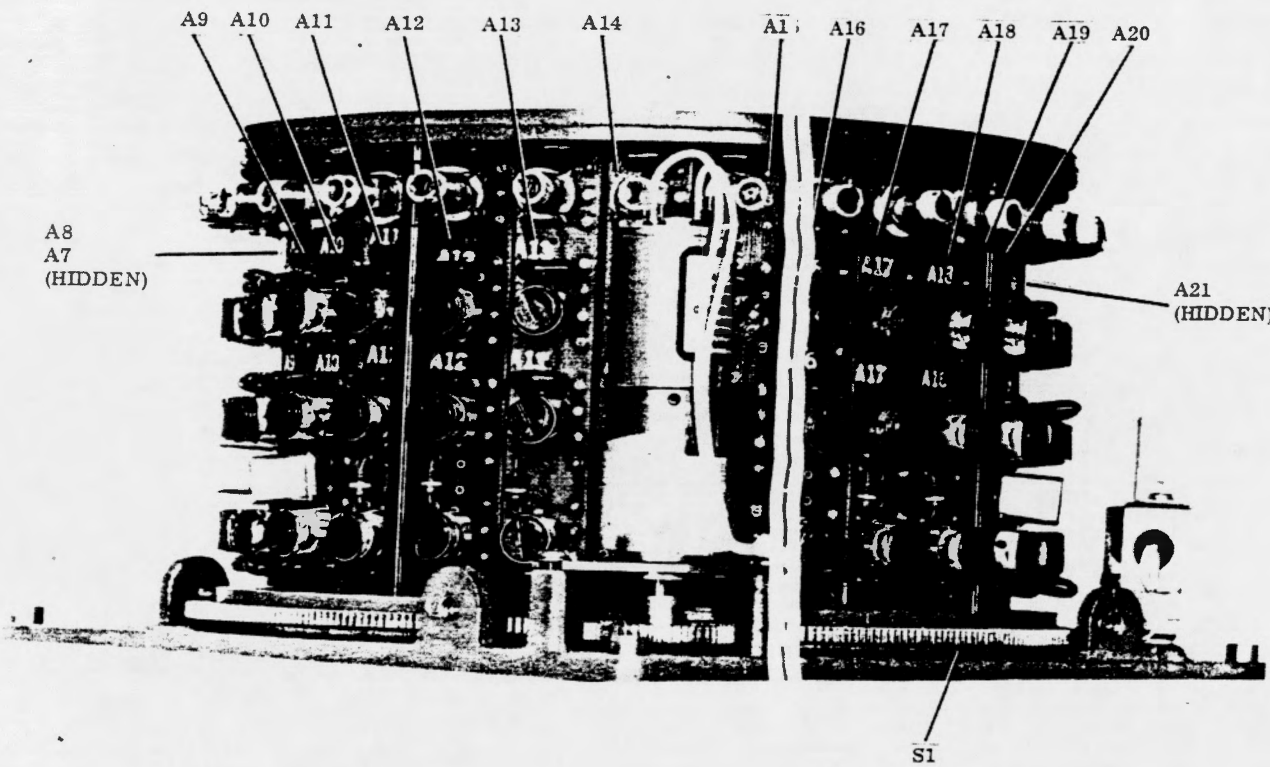


Figure 5-40. Audio Amplifiers (Foil Side Up), Component and Test Point Location



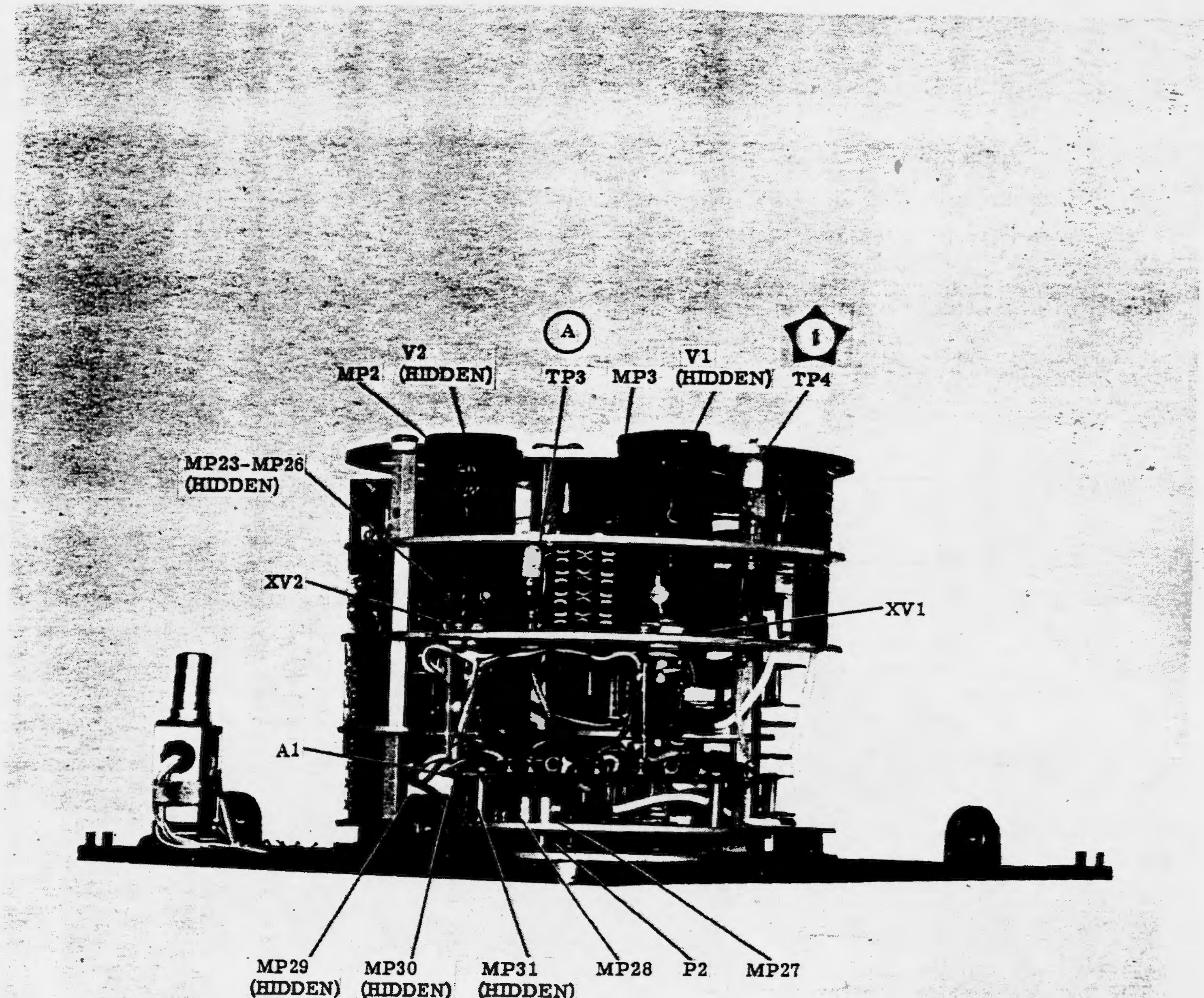
REF. DESIG. PREFIX 2A2A4

Figure 5-41. RF Amplifier Electronic Assembly, Front and Left Side, Component Location



REF. DESIG. PREFIX 2A2A4

Figure 5-42. RF Amplifier Electronic Assembly, Rear and Right Side, Component Location



REF. DESIG. PREFIX 2A2A4

Figure 5-43. RF Amplifier Electronic Assembly, Turret Removed, Front and Left Side, Component and Test Point Location

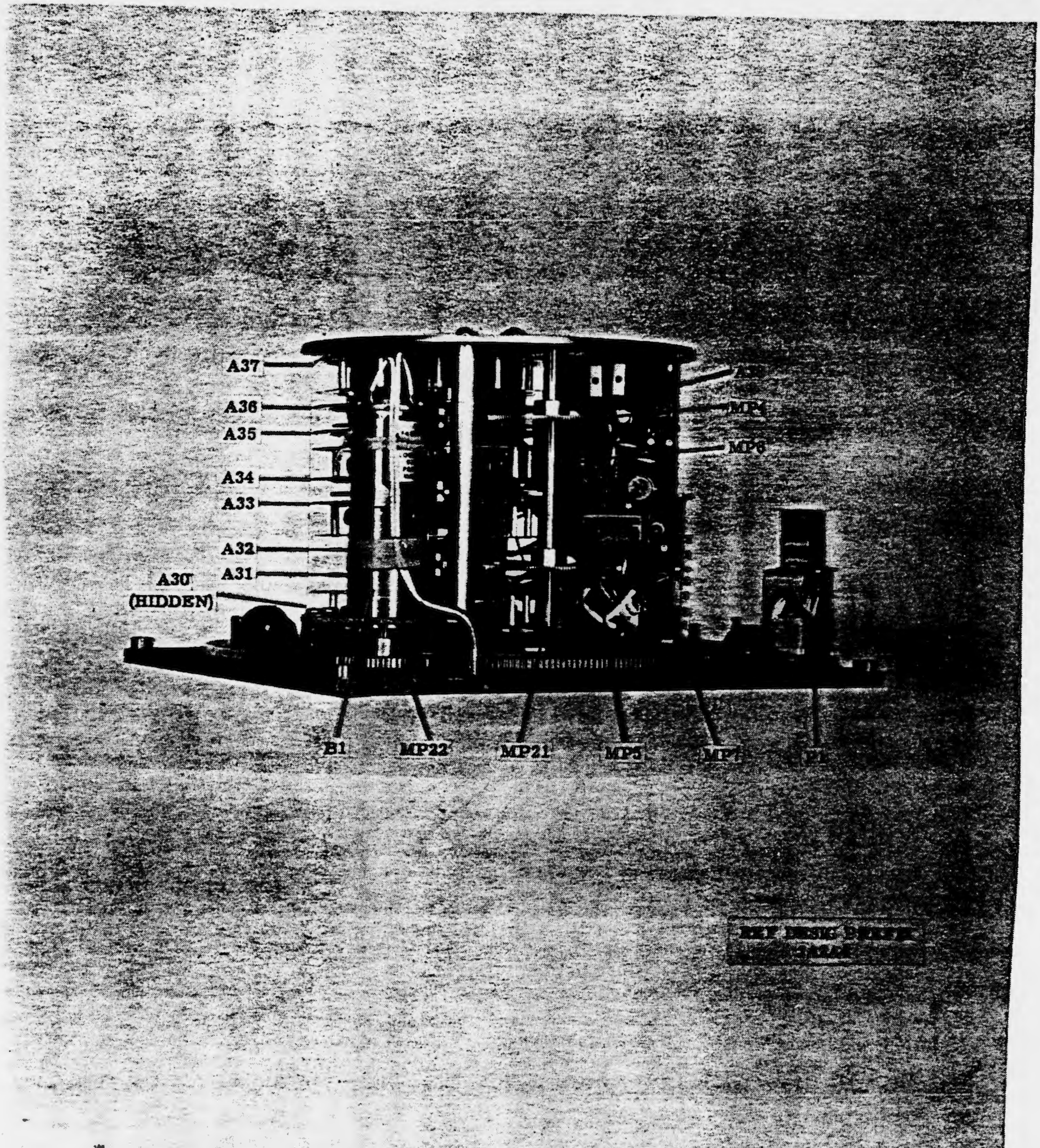


Figure 5-44. RF Amplifier Electronic Assembly, Turret Removed, Rear and Right Side View, Component Location

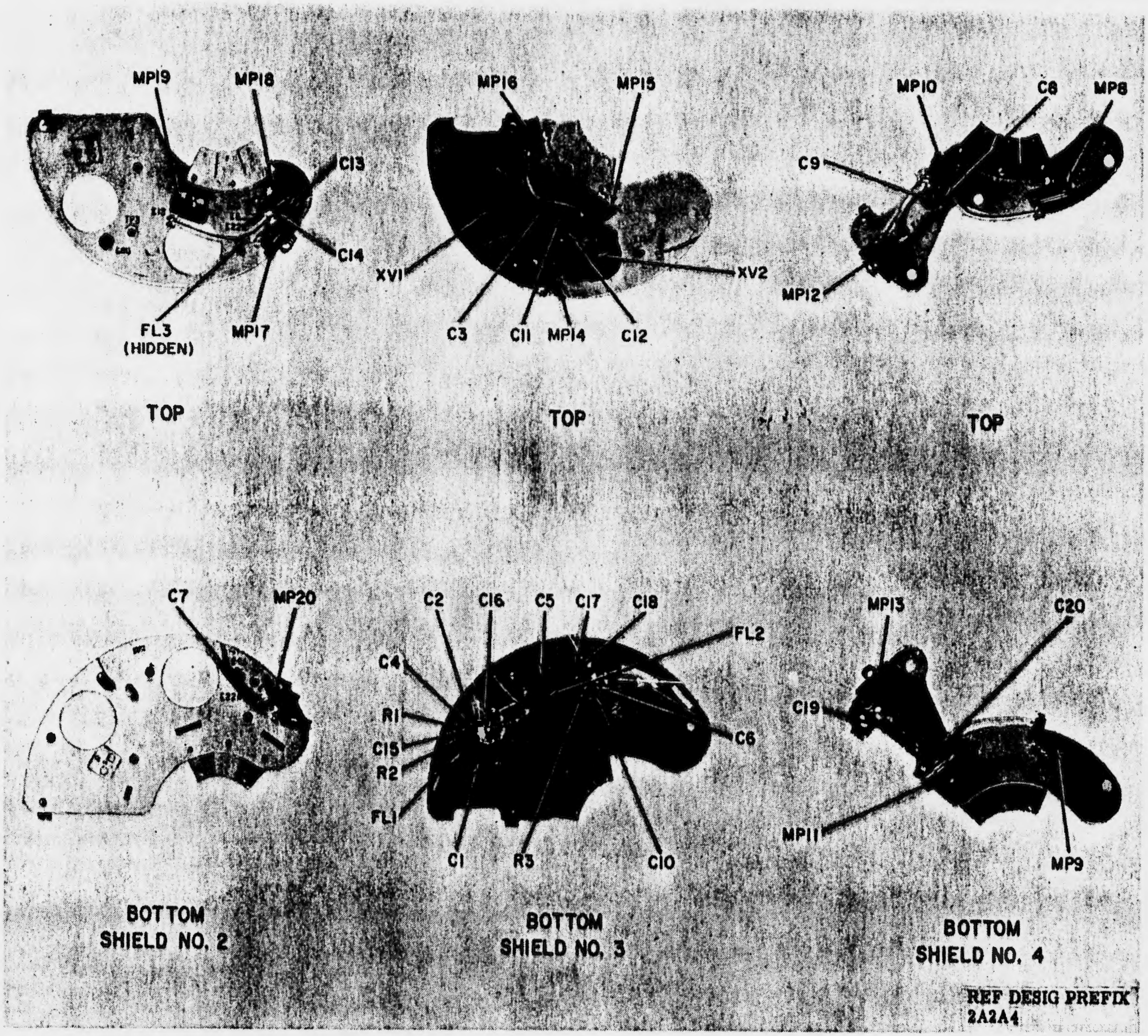


Figure 5-44a. RF Amplifier Electronic Assembly, Internal Shields, Component Location

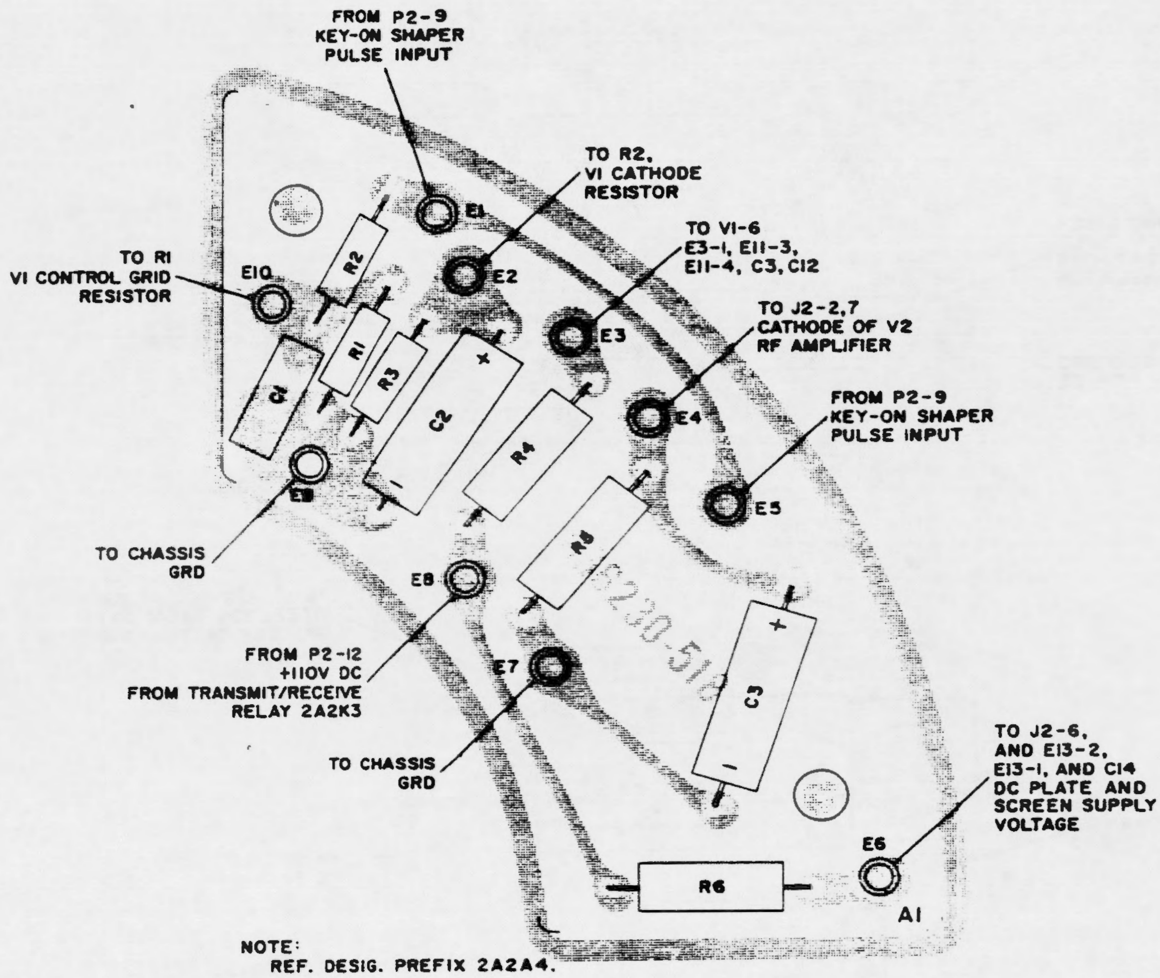


Figure 5-45. RF Amplifier Bias Circuit (Foil Side Up), Component Location

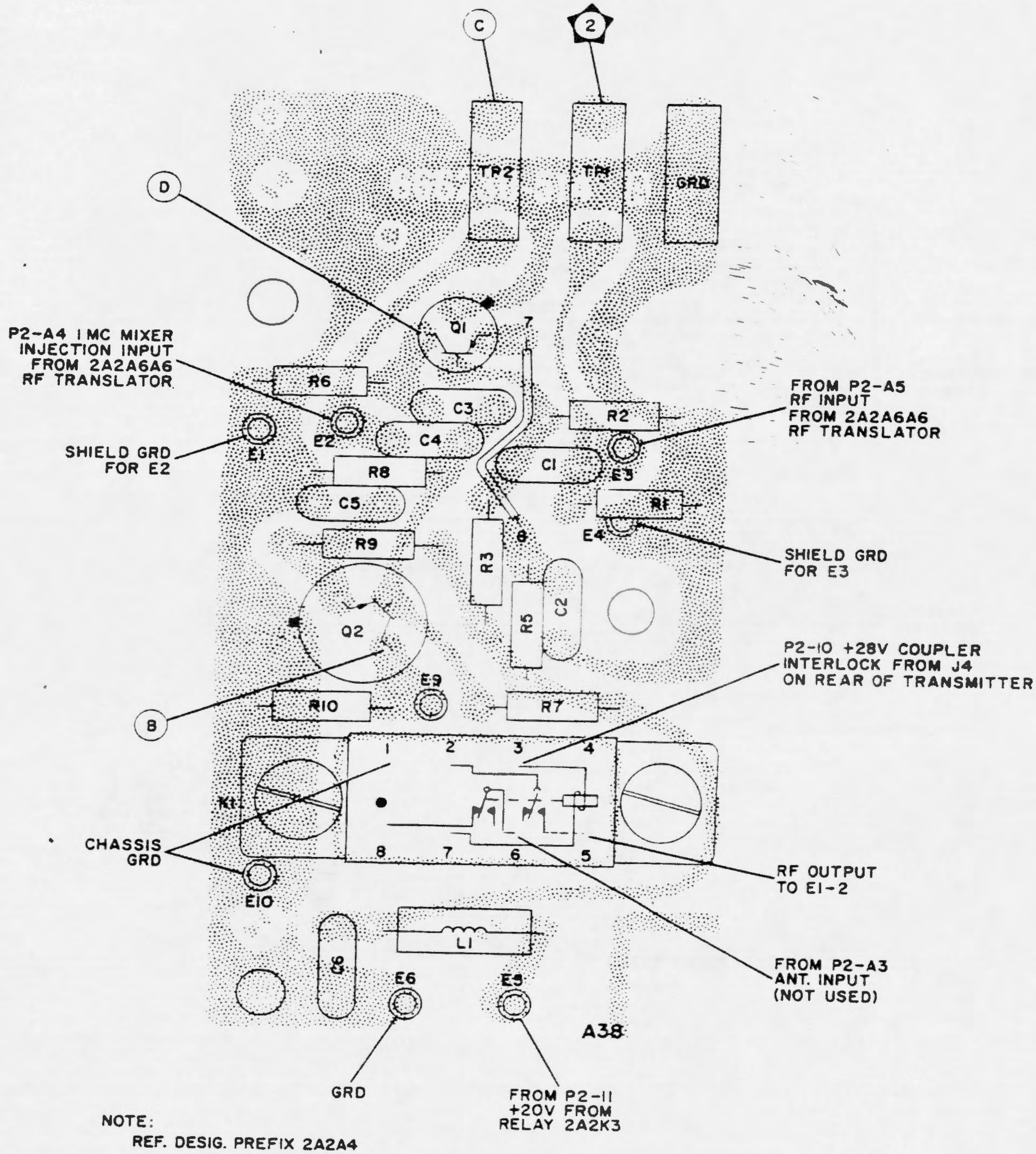
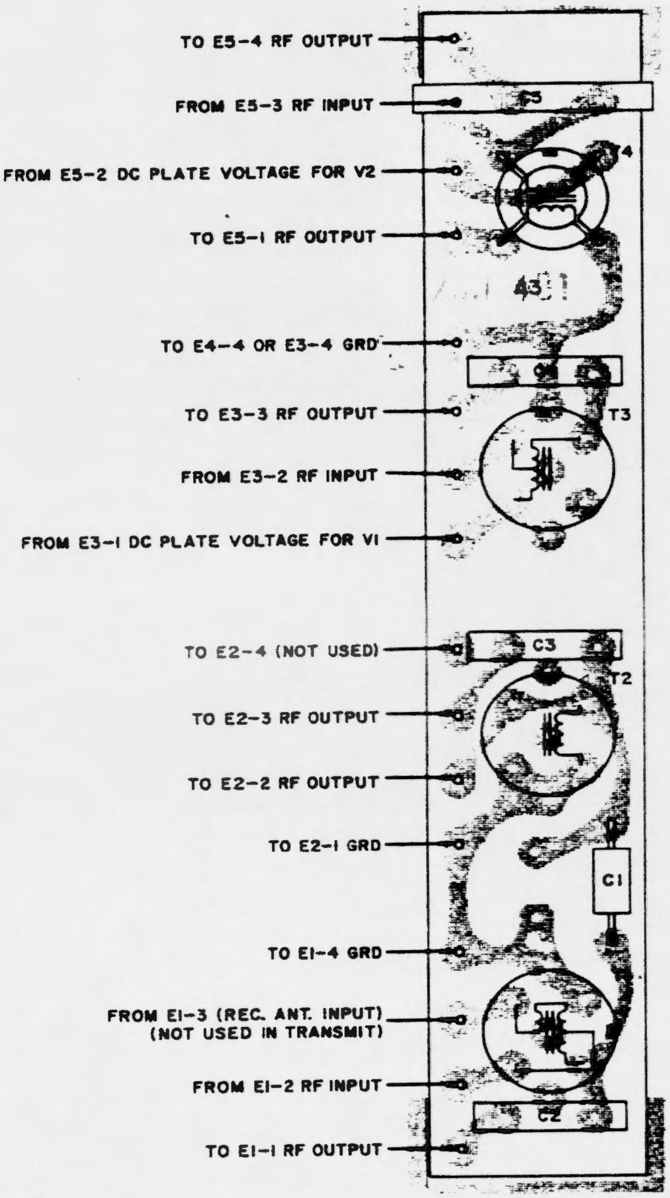
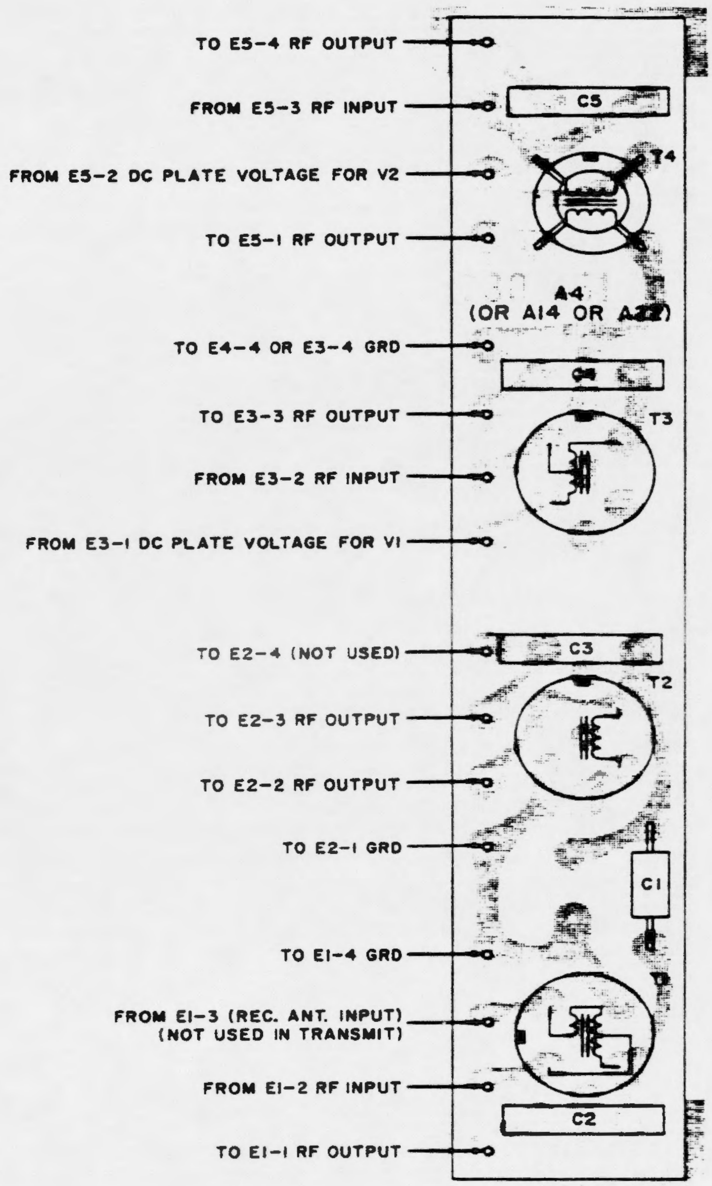


Figure 5-46. HF Mixer/Amplifier (Foil Side Up), Component and Test Point Location



NOTE:
REF. DESIG. PREFIX 2A2A4.

Figure 5-47. Megacycle Assembly A3 (Foil Side Up), Component Location



NOTE:
REF. DESIG. PREFIX 2A2A4.

Figure 5-48. Megacycle Assembly A4, A14, or A22 (Foil Side Up), Component Location

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NOTE:
REF DESIG PREFIX 2A2A5

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	6D	E6	3C	R7	5B
C2	6C	E7	5B	R8	5B
C3	4C	E8	2D	R9	4B
C4	7E	E9	2D	R10	7B
C5	6C	E10	3G	R11	6B
C6	4D	E13	5E	R12	4B
C7	4D	E14	5E	R13	7D
C8	5D	E15	3F	R14	3B
C9	6D	E17	E4	R15	3B
C10	6C	E18	5G	R16	2B
C11	5E	E19	6F	R17	2F
C12	5E	E20	6C	R18	3G
C13	6D	E22	3C	R19	2D
C14	5C	E25	2B	R20	3D
C15	2D	E26	4E	R21	3E
C16	2C	E28	2G	R22	2G
C17	3D	E30	6H	R23	4E
C18	2E	E31	6G	R24	3G
C19	3D	L1	4C	R25	4G
C20	4F	L2	3F	R26	6H
C21	4F	Q1	7D	R27	6F
C22	4G	Q2	5D	R28	5G
C23	5G	Q3	5D	R29	6F
C24	5G	Q4	3C	R30	6G
C25	6F	Q5	2E	T1	7F
C26	5C	Q6	7G	T2	4D
CR1	4G	Q7	5F	T3	6E
CR2	5G	R1	6D	T4	2C
DS1	6H	R2	7D	T5	3E
E1	7F	R3	4B	T6	4F
E3	6F	R4	7E	TP1	7H
E4	2F	R5	3E	TP2	5H
E5	3E	R6	4E		

REF DESIG	LOC	ORIGIN/DESTINATION
E3	6F	TO P1-A3 1 MC OUTPUT
E5	3E	+20V FROM P1-1
E13	5E	FROM P1-A4 EXTERNAL 5 MC INPUT
E14	5E	5 MC INPUT FROM S1-7
E17	4E	EXTERNAL 5 MC TO S1-1
E18	5G	+20V FROM S1-11
E19	6F	SHIELD GRD FOR E3
E26	4E	SHIELD GRD FOR E13 AND E14

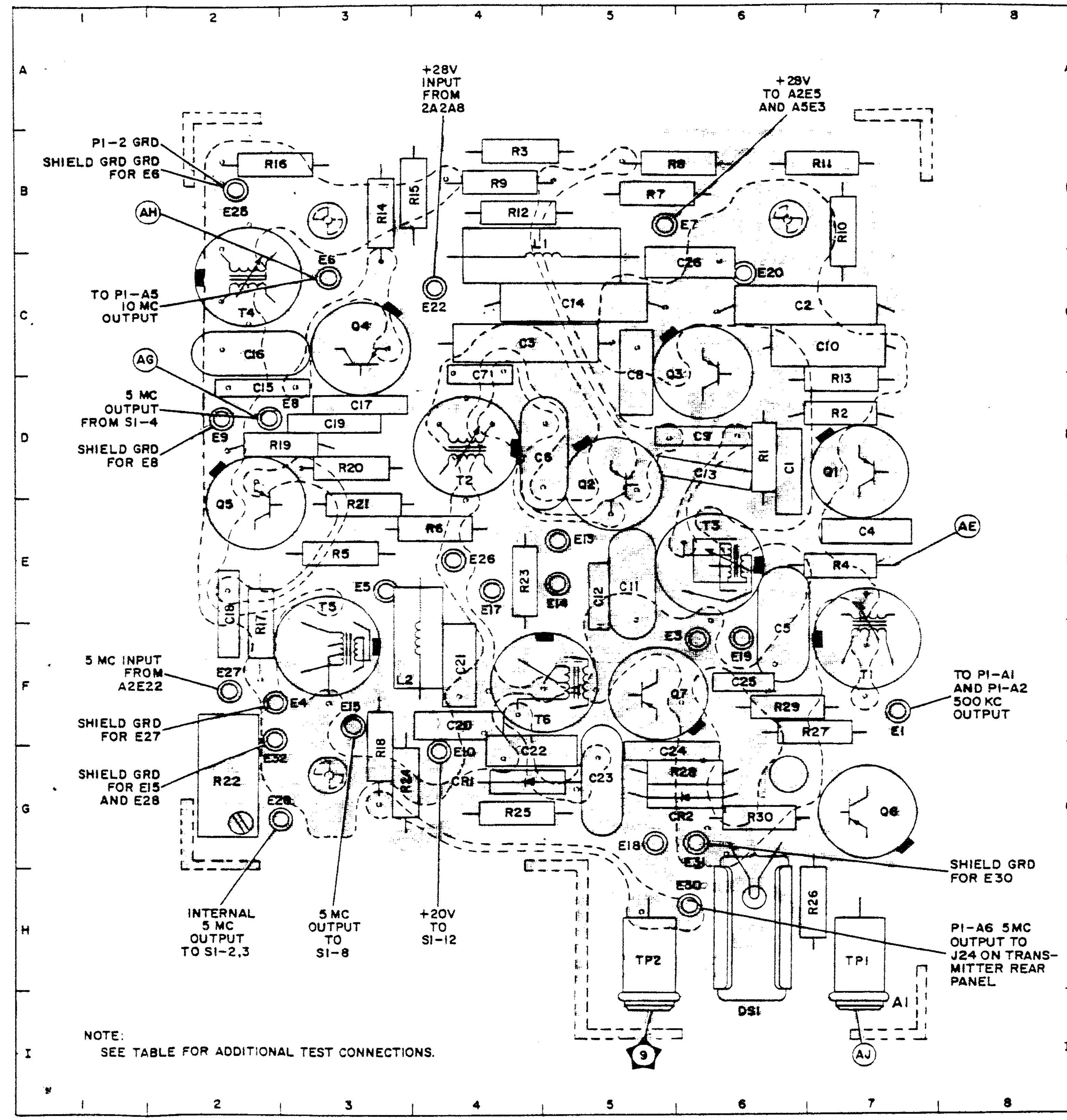
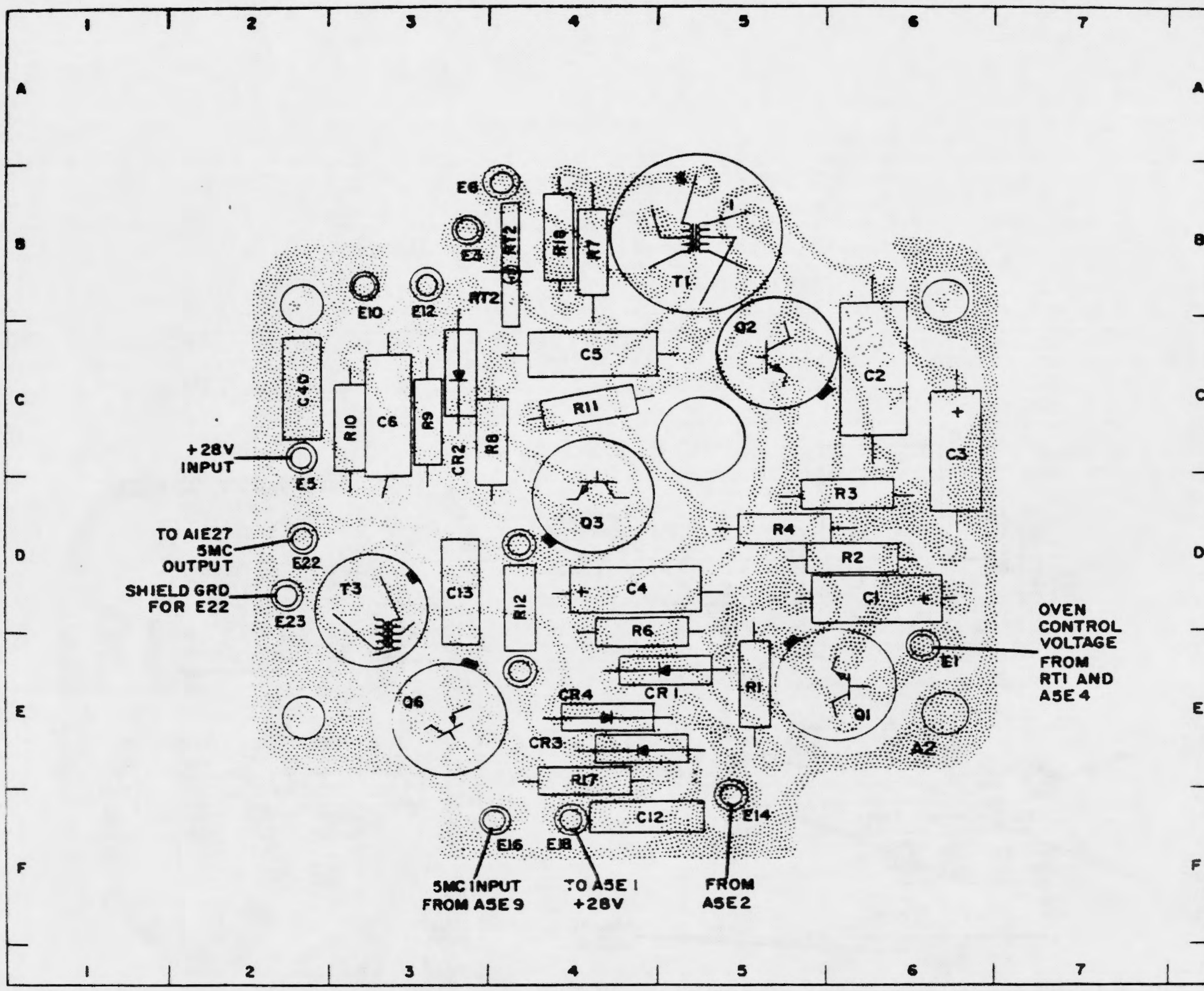


Figure 5-71. 5 MC Multiplier, Dividers, and Comparator (Foil Side Up), Component and Test Point Location

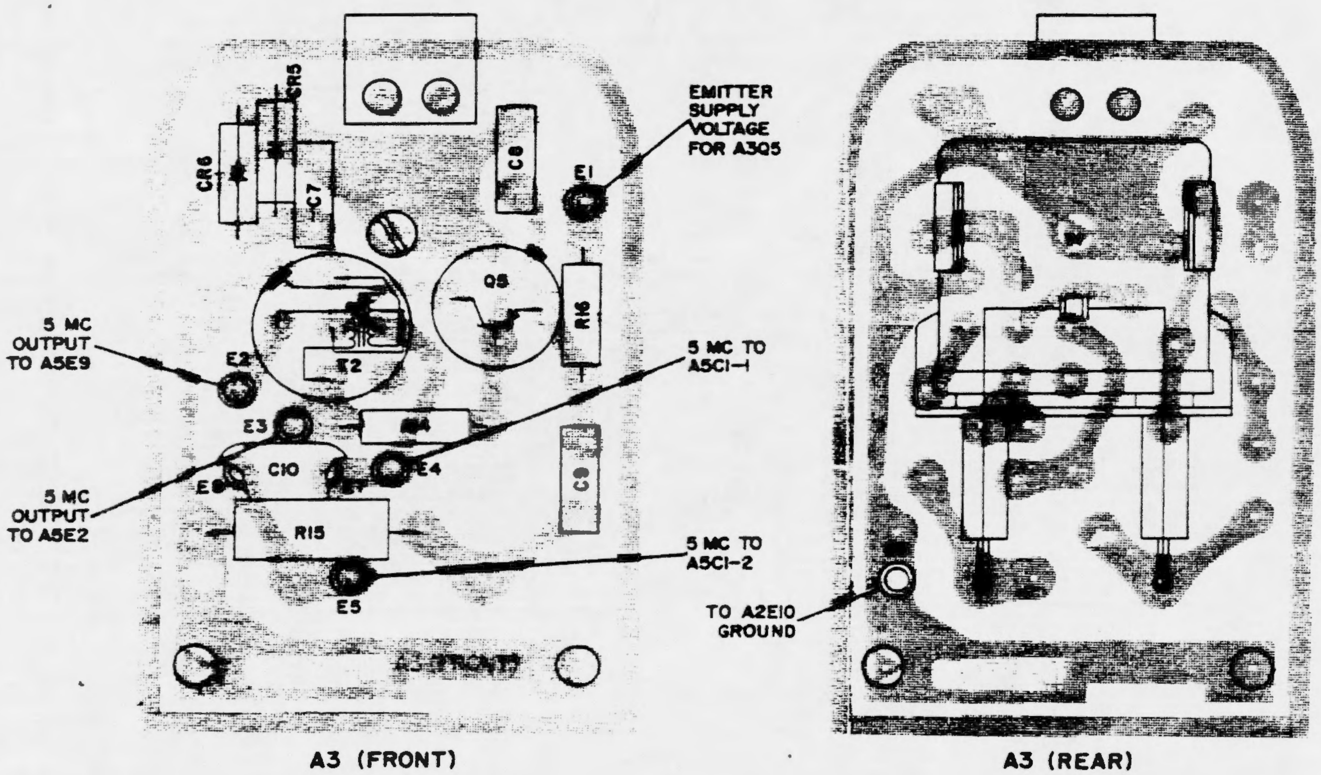


NOTE:
REF. DESIG. PREFIX 2A2A5.

PARTS LOCATION INDEX

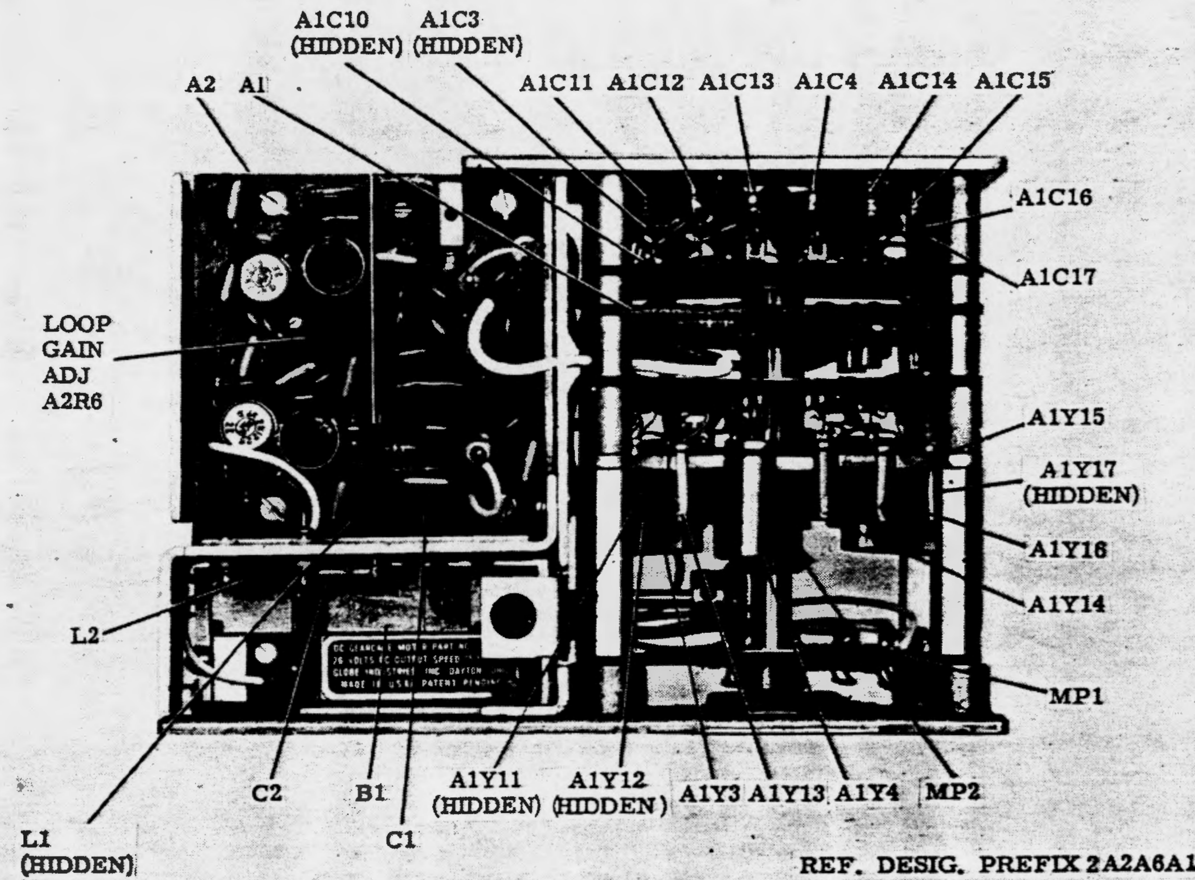
REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	6D	CR3	4E	E22	2D	R7	4B
C2	6C	CR4	4E	E23	2D	R8	3C
C3	6C	E1	6E	Q1	5E	R9	3C
C4	4D	E3	3B	Q2	5C	R10	3C
C5	4C	E5	2C	Q3	4D	R11	4C
C6	3C	E6	4B	Q6	3E	R12	4D
C12	4F	E10	3B	R1	5E	R17	4E
C13	3D	E12	3B	R2	6D	R18	4B
C40	2C	E14	5F	R3	6D	RT2	4B
CR1	4E	E16	4F	R4	5D	T1	5B
CR2	3C	E18	4F	R6	4D	T3	3D

Figure 5-72. Oven Control and Buffer Amplifier (Foil Side Up), Component Location



NOTE:
REF. DESIG. PREFIX 2A2A5.

Figure 5-73. 5 MC Oscillator (Foil Side Up), Component Location



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igure 5-75. 1 MC Synthesizer Electronic Subassembly, Front View, Component Location

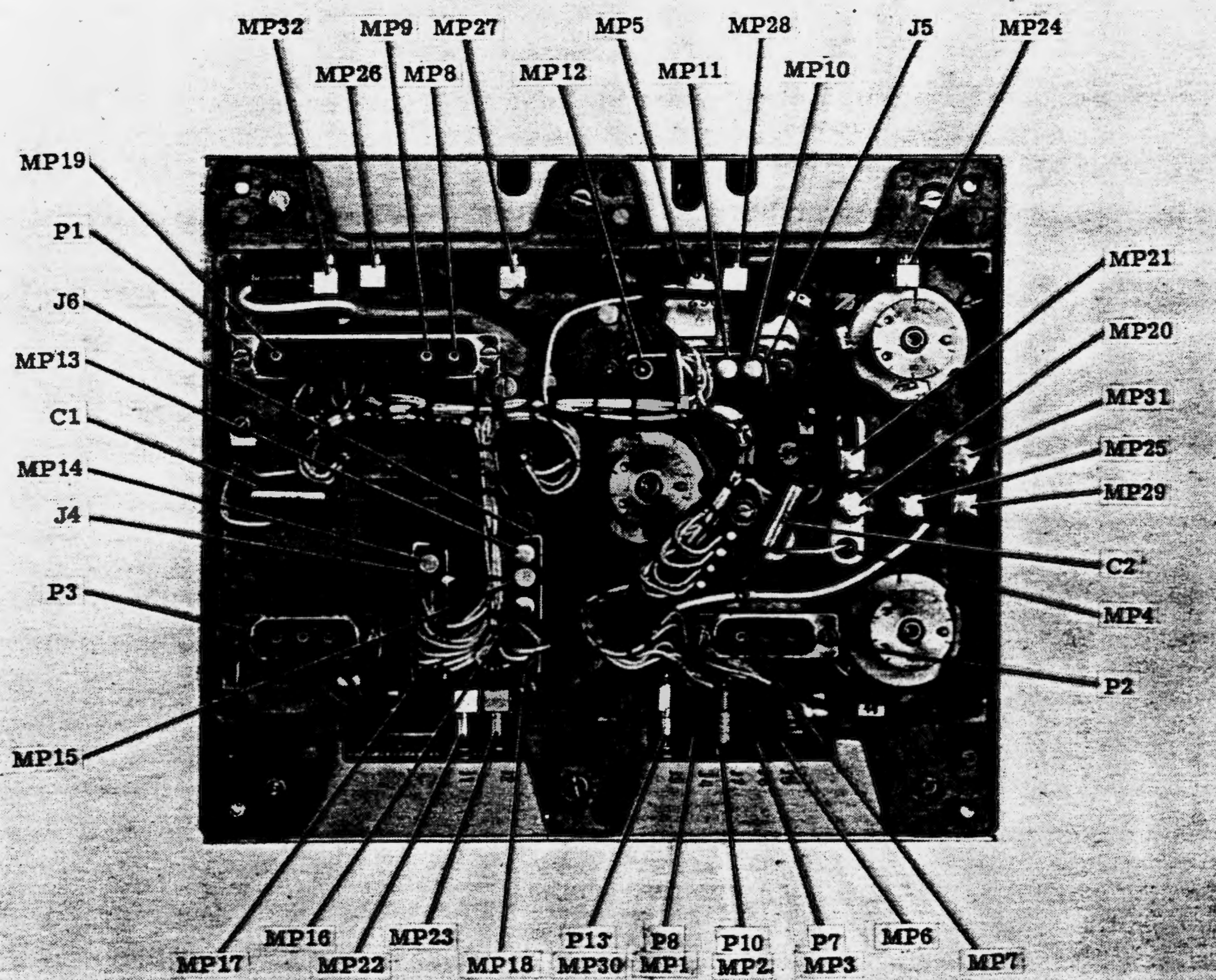


Figure 5-74. Translator/Synthesizer Electronic Assembly, Bottom View, Component Location

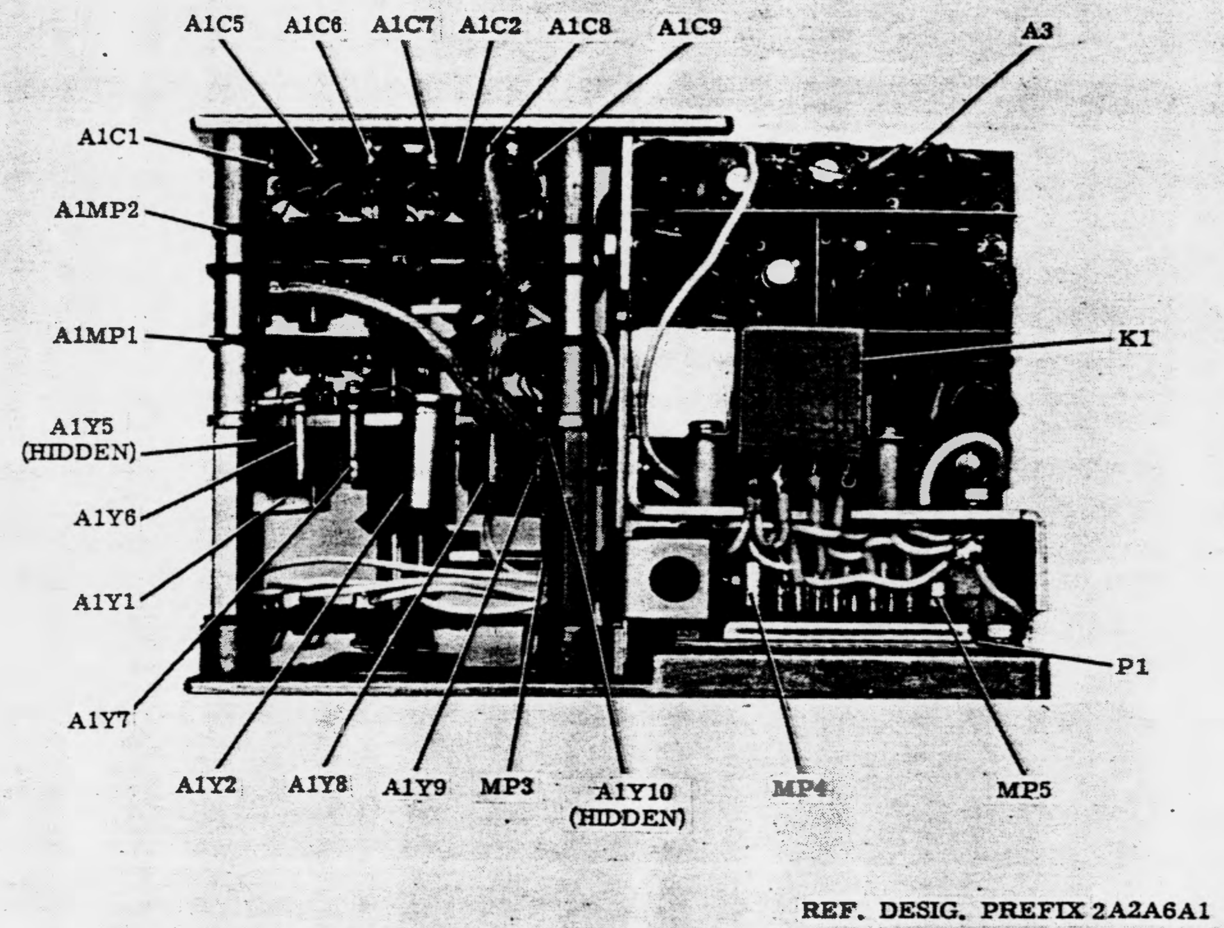


Figure 5-76. 1 MC Synthesizer Electronic Subassembly, Rear View, Component Location

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C18	6E	C27	3D	E4	6F	L3	3B	R4	5E	R12	3D
C19	5C	C28	4F	E5	6F	Q1	3C	R5	5D	R13	2C
C20	5B	CR1	6C	E6	6B	Q2	3E	R6	6D	R14	2E
C21	4B	CR2	6C	E8	6B	Q3	3E	R7	4C	R15	3E
C23	6C	CR3	6B	E9	6C	Q4	4E	R8	4B	R16	3E
C24	3C	E1	3F	E10	2C	R1	6B	R9	3C	R17	5F
C25	5E	E2	3F	L1	6E	R2	4B	R10	3B	R18	4F
C26	2D	E3	5F	L2	4C	R3	5D	R11	3D	RT1	6D

NOTE:
REF. DESIG. PREFIX 2A2A6A1.

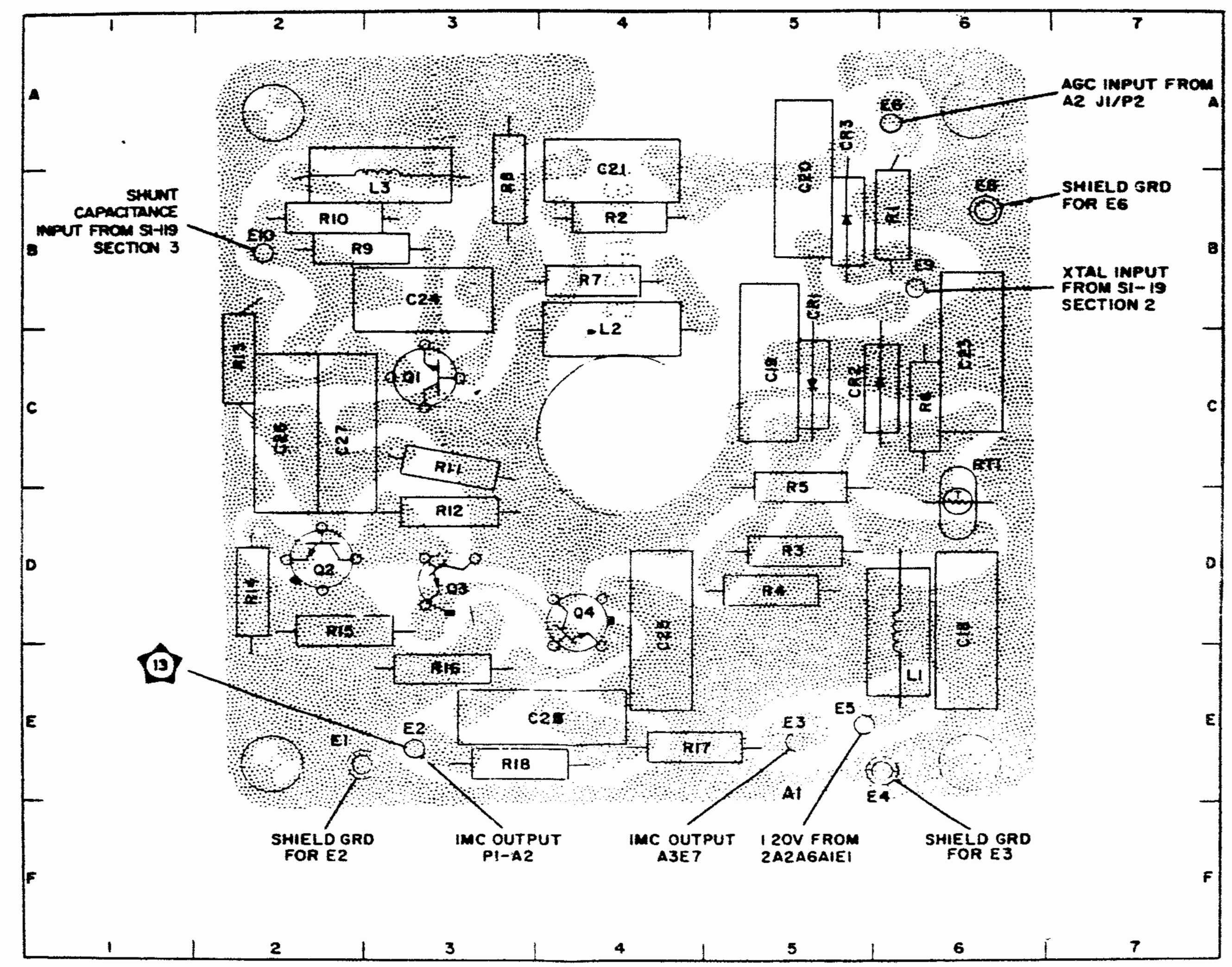
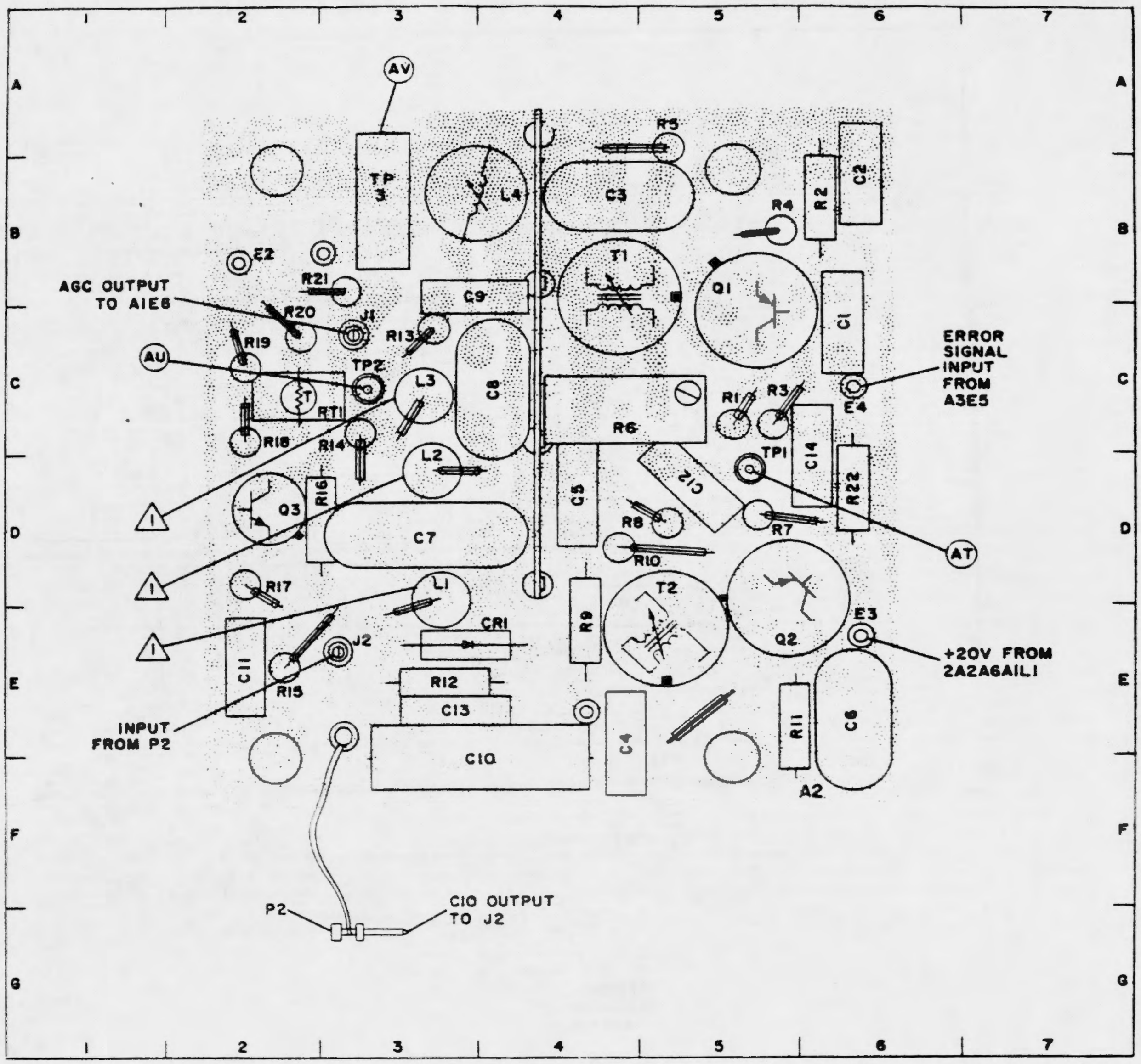


Figure 5-77. MC Oscillator (Foil Side Up), Component and Test Point Location



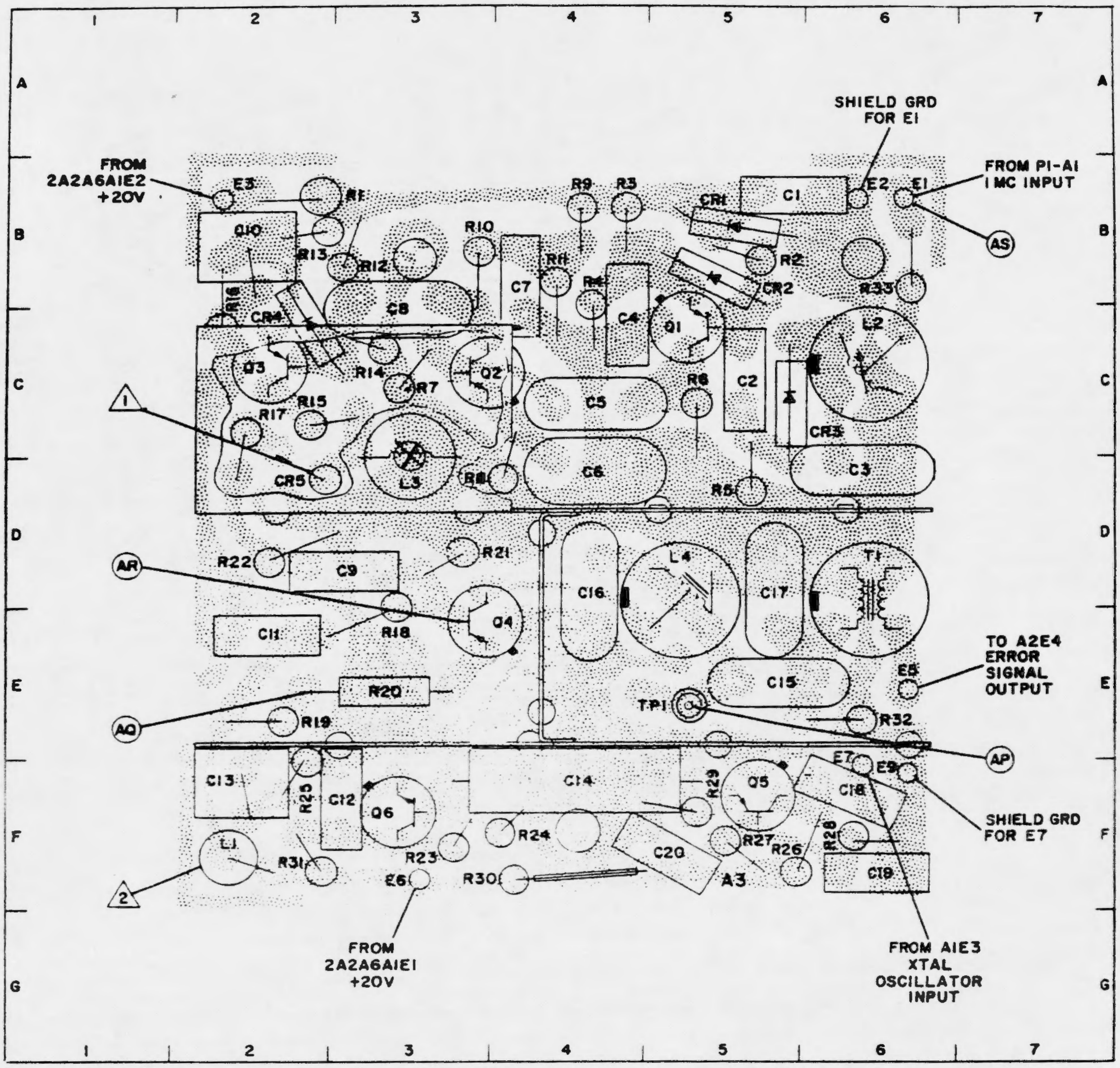
NOTES:

1. REF. DESIG. PREFIX 2A2A6A1.
2. △1 VERTICALLY MOUNTED COMPONENTS

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	6C	C11	2E	L1	3D	R3	5C	R13	3C	RT1	2C
C2	6B	C12	5D	L2	3D	R4	5B	R14	3C	T1	4B
C3	4B	C13	3E	L3	3C	R5	5A	R15	2E	T2	5E
C4	4E	C14	6D	L4	4B	R6	4C	R16	3D	TP1	5D
C5	4D	CR1	2E	P2	3G	R7	5D	R17	2D	TP2	3C
C6	6E	E2	2B	Q1	5B	R8	5D	R18	2C	TP3	3B
C7	3D	E3	6E	Q2	5E	R9	4E	R19	2C		
C8	4C	E4	6C	Q3	2D	R10	4D	R20	2C		
C9	3B	J1	3C	R1	5C	R11	5E	R21	3B		
C10	3F	J2	3E	R2	6B	R12	3E	R22	6D		

Figure 5-78. MC Oscillator AGC (Foil Side Up), Component and Test Point Location



NOTES:
1. REF. DESIG. PREFIX 2A2A6A1.
2. ⚠1 CR5 ANODE CONNECTION ON FOIL SIDE, VERTICALLY MOUNTED.
⚠2 L1 VERTICALLY MOUNTED.

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PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG
C1	5B	C12	3F	CR3	5C	L2	6C	R3	4B	R14	3C	R25
C2	5C	C13	2F	CR4	2C	L3	3D	R4	4B	R15	2C	R26
C3	6D	C14	4F	CR5	2D	L4	5D	R5	5D	R16	2C	R27
C4	4C	C15	5E	E1	6B	Q1	5C	R6	5C	R17	2C	R28
C5	4C	C16	4D	E2	6B	Q2	3C	R7	3C	R18	3E	R29
C6	4D	C17	5D	E3	2B	Q3	2C	R8	3D	R19	2E	R30
C7	4B	C18	6F	E5	6E	Q4	3E	R9	4B	R20	3E	R31
C8	3B	C19	6F	E6	3F	Q5	5F	R10	3B	R21	3D	R32
C9	3D	C20	5F	E7	6F	Q6	3F	R11	4B	R22	2D	R33
C10	2B	CR1	5B	E9	6F	R1	2B	R12	3B	R23	3F	T1
C11	2E	CR2	5B	L1	2F	R2	5B	R13	2B	R24	4F	TP1

Figure 5-79. Spectrum Generator/Mixer (Fo
Side Up), Component and Test Point Locatio

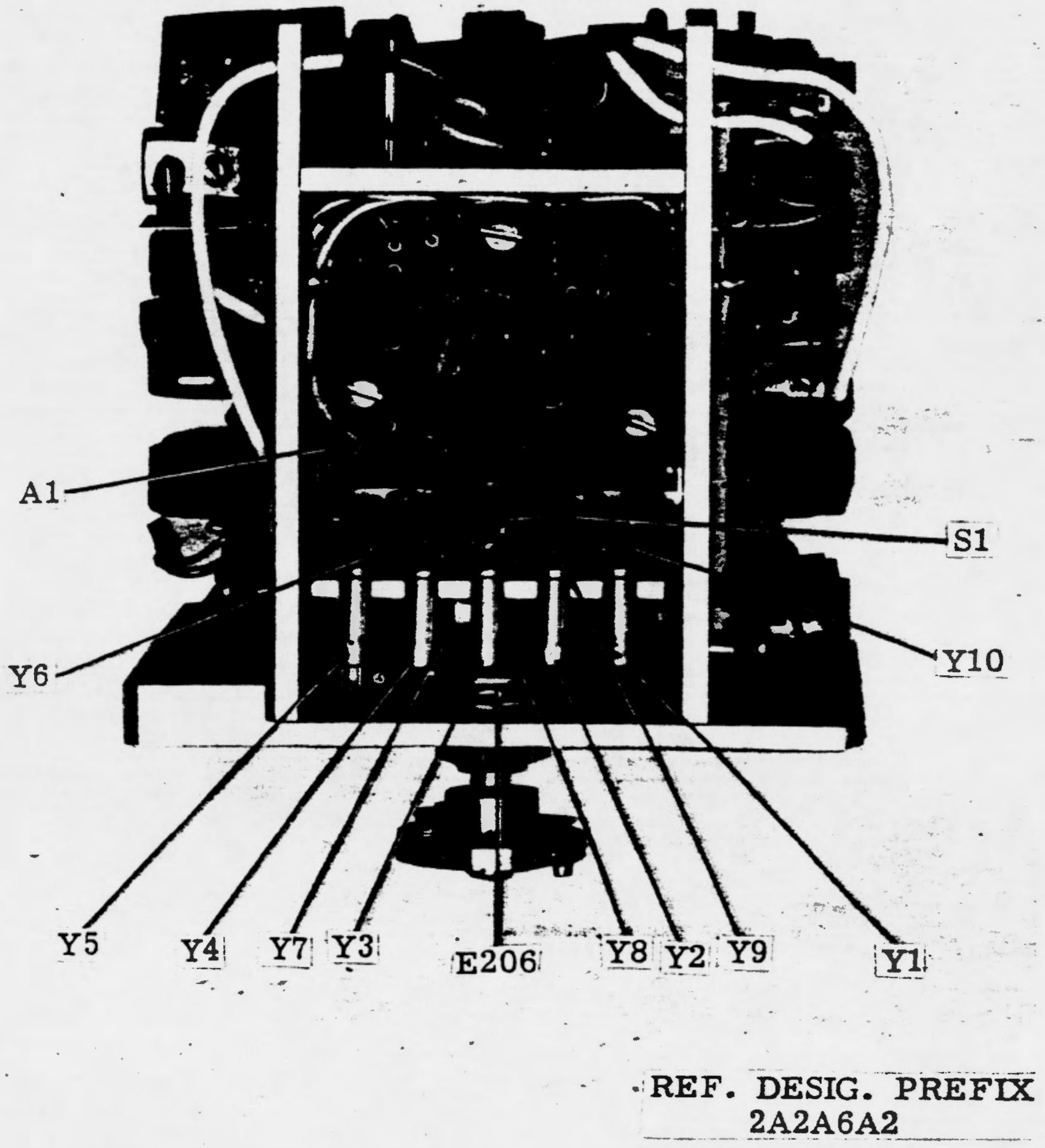

Figure 5-80. 100 KC Synthesizer Electronic Subassembly, Right Side, Component Location

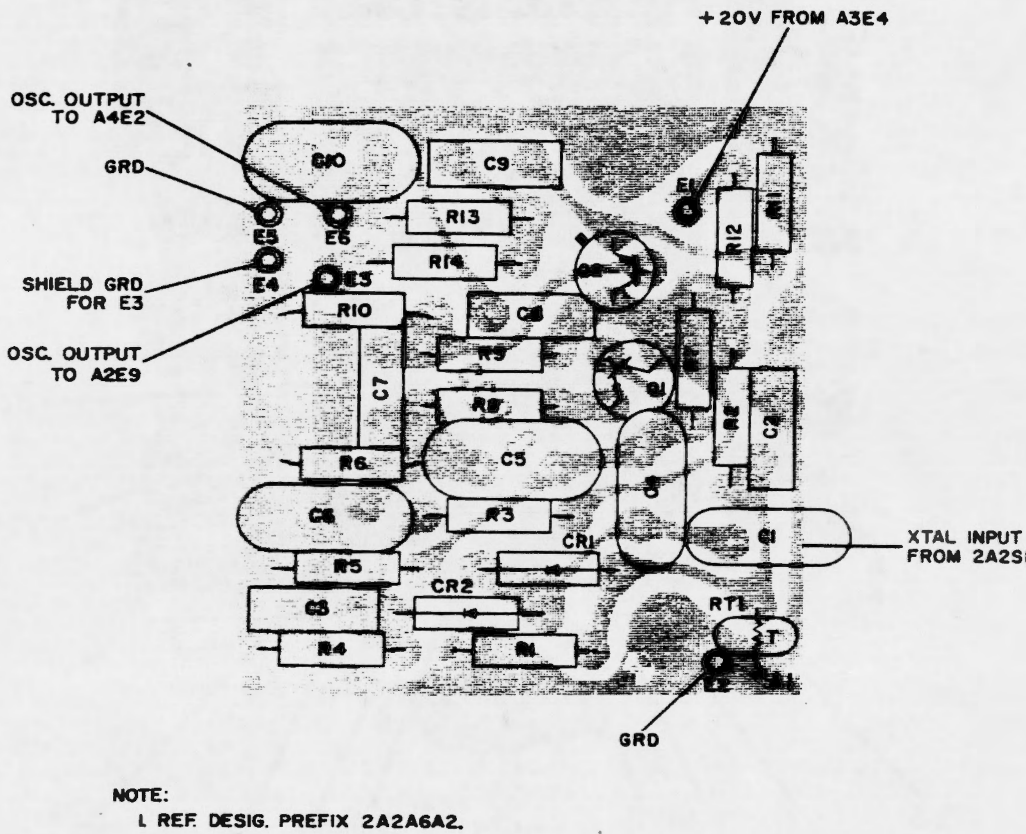

Figure 5-81. 4.553 MC to 5.453 MC Oscillator (Foil Side Up), Component Location

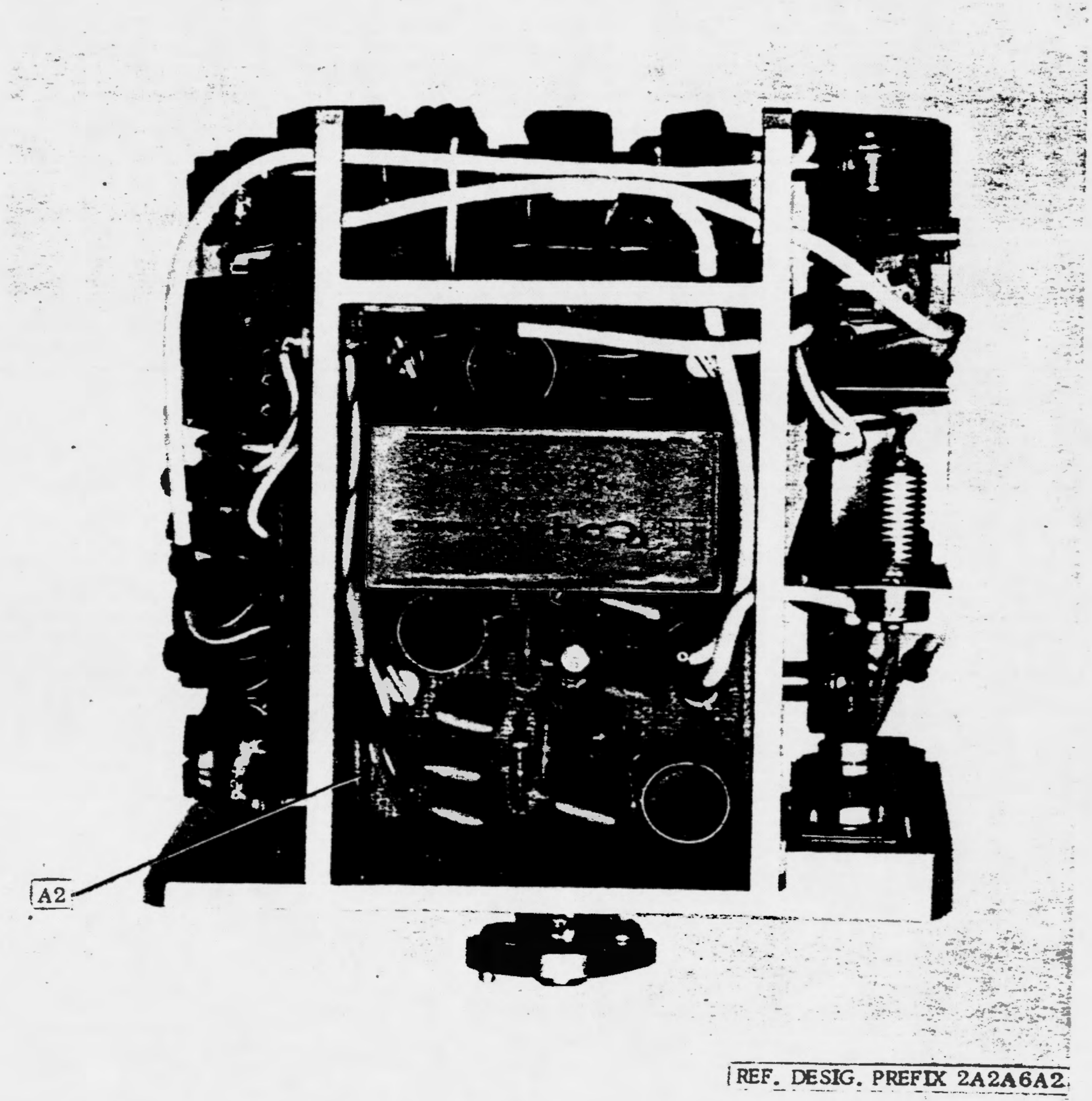

Figure 5-82. 100 KC Synthesizer Electronic Subassembly, Left Side, Component Location

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PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
C1	2B	Q2	4D
C2	3C	R1	3E
C3	2C	R2	3E
C4	2D	R3	2A
C5	3B	R4	2D
C6	3D	R5	4B
C7	4E	R6	4C
C8	4B	R7	2D
C9	4E	R8	4D
C10	4C	R9	5D
CR1	3B	R10	4D
CR2	3B	R11	3B
E1	2C	R12	3A
E2	3B	R13	3B
E3	5C	R14	3D
E4	5B	R15	5C
E5	5D	R16	4B
E6	4B	RT1	2B
E7	2C	T1	5B
Q1	3D		

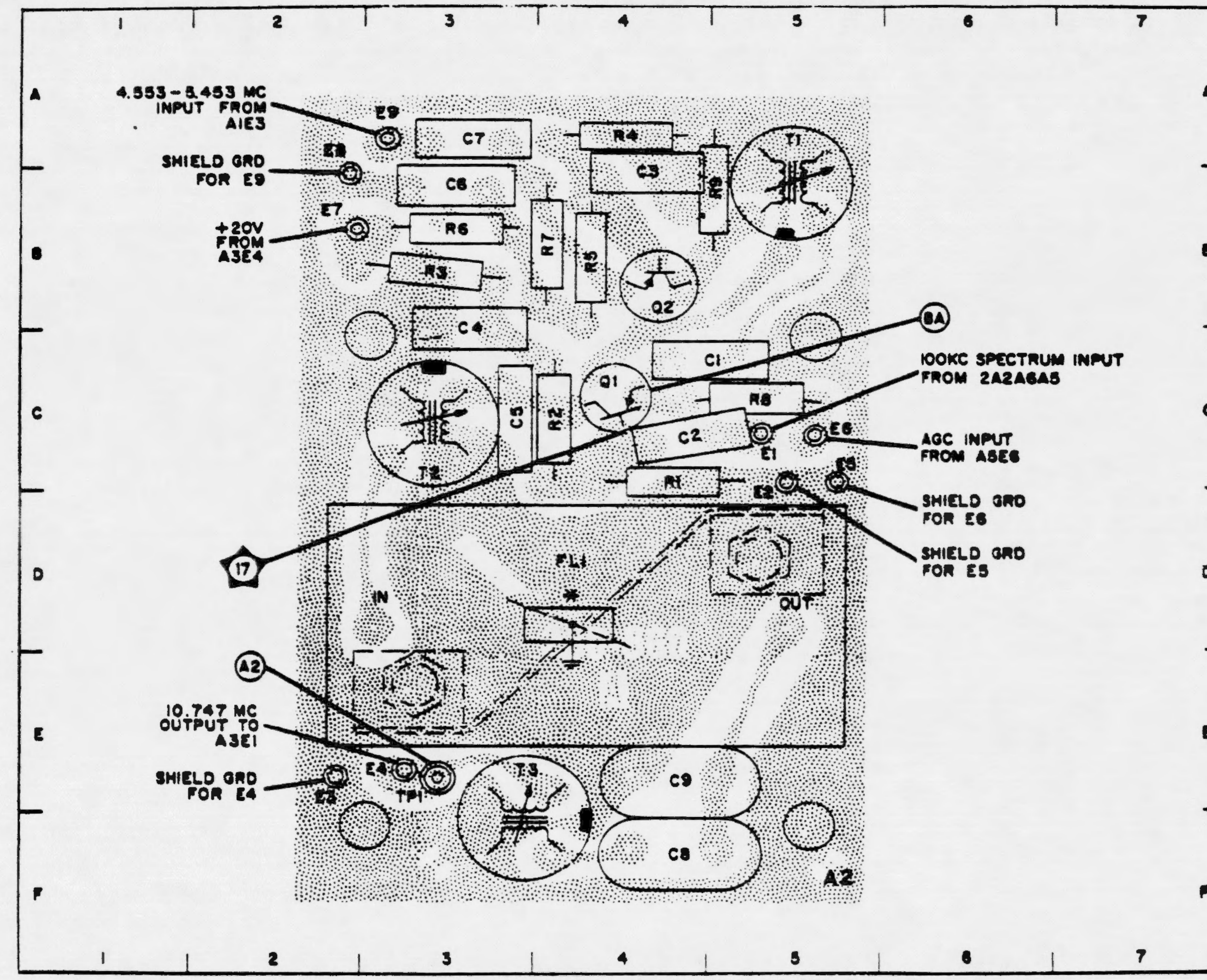


Figure 5-83. 10.747 MC Mixer (Foil Side Up), Component and Test Point Location

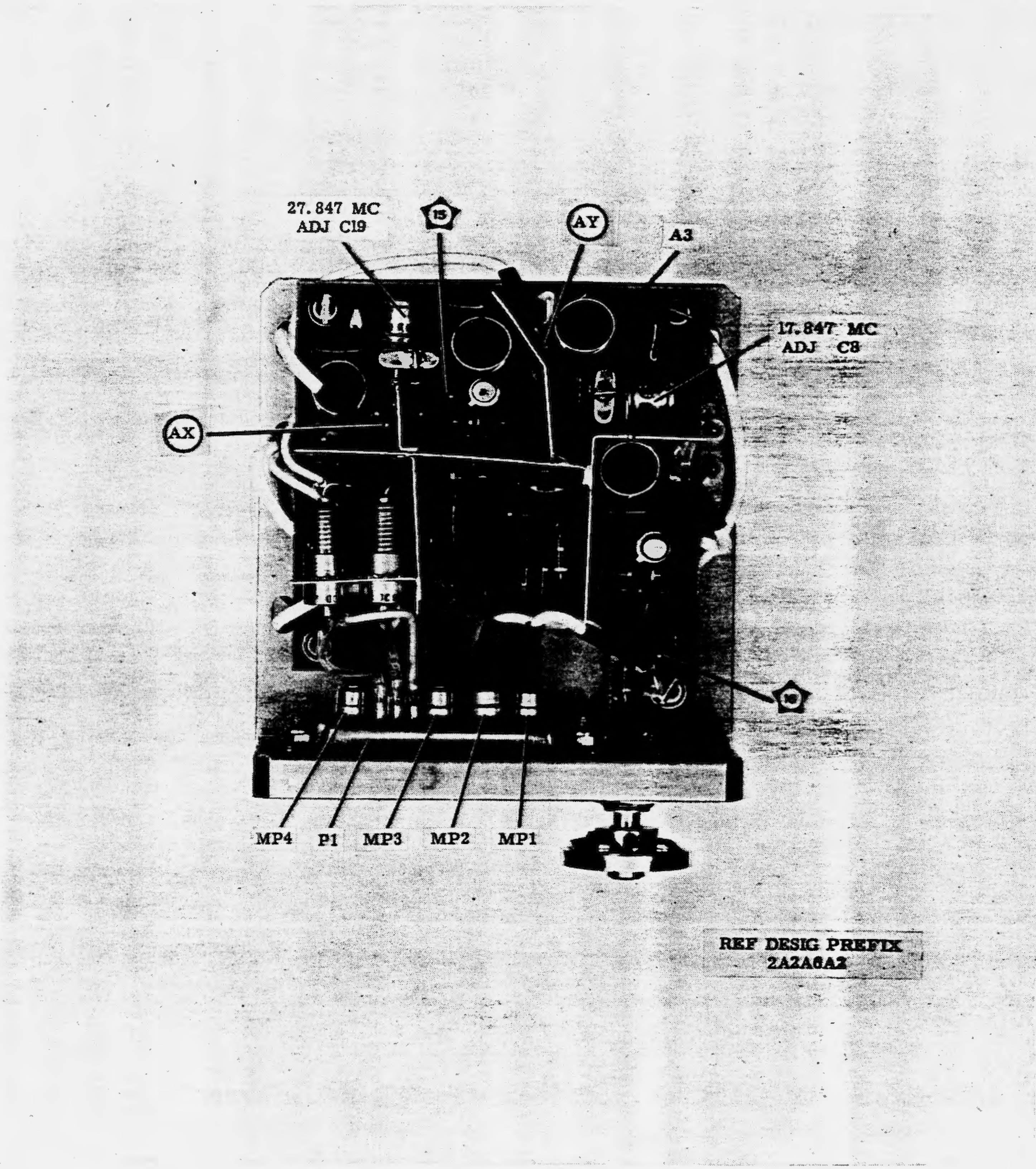


Figure 5-84. 100 KC Synthesizer Electronic Subassembly, Front View, Component Location

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
CR3	4C	E11	5F	R7	4E	T2	5F
E1	7D	E12	6A	R8	4D	T3	4F
E2	7E	E13	6A	R9	3E	T4	2E
E3	2B	Q1	6C	R10	4D	TP1	6B
E4	2D	Q2	4E	R11	5C	TP2	5F
E5	3E	R1	7B	R12	5C	TP3	4E
E6	2E	R2	6C	R13	5D	TP4	3E
E7	4C	R3	6C	R14	4C	Y1	6E
E8	3B	R4	6C	R15	2E	Y2	3F
E9	2D	R5	5E	R16	6A		
E10	5G	R6	4E	T1	6D		

NOTE:
REF. DESIG. PREFIX 2A2A6A2.

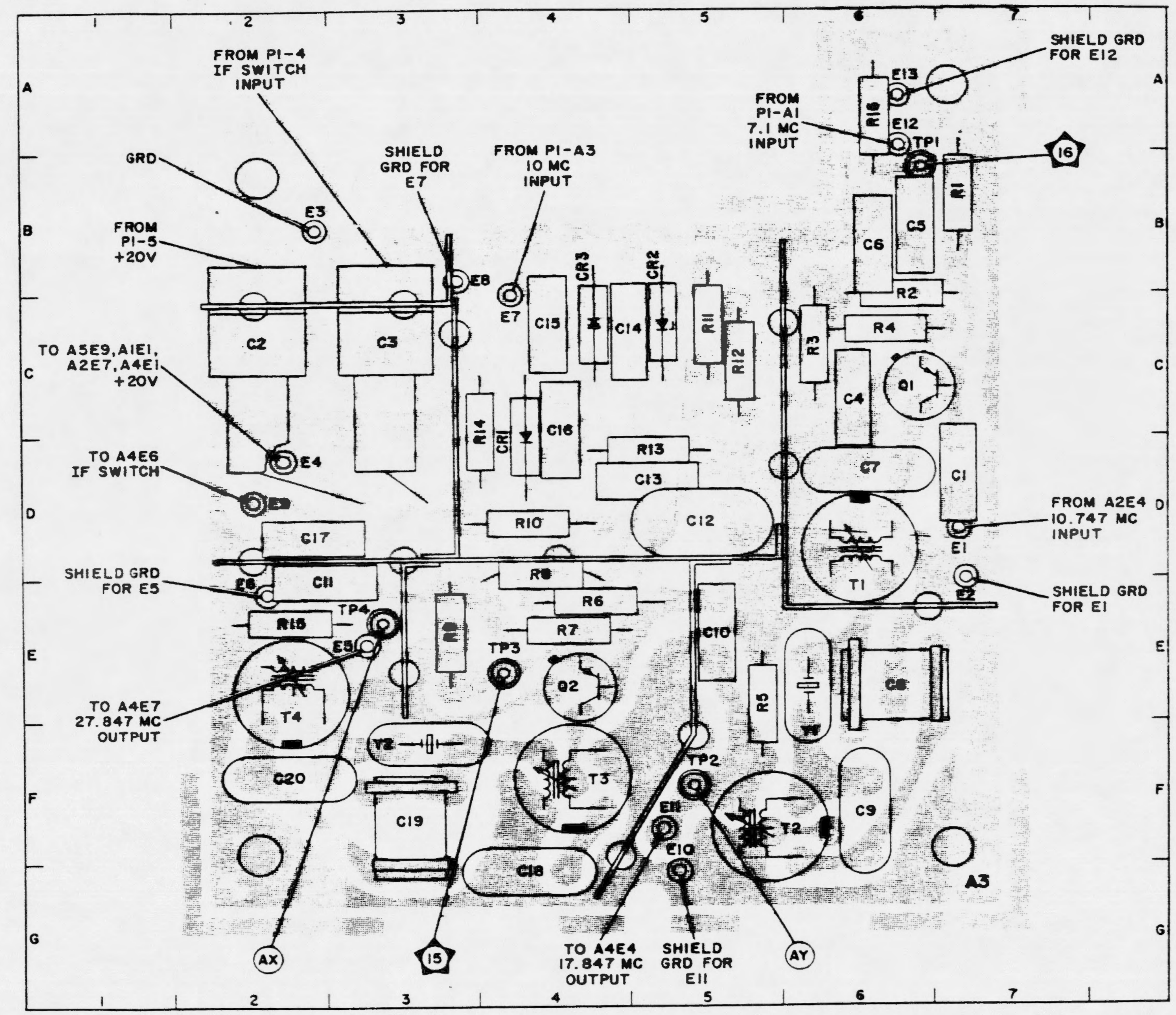
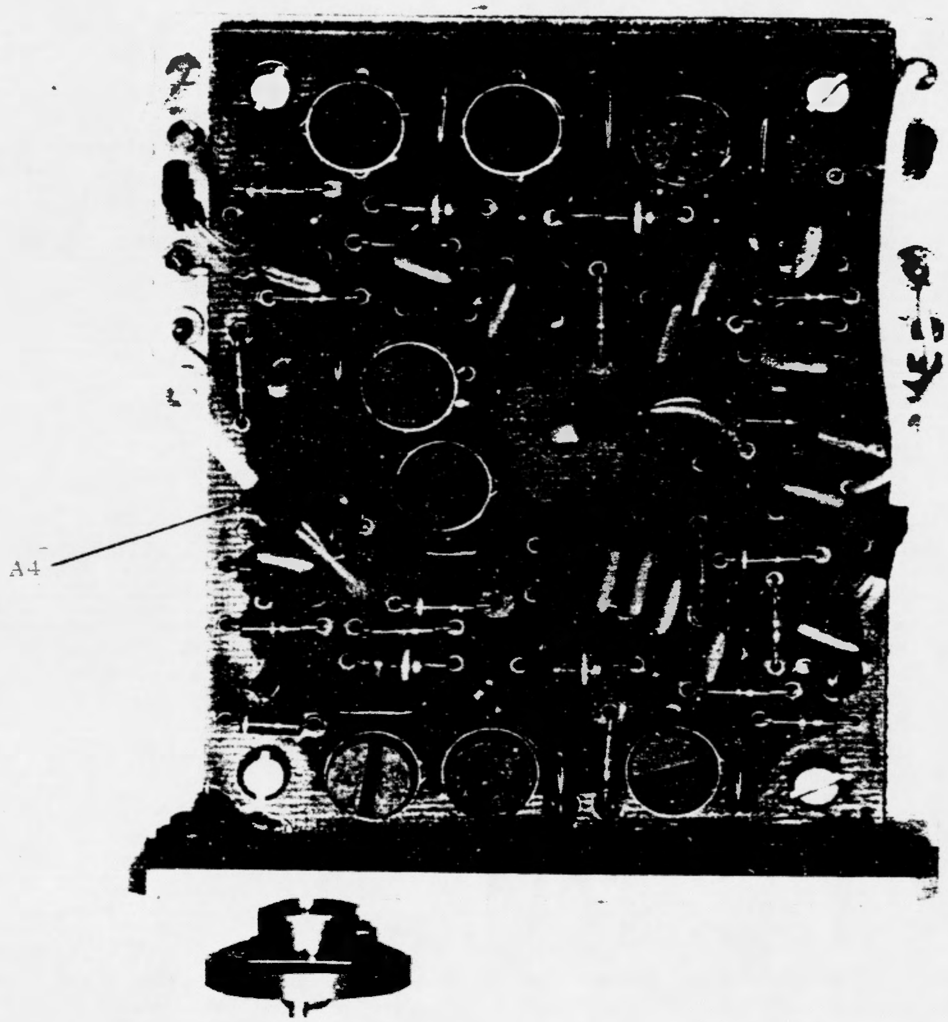
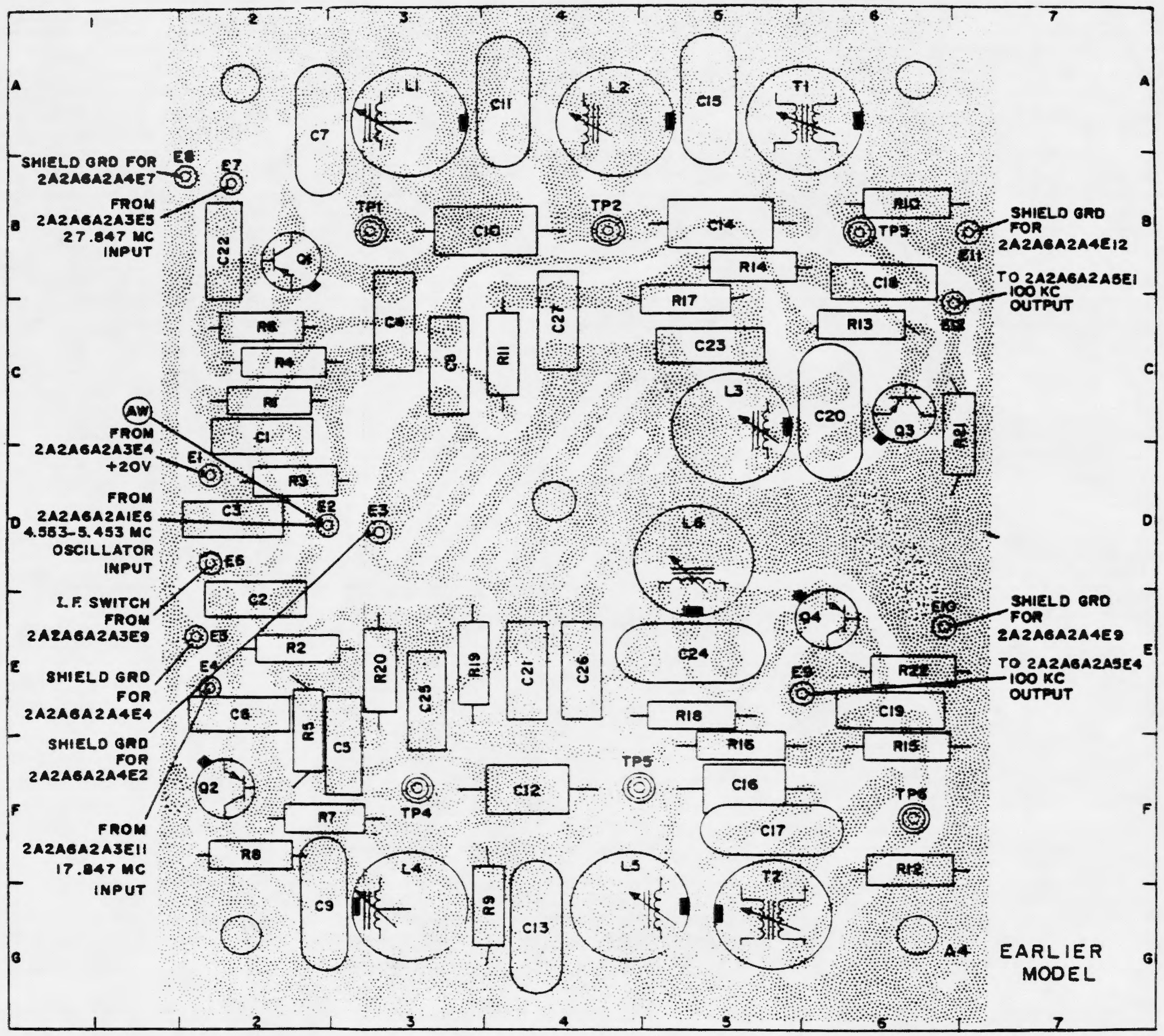


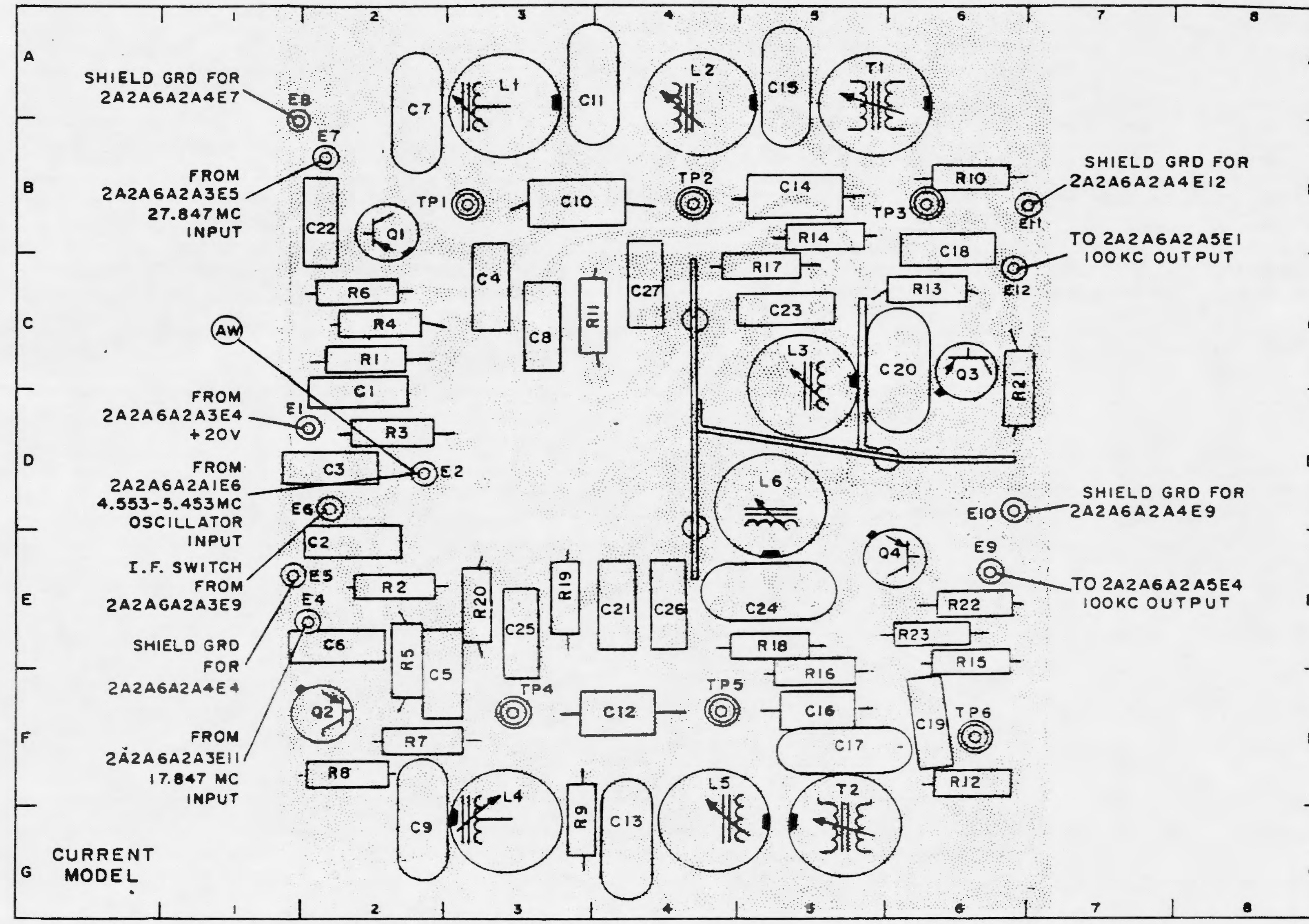
Figure 5-85. 17.847/27.847 MC Mixer (Foil Side Up), Component and Test Point Location



REF. DESIG. PREFIX 2A2A6A2

Figure 5-86. 100 KC Synthesizer Electronic Subassembly, Rear View, Component Location





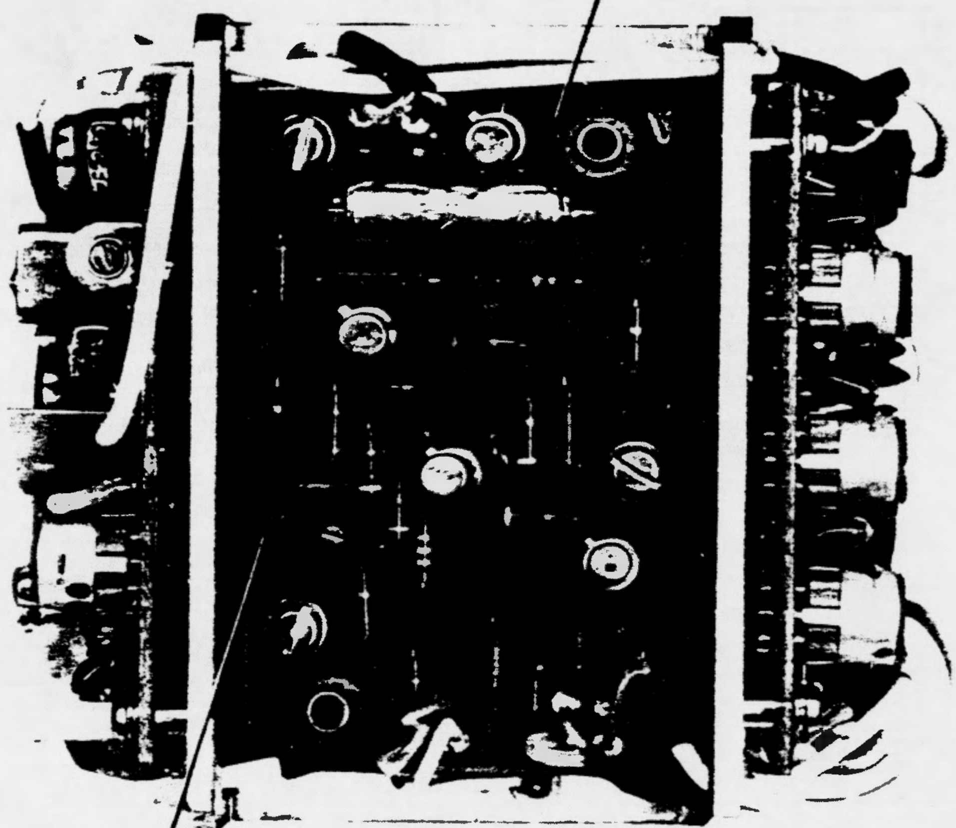
PARTS LOCATION INDEX

REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.
C1	2C	C11	4A	C21	4E	E4	2E	L2	4A	R2	2E	R12	6F	R22	6E
C2	2E	C12	4F	C22	2B	E5	2E	L3	5C	R3	2D	R13	6C	R23	6E
C3	2D	C13	4G	C23	5C	E6	2D	L4	3G	R4	2C	R14	5B	T1	6A
C4	3C	C14	5B	C24	5E	E7	2B	L5	4G	R5	2E	R15	6F OR 6E	T2	5G
C5	3F	C15	5A	C25	3E	E8	2B	L6	5D	R6	2C	R16	5F OR 5E	TP1	3B
C6	2E	C16	5F	C26	4E	E9	6E	Q1	2B	R7	2F	R17	5C	TP2	4B
C7	2A	C17	5F	C27	4C	E10	6E	Q2	2F	R8	2F	R18	5E	TP3	6B
C8	3C	C18	6B	E1	2D	E11	7B	Q3	6C	R9	4G	R19	3E	TP4	3F
C9	2F	C19	6E OR 6F	E2	2D	E12	6C	Q4	6E	R10	6B	R20	3E	TP5	4F
C10	4B	C20	6C	E3	3D	L1	3A	R1	2C	R11	4C	R21	7C	TP6	6F

NOTE:

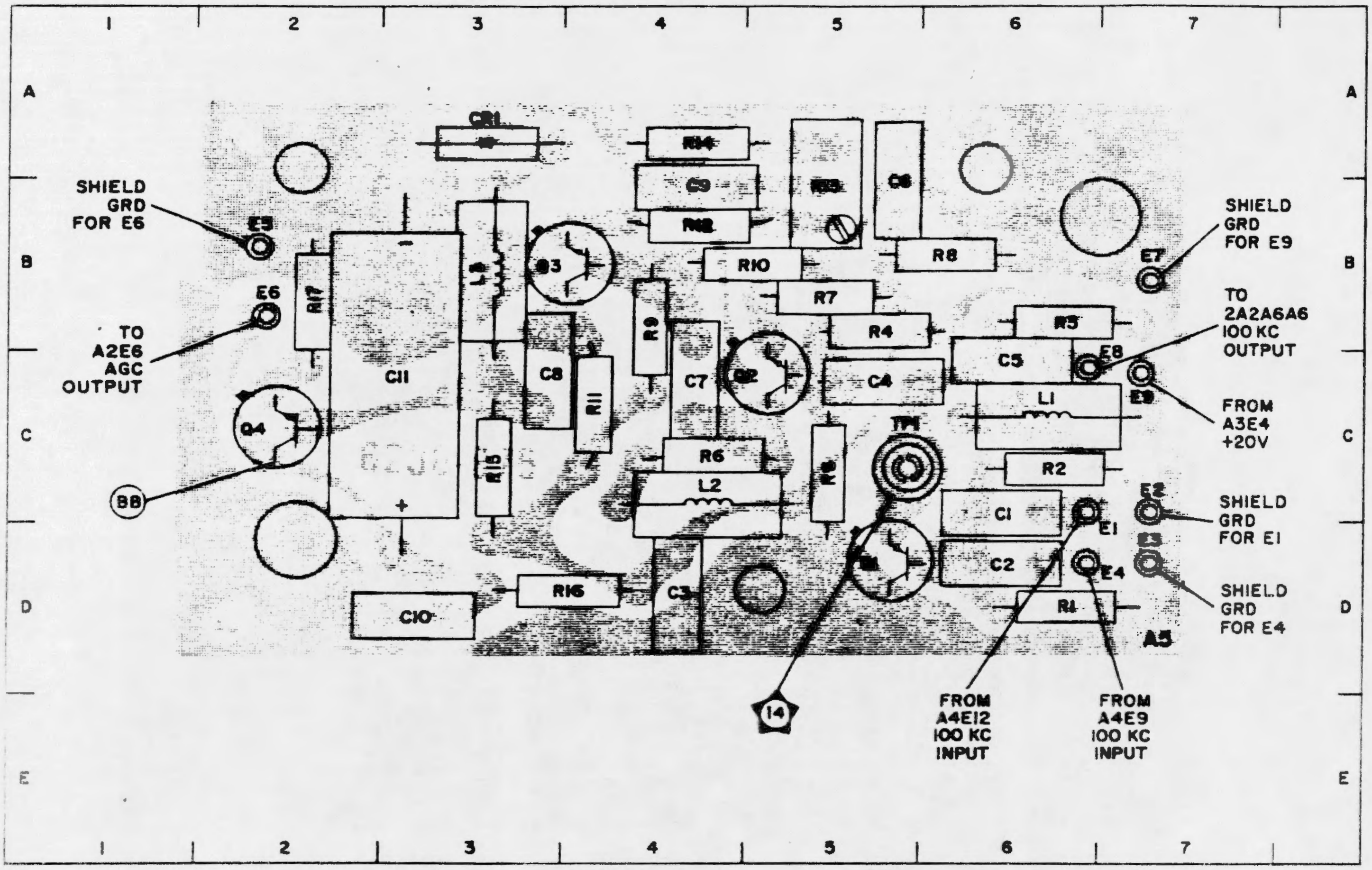
1. COMPONENT REF. DESIG. PREFIX 2A2A6A2A4.
2. VARIATIONS OF HI-BAND/LO-BAND MIXER/AMPLIFIER EXIST DUE TO DESIGN CHANGES. CURRENT MODELS AND EARLIER MODELS ARE INTERCHANGEABLE ON UNIT BASIS. MAJOR CHANGES FOR CURRENT MODEL INCLUDE FOIL PATTERN ALTERATIONS, ADDITION OF RESISTOR R23 AND DELETION OF E3.

Figure 5-87. Hi-Band/Lo-Band Mixer Amplifier (Foil Side Up), Component and Test Point Location



REF DESIG PREFIX 2A2A6A2

Figure 5-88. 100 KC Synthesizer Electronic Subassembly, Top View, Component Location



NOTE:
REF. DESIG. PREFIX 2A2A6A2.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	6C	C11	3C	E9	7C	R3	6B	R13	5B
C2	6D	CR1	3A	L1	6C	R4	5B	R14	4A
C3	4D	E1	6C	L2	4C	R5	5C	R15	3C
C4	5C	E2	7C	L3	3B	R6	4C	R16	4D
C5	6B	E3	7D	Q1	5D	R7	5B	R17	2B
C6	5B	E4	6D	Q2	5C	R8	6B	TP1	5C
C7	4C	E5	2B	Q3	3B	R9	4B		
C8	3C	E6	2B	Q4	2C	R10	5B		
C9	4A	E7	7B	R1	6D	R11	4C		
C10	3D	E8	6C	R2	6C	R12	4B		

Figure 5-89. 10.747 MC Mixer AGC (Foil Side Up), Component and Test Point Location

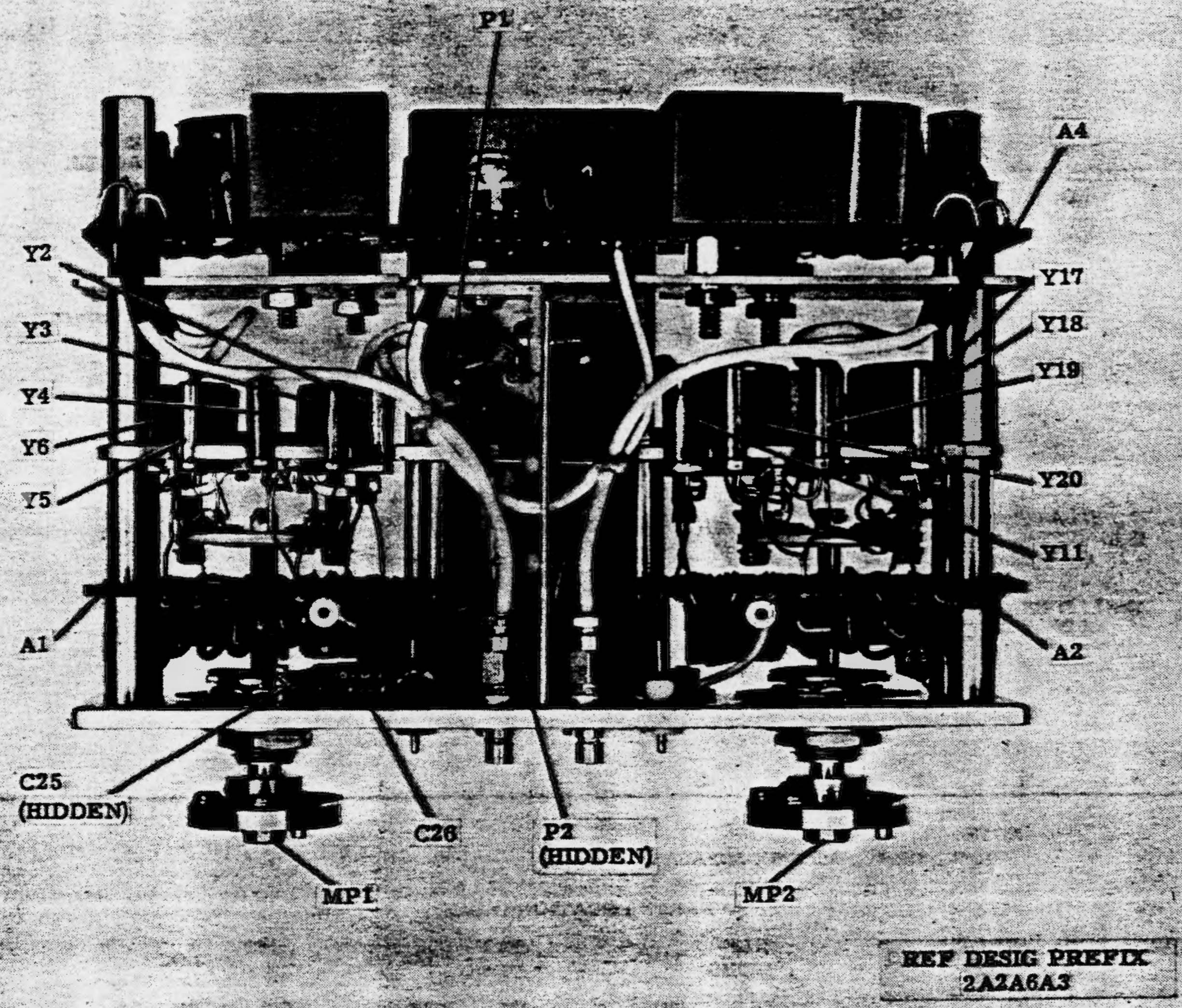
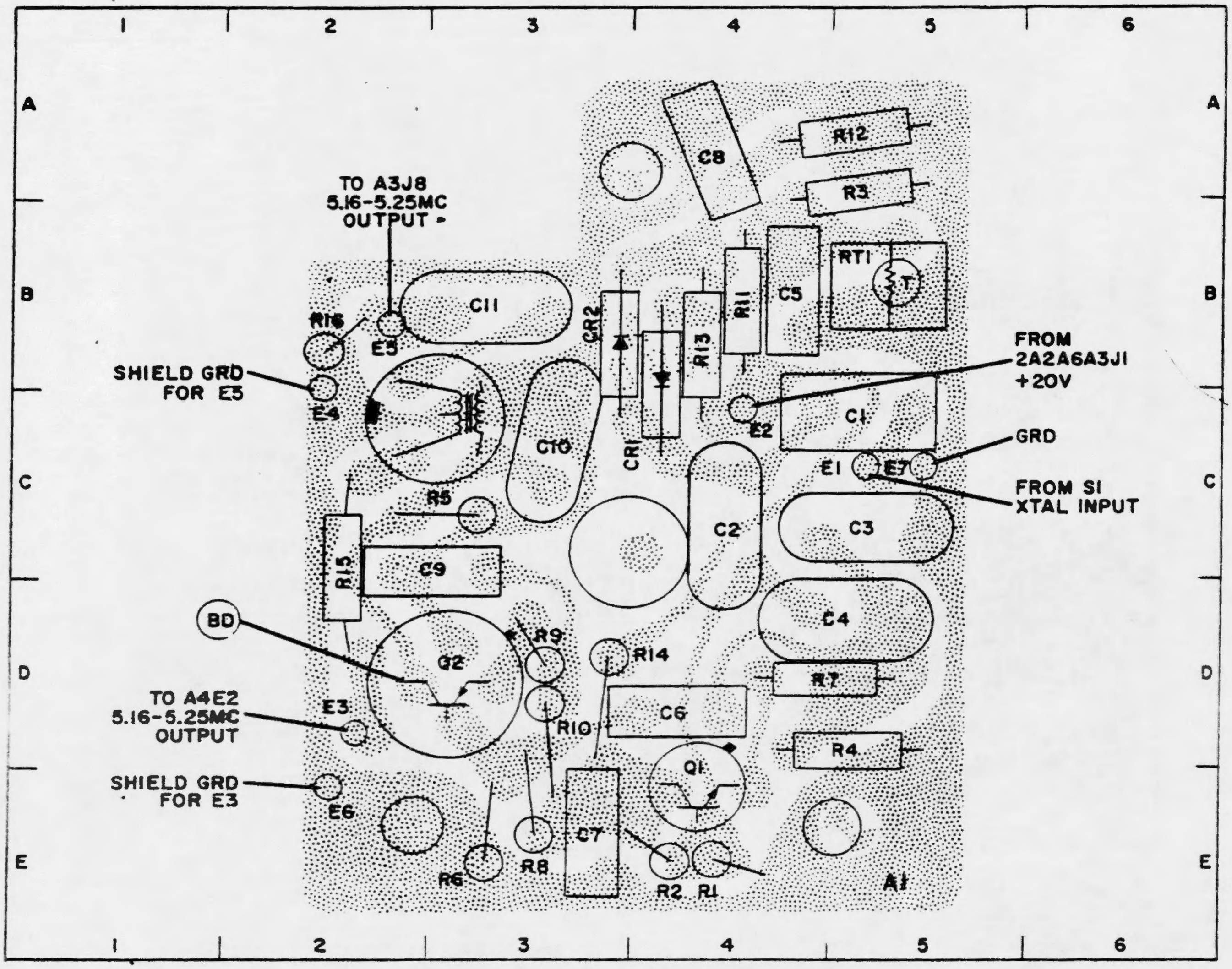


Figure 5-90. 1 and 10 KC Synthesizer Electronic Subassembly, Front View, Component Location

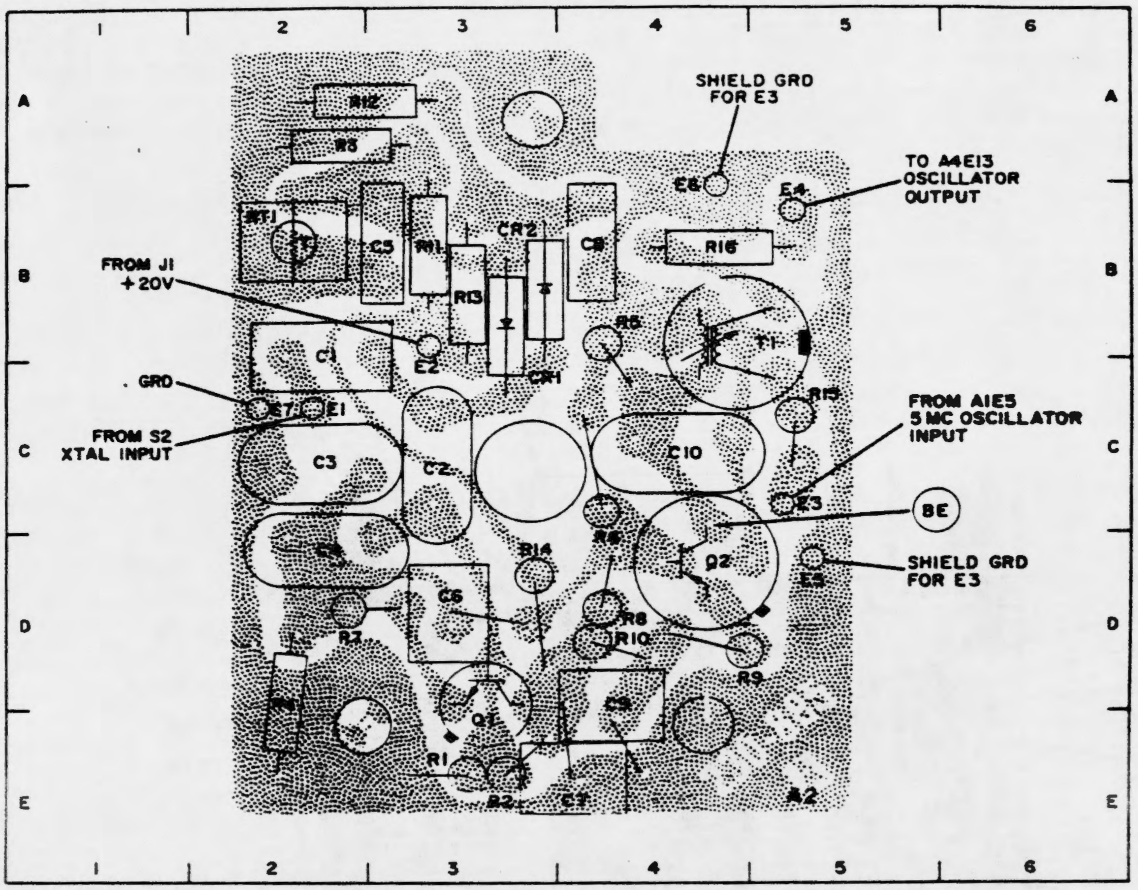


NOTE:
REF. DESIG. PREFIX 2A2A6A3.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	5C	C11	3C	Q1	4E	R9	4D
C2	5D	CR1	4C	Q2	3D	R10	4E
C3	5D	CR2	4C	R1	4E	R11	5B
C4	5D	E1	5C	R2	4E	R12	5B
C5	5B	E2	5C	R3	5B	R13	4C
C6	4E	E3	3E	R4	5E	R14	4E
C7	4E	E4	3C	R5	3D	R15	3D
C8	4B	E5	3B	R6	3E	R16	3C
C9	3D	E6	3E	R7	5D	RT1	5B
C10	4C	E7	6C	R8	4E	T1	3C

Figure 5-91. 5.25 MC to 5.16 MC Oscillator (Foil Side Up), Component and Test Point Location

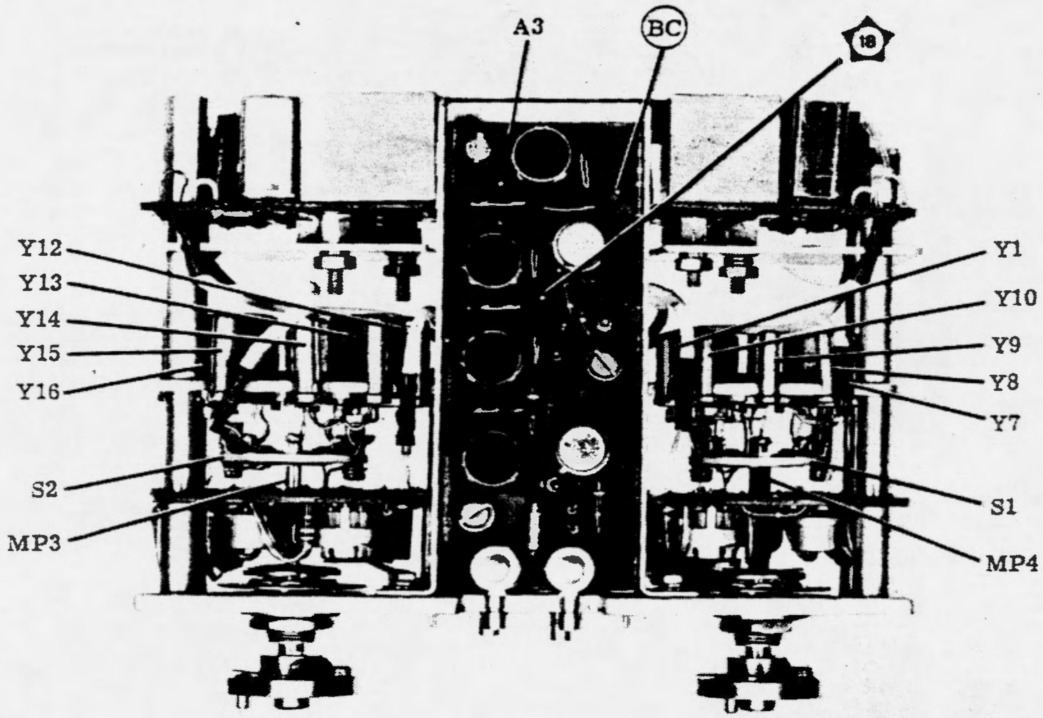


PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
C1	2C	Q2	4D
C2	3C	R1	3E
C3	2C	R2	3E
C4	2D	R3	2A
C5	3B	R4	2E
C6	3D	R5	4C
C7	4E	R6	4C
C8	4B	R7	2D
C9	4E	R8	4D
C10	4C	R9	4D
CR1	3B	R10	4D
CR2	3B	R11	3B
E1	2C	R12	2A
E2	3C	R13	3B
E3	5B	R14	3D
E4	5D	R15	4B
E5	4B	R16	5C
E6	5D	RT1	2B
E7	2C	T1	5C
Q1	3E		

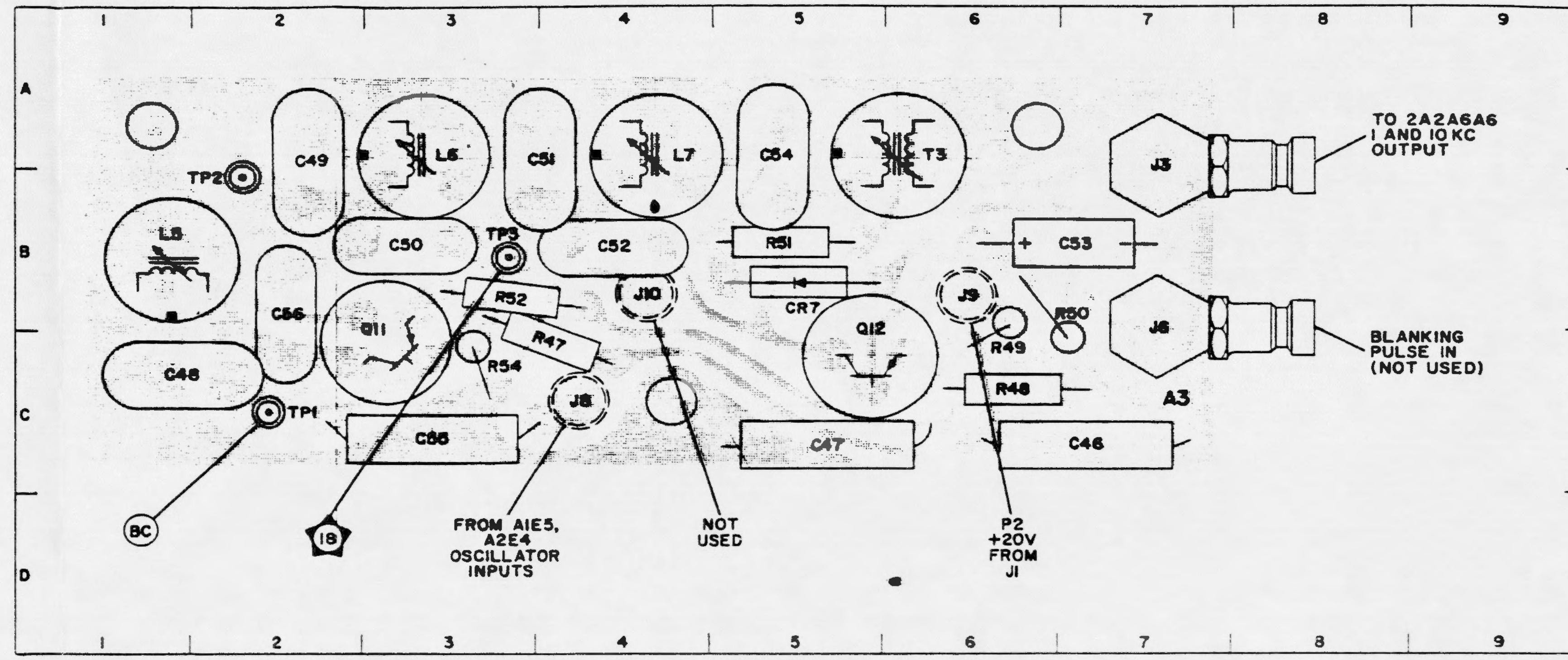
NOTE:
REF. DESIG. PREFIX 2A2A6A3.

Figure 5-92. 1.850 MC to 1.859 MC Oscillator (Foil Side Up), Component and Test Point Location



REF DESIG PREFIX
2A2A6A3

Figure 5-93. 1 and 10 KC Synthesizer Electronic Subassembly, Rear View, Component Location

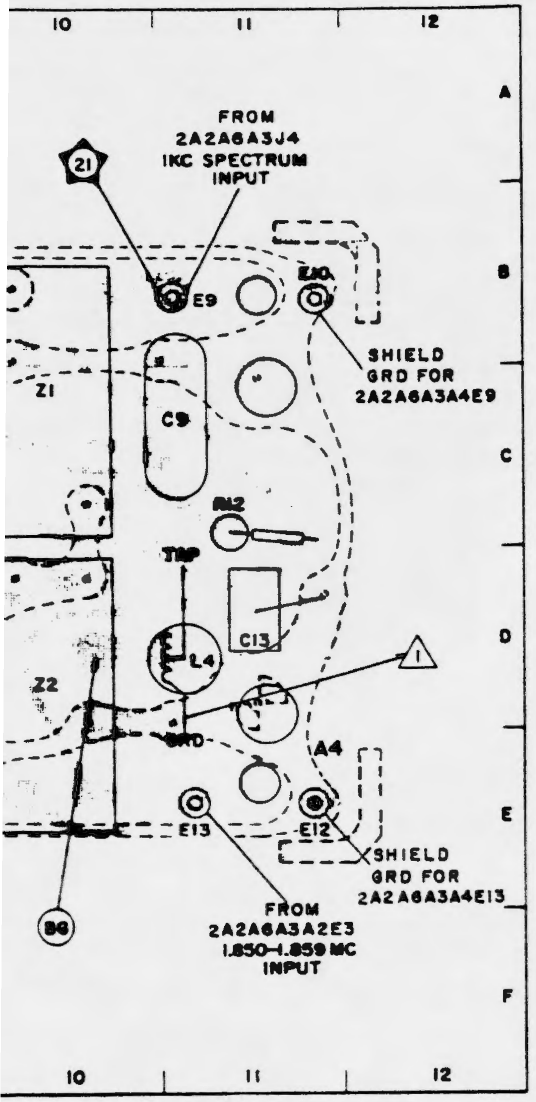


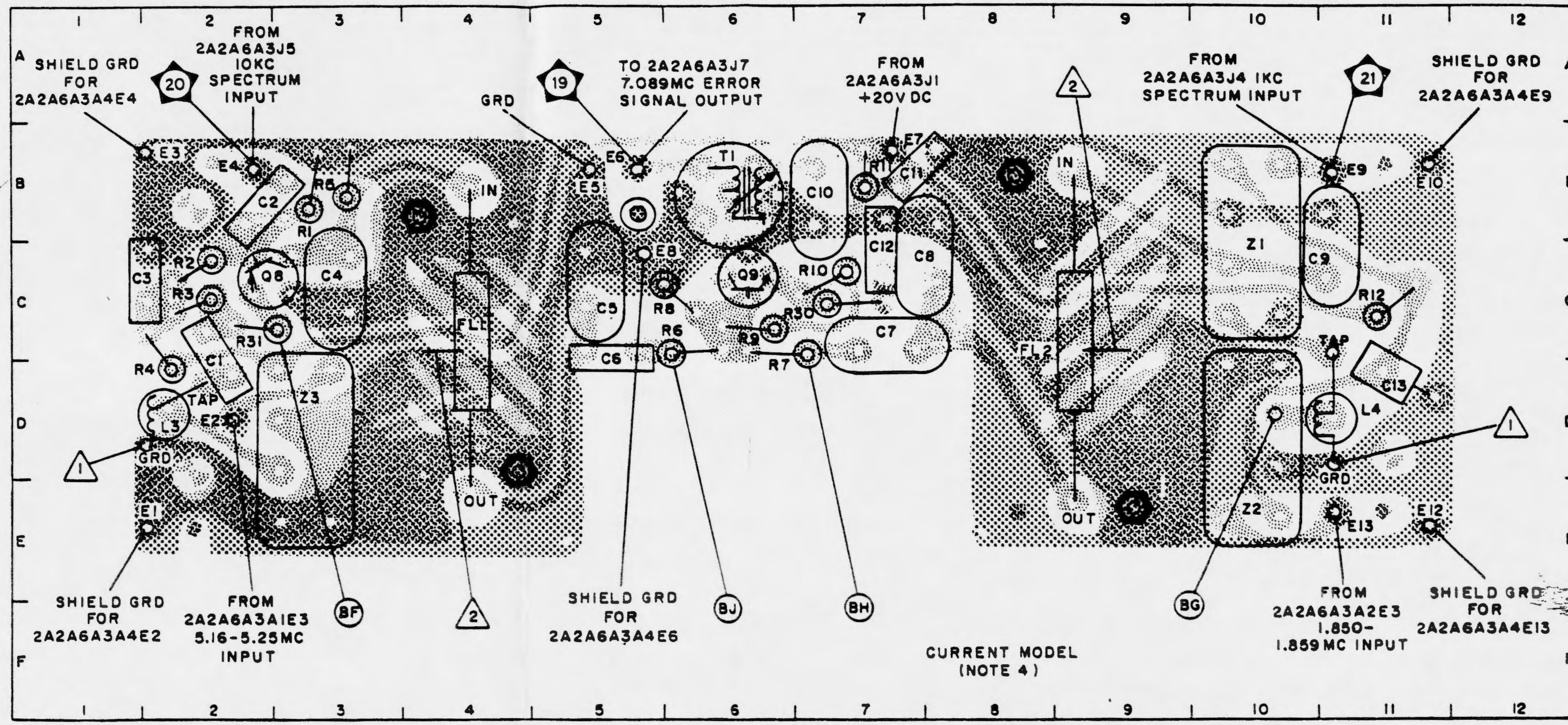
NOTE:
REF. DESIG. PREFIX 2A2A6A3.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C46	7C	CR7	5B	R47	4C
C47	5C	J3	7A	R48	6C
C48	1C	J6	7B	R49	6B
C49	2A	J8	4C	R50	7C
C50	3B	J9	6B	R51	5B
C51	4A	J10	4B	R52	3B
C52	4B	L5	1B	R54	3C
C53	7B	L6	3A	T3	6A
C54	5A	L7	4A	TP1	2C
C55	3C	Q11	3C	TP2	2B
C56	2B	Q12	5C	TP3	3B

Figure 5-94. 1 and 10 KC Synthesizer Output Circuit (Foil Side Up), Component and Test Point Location





NOTES:

1. COMPONENT REF. DESIG. PREFIX 2A2A6A3A4.
2. △1 THIS CONNECTION IS ON OPPOSITE SIDE OF BOARD.
3. △2 GROUNDED SHIELD BETWEEN INPUT AND OUTPUT.
4. VARIATIONS OF 7.089 MC MIXER EXIST DUE TO EQUIPMENT DESIGN CHANGES. CURRENT MODEL AND EARLIER MODEL ARE INTERCHANGEABLE ON UNIT BASIS BUT INDIVIDUAL COMPONENTS ARE NOT NECESSARILY INTERCHANGEABLE. MAJOR CHANGES FOR CURRENT MODEL INCLUDE FOIL PATTERN ALTERATIONS AND ADDITION OF RESISTORS R30 AND R31.

PARTS LOCATION INDEX

REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.
C1	2D	E3	2B	Q9	6C	T1	6B
C2	2B	E4	2B	R1	3B	Z1	10C
C3	2C	E5	5B	R2	2C	Z2	10D
C4	3C	E6	5B	R3	2C	Z3	3D
C5	5C	E7	7B	R4	2D		
C6	5D	E8	5C	R5	3B		
C7	7C	E9	11B	R6	5C		
C8	7C	E10	11B	R7	7C		
C9	10C	E12	11E	R8	5C		
C10	7B	E13	11E	R9	6C		
C11	7B	FL1	4C	R10	7C		
C12	7C	FL2	8C	R11	7B		
C13	11D	L3	2D	R12	11C		
E1	2E	L4	11D	R30	7C		
E2	2D	Q8	2C	R31	2C		

Figure 5-96. 7.089 MC Mixer (Component Side Down), Component and Test Point Location

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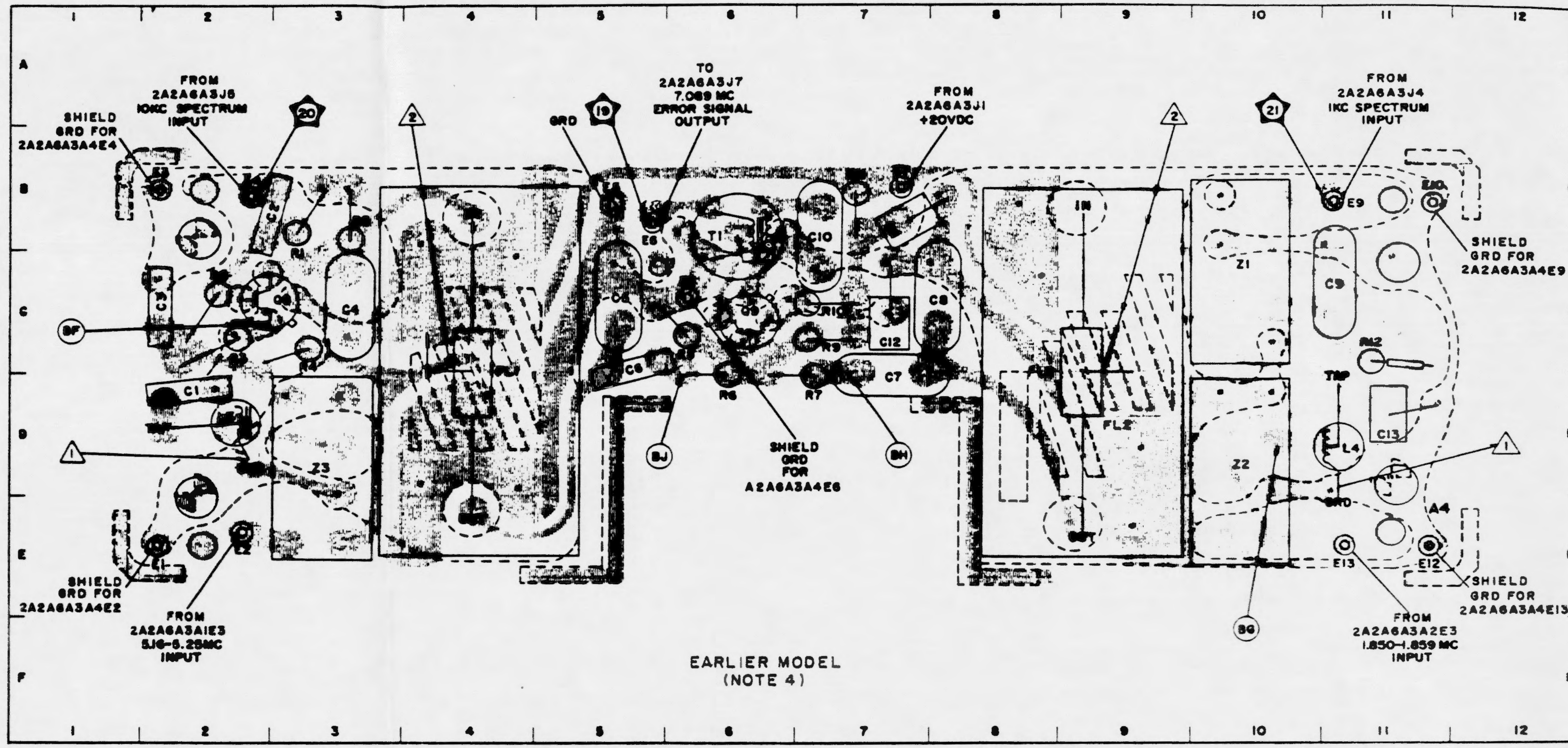
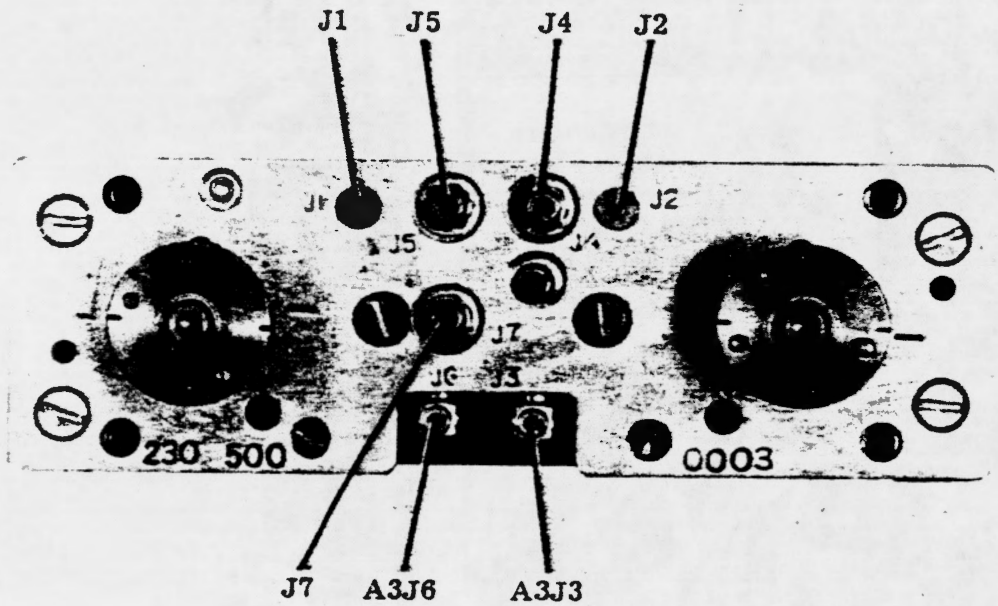


PARTS LOCATION INDEX

REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.	REF. DESIG.	LOC.
C1	2D	C9	11C	E4	2B	E13	10E	R2	2C	R10	7C
C2	2B	C10	7B	E5	5B	FL1	4C	R3	2C	R11	7B
C3	2C	C11	7B	E6	5B	FL2	9C	R4	3C	R12	11C
C4	3C	C12	7C	E7	7B	L3	2D	R5	3B	T1	6B
C5	5C	C13	11D	E8	6C	L4	11D	R6	6D	Z1	10C
C6	5C	E1	2E	E9	11B	Q8	3C	R7	7D	Z2	10D
C7	7D	E2	2E	E10	11B	Q9	6C	R8	6C	Z3	3D
C8	8C	E3	2B	E12	11E	R1	3B	R9	7C		

NOTES:

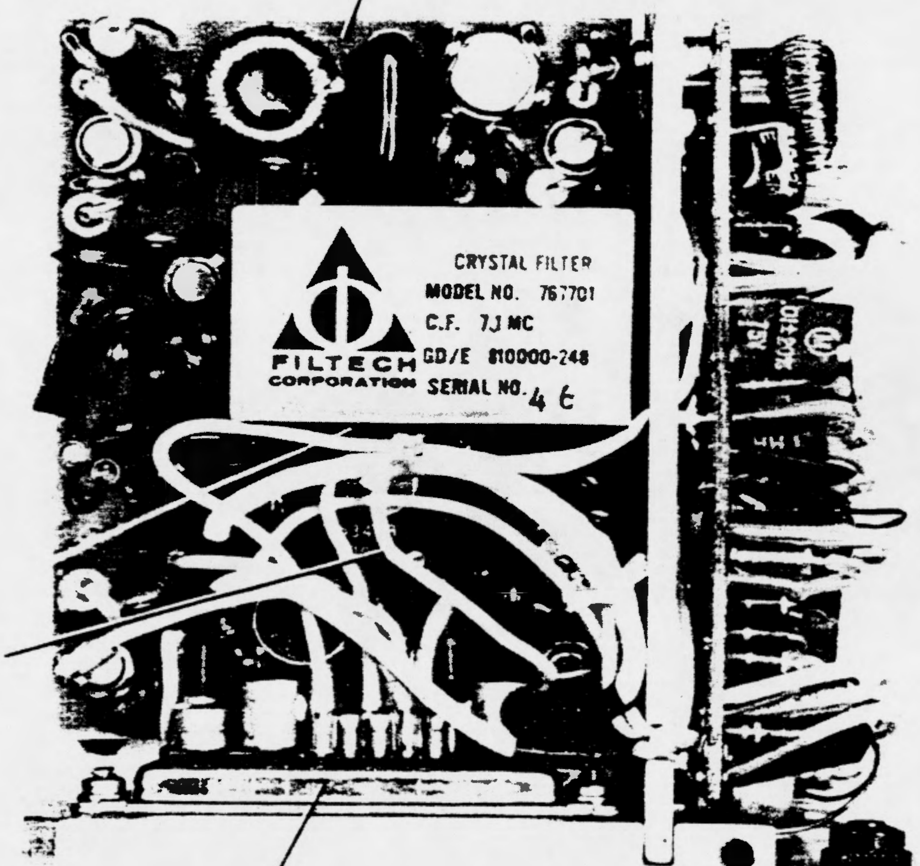
1. COMPONENT REF. DESIG. PR
2. △1 THIS CONNECTION IS ON C
3. △2 GROUNDED SHIELD BETWE
4. VARIATIONS OF 7.089 MC M
CHANGES. CURRENT MOD
CHANGEABLE ON UNIT BA
NOT NECESSARILY INTERC
CURRENT MODEL INCLUD
ADDITION OF RESISTORS R



REF DESIG PREFIX
2A2A6A3

Figure 5-97. 1 and 10 KC Synthesizer Electronic Subassembly, Bottom View, Component Location

A1



GAIN
ADJ
R16

P1

REF DESIG PREFIX
2A2A6A4

Figure 5-98. 500 CPS Synthesizer Electronic Subassembly, Left Side View, Component Location

NOTE:
REF. DESIG. PREFIX 2A2A6A4.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	5G	E5	5F	R11	3F
C2	6E	E6	3G	R12	4G
C3	6D	E7	5F	R13	4F
C4	6C	E8	5F	R14	3E
C5	5E	E9	5F	R15	3E
C6	2E	E10	2B	R16	4F
C7	2E	FL1	3D	R17	6C
C8	3F	L1	4G	R18	4C
C9	3F	L2	5F	R19	5B
C10	3E	Q1	5C	R20	6A
C11	5E	Q2	2F	R21	3B
C12	4E	Q3	4E	R22	3A
C13	6F	Q4	5B	R23	3C
C14	6C	Q5	3B	R24	3B
C15	6B	R1	5D	R25	3B
C16	6A	R2	5D	R26	3A
C17	4B	R3	6D	T1	4F
C18	2C	R4	6D	T2	5B
C19	3C	R5	5C	TP1	5D
C20	2B	R6	5D	TP2	5E
E1	6E	R7	2F	TP3	6C
E2	6E	R8	2E	TP4	3E
E3	5G	R9	2F	TP5	5G
E4	4G	R10	3G	TP6	2A

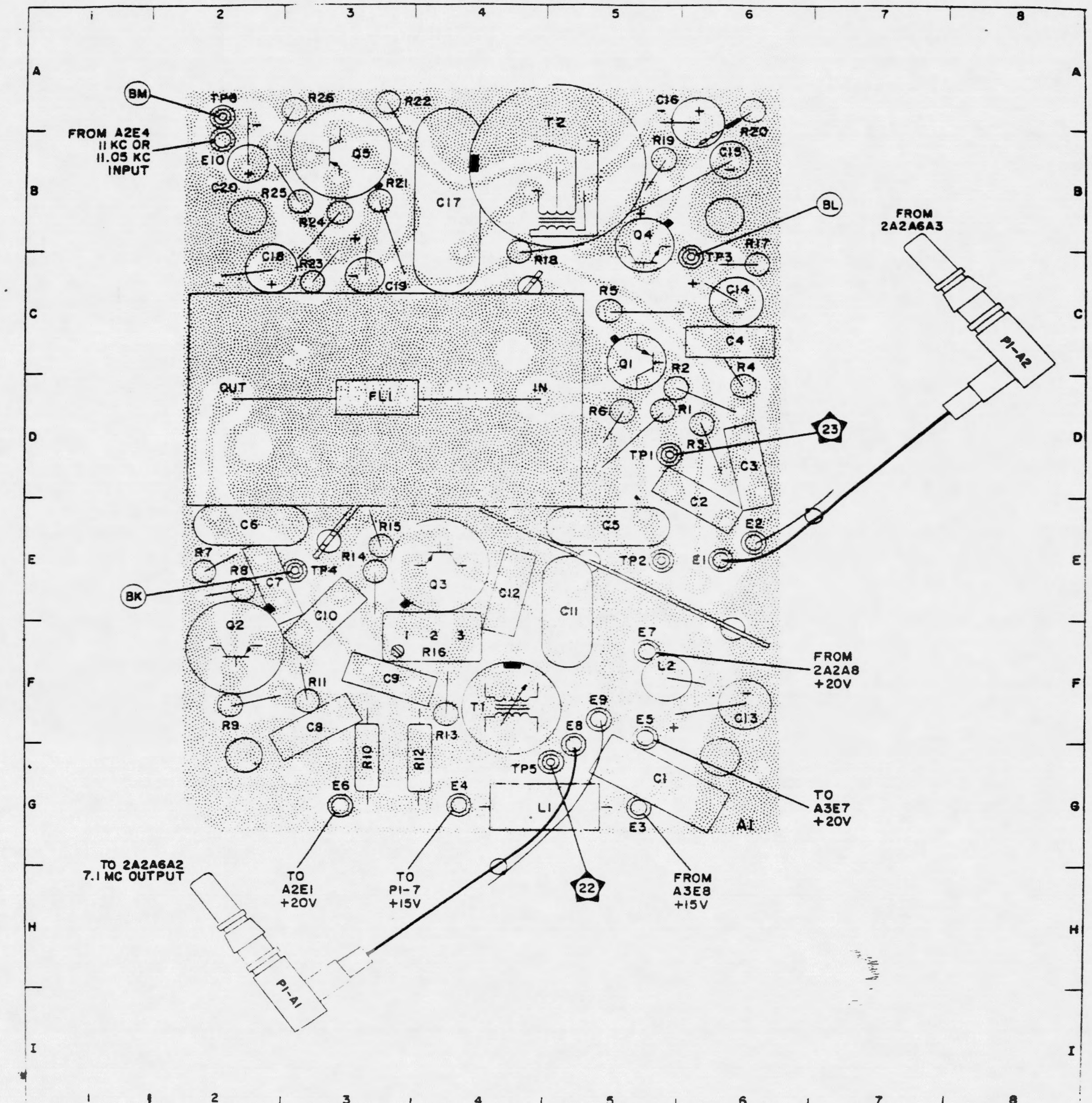
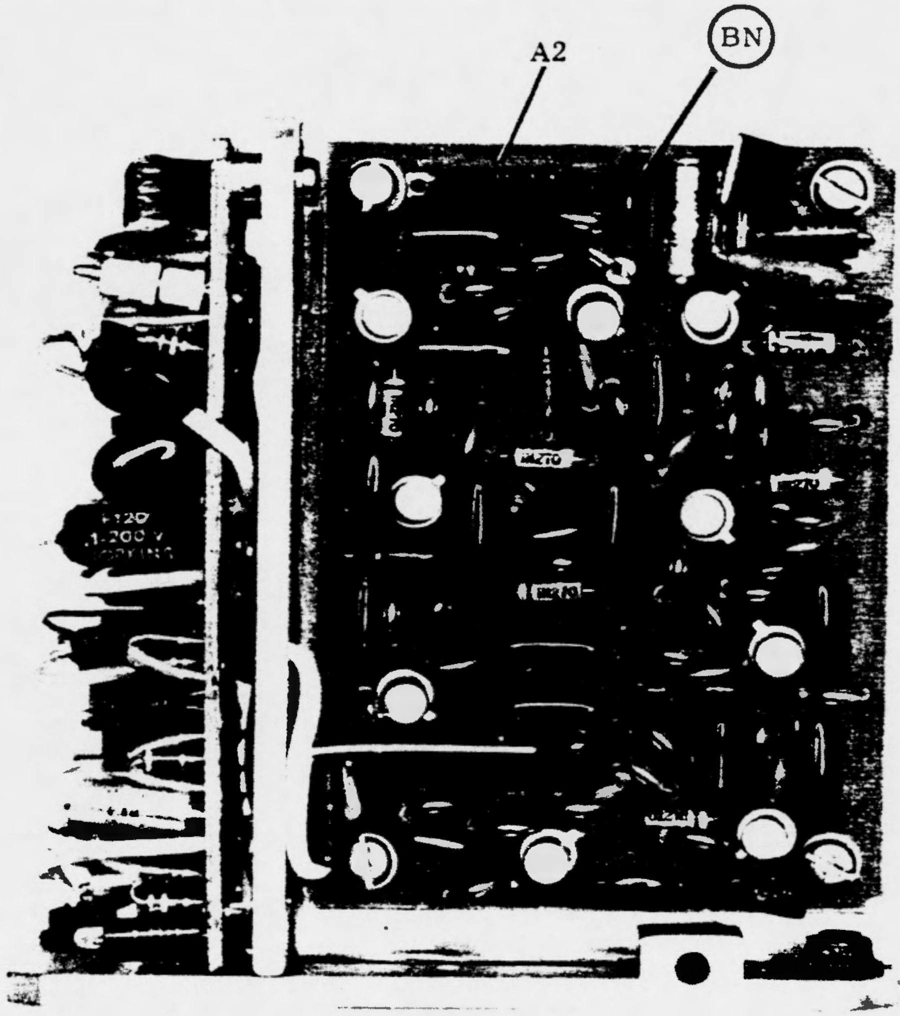


Figure 5-99. 7.1 MC Mixer (Foil Side Up), Component and Test Point Location



REF DESIG PREFIX
2A2A6A4

Figure 5-100. 500 CPS Synthesizer Electronic Subassembly, Right Side View, Component Location

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PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	8C	CR1	7C	Q9	2D	R25	4E
C2	7C	CR2	2E	R1	7C	R26	3E
C3	2E	CR3	2C	R2	2F	R27	4F
C4	2E	CR4	3C	R3	3D	R28	3F
C5	3D	CR5	6B	R4	3D	R29	5D
C6	2D	CR6	5B	R5	2E	R30	6E
C7	2C	CR7	4D	R6	3D	R31	4E
C8	3C	CR8	4D	R7	4C	R32	4F
C9	3B	CR9	5E	R8	3C	R33	6D
C10	4B	CR10	6D	R9	2D	R34	6D
C11	6B	CR11	6F	R10	3C	R35	7E
C12	6C	CR12	4C	R11	2C	R36	7D
C13	6D	E1	7B	R12	4C	R37	6E
C14	5D	E2	2F	R13	4D	R38	6F
C15	3E	E3	2F	R14	3B	R39	6E
C16	4F	E4	8C	R15	3B	R40	6E
C17	5E	L1	7C	R16	5B	R41	7D
C18	5F	Q1	2C	R17	6C	TP1	2D
C19	7F	Q2	4C	R18	5C	TP2	3B
C20	7E	Q3	6C	R19	6C	TP3	5D
C21	6E	Q4	5C	R20	6B	TP4	7D
C22	7E	Q5	3E	R21	4B	TP5	5E
C23	7D	Q6	5E	R22	5C		
C24	3D	Q7	6D	R23	6C		
C25	4D	Q8	6F	R24	5D		

NOTES:
1. REF. DESIG. PREFIX 2A2A6A4
2. 1 VERTICALLY MOUNTED DIODES CR2, CR7, CR12 HAVE ANODE CONNECTIONS TO BOARD, CATHODE CONNECTIONS UP.

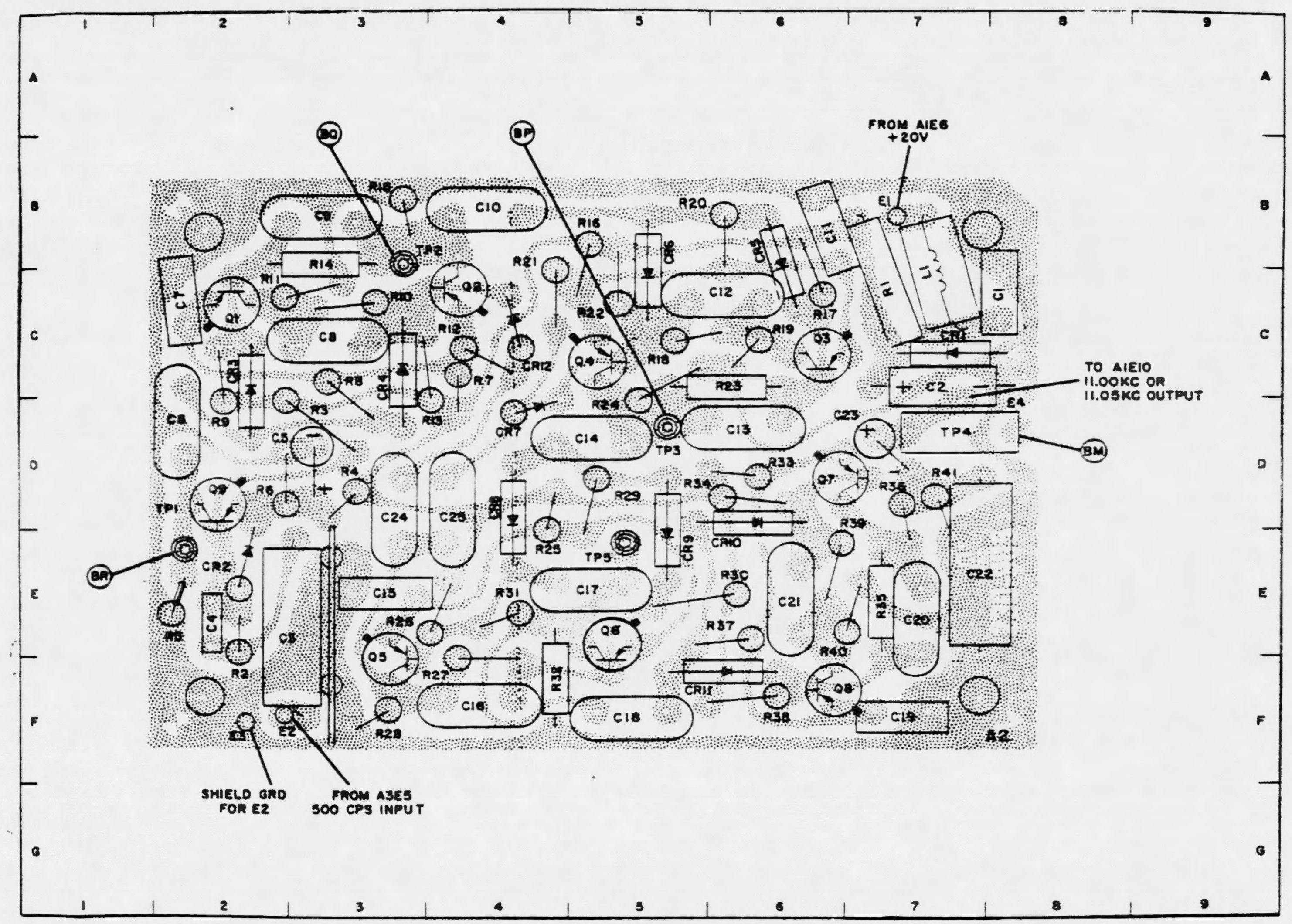
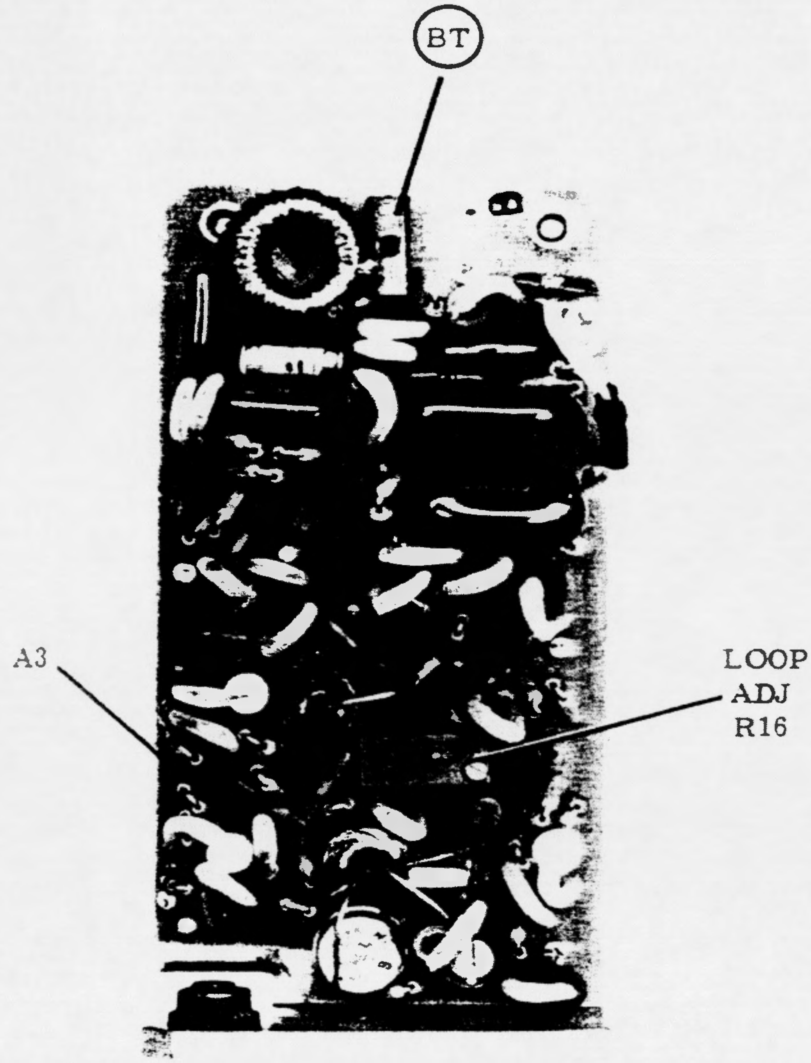


Figure 5-101. Divide-By-Ten Multivibrators (Foil Side Up), Component and Test Point Location



REF DESIG PREFIX 2A2A6A4

Figure 5-102. 500 CPS Synthesizer Electronic Subassembly, Front View, Component Location

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REF DESIG	LOC
R.5	6F
R16	7E
R17	7F
R18	7F
R19	8F
R20	9F
R21	7E
R22	7D
R23	8D
R24	7C
R25	7D
R26	6F
R27	7C
R28	8D
R29	7C
R30	8C
R31	9E
RT1	5D
T1	8E
TP1	3E

IT.

R5, CR9 ANODE CONNECTIONS TO
CR7, CR8 CATHODE CONNECTIONS

ARIABLE CAPACITOR. CR2 AND
TOP END OF COMPONENTS.

CONNECTION ON TOP AND ONE

DE.

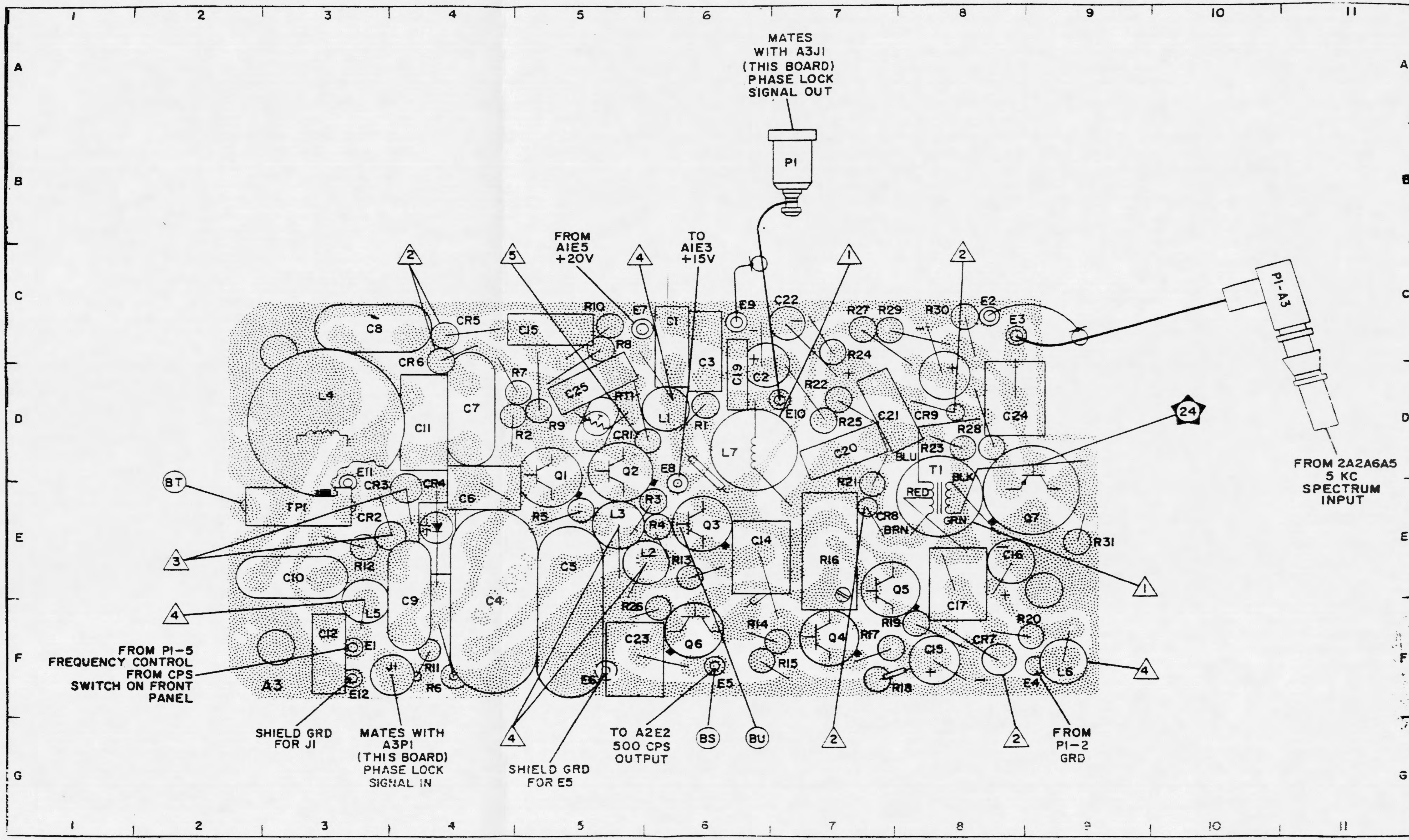

Figure 5-103. 500 CPS Oscillator (Foil Side Up), Component and Test Point Location

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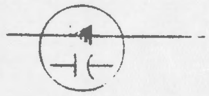
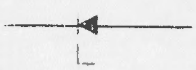
PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	6C	CR1	6D	L4	3D	R15	6F
C2	6D	CR2	4E	L5	3F	R16	7E
C3	6C	CR3	4E	L6	9F	R17	7F
C4	4E	CR4	4E	L7	6D	R18	7F
C5	5E	CR5	4C	Q1	5D	R19	8F
C6	4E	CR6	4C	Q2	5D	R20	9F
C7	4D	CR7	8F	Q3	6E	R21	7E
C8	3C	CR8	7E	Q4	7F	R22	7D
C9	4E	CR9	8D	Q5	7E	R23	8D
C10	3E	E1	3F	Q6	6F	R24	7C
C11	4D	E2	8C	Q7	9E	R25	7D
C12	3F	E3	8C	R1	6D	R26	6F
C13	5C	E4	9F	R2	4D	R27	7C
C14	6E	E5	6F	R3	6E	R28	8D
C15	8F	E6	5F	R4	6E	R29	7C
C16	8E	E7	5C	R5	5E	R30	8C
C17	8F	E8	6E	R6	4F	R31	9E
C18	8D	E9	6C	R7	5D	RT1	5D
C19	6D	E10	7D	R8	5C	T1	8E
C20	7D	E11	3D	R9	5D	TP1	3E
C21	7D	E12	3F	R10	5C		
C22	7C	J1	4F	R11	4F		
C23	5F	L1	6D	R12	3E		
C24	8D	L2	6E	R13	6E		
C25	5D	L3	5E	R14	7F		

NOTES:

1. REF. DESIG. PREFIX 2A2A6A4.
2. 1 ALL CONNECTIONS ARE FROM TOP END OF COMPONENT.
3. 2  VERTICALLY MOUNTED DIODES. CR5, CR9 ANODE CONNECTIONS TO BOARD, CATHODE ON TOP. CR6, CR7, CR8 CATHODE CONNECTIONS TO BOARD, ANODE ON TOP.
4. 3  VERTICALLY MOUNTED VOLTAGE VARIABLE CAPACITOR. CR2 AND CR3 ANODE CONNECTIONS ARE ON TOP END OF COMPONENTS.
5. 4 VERTICALLY MOUNTED COIL. ONE CONNECTION ON TOP AND ONE ON BOTTOM OF EACH COMPONENT.
6. 5  VERTICALLY MOUNTED ZENIER DIODE.

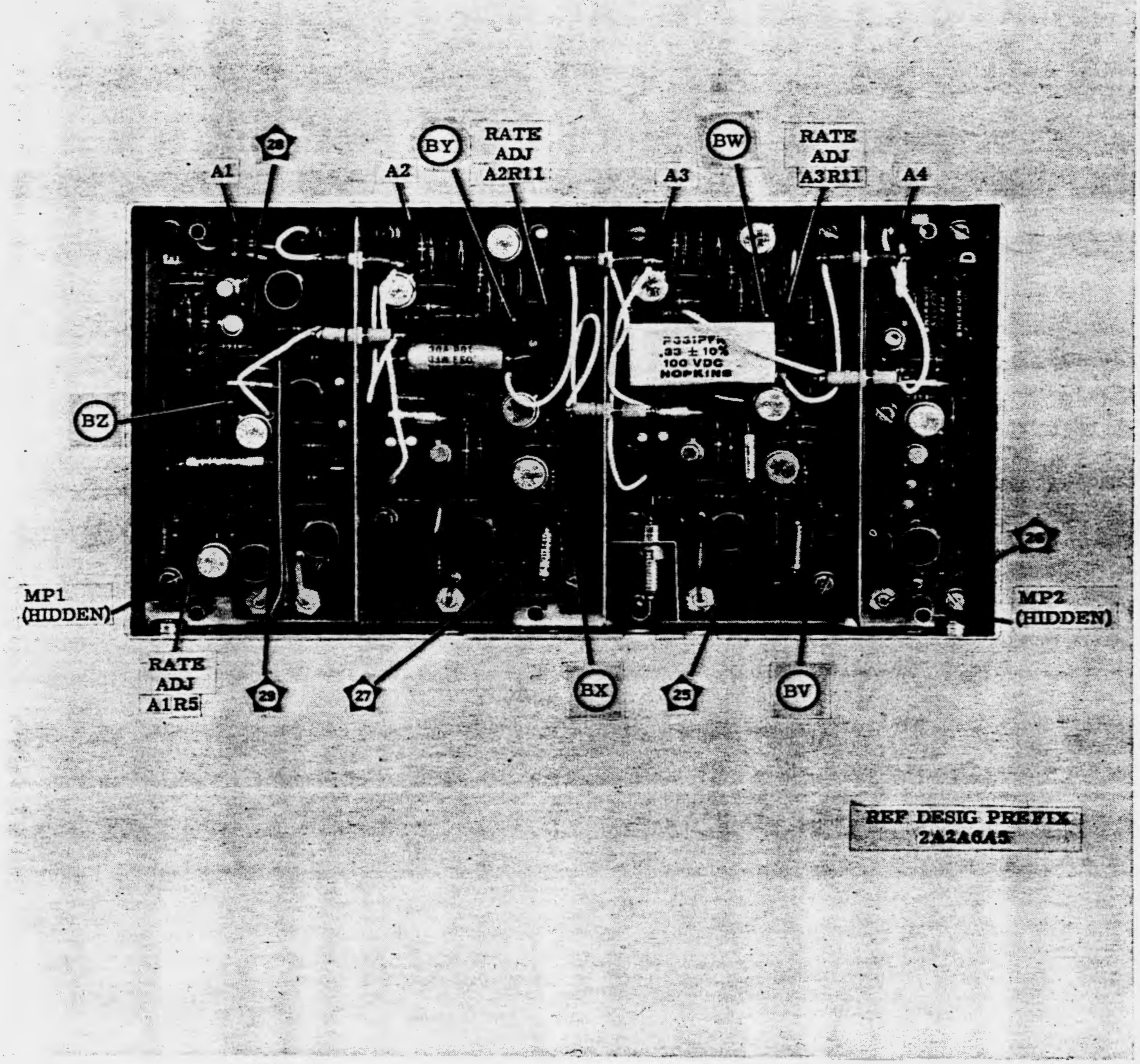


Figure 5-104. Spectrum Generator Electronic Subassembly, Component Location

ION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
R1	6F	R10	7F	R19	8D	TP1	4D
R2	4F	R11	8E	R20	7D	TP2	5D
R3	4E	R12	9F	R21	9C	TP3	7E
R4	5F	R13	7E	R22	5C	TP4	6E
R5	5E	R14	8F	R23	7C	TP5	9F
R6	4F	R15	9E	R24	6C	TP6	8E
R7	6E	R16	7D	R25	5C		
R8	6E	R17	9F	T1	9D		
R9	7E	R18	10E	T2	4C		

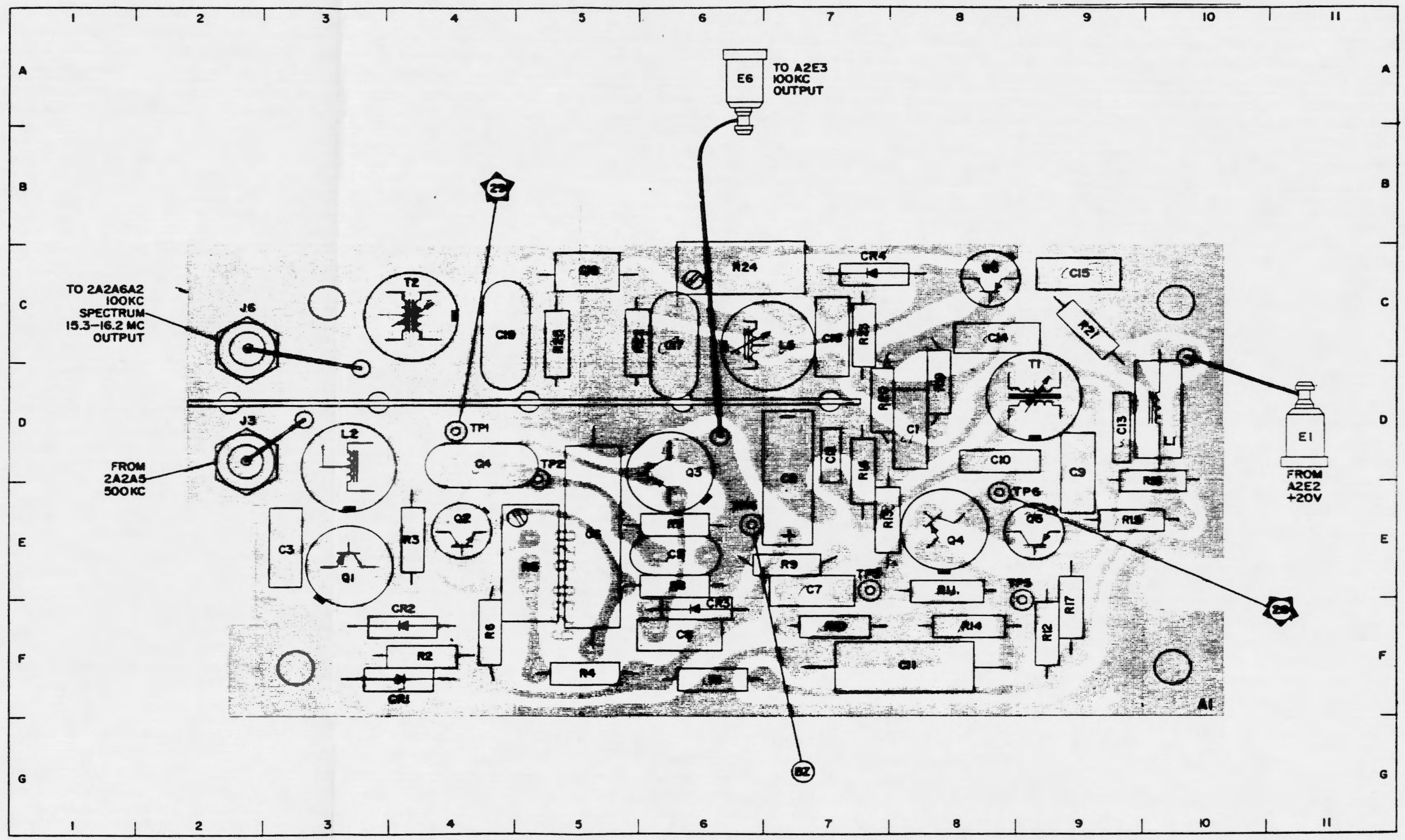


Figure 5-105. 100 KC Spectrum Generator (Foil Side Up), Component and Test Point Location

NOTE:
REF. DESIG. PREFIX 2A2A6A5.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC	REF DESIG
C1	8D	C10	8D	C19	4C	L1	10D	R1	6F	R10	7F	R19
C2	7E	C11	8F	CR1	4F	L2	3D	R2	4F	R11	8E	R20
C3	3E	C12	7D	CR2	4F	L5	7C	R3	4E	R12	9F	R21
C4	4D	C13	9D	CR3	6F	Q1	3E	R4	5F	R13	7E	R22
C5	6E	C14	8C	CR4	7C	Q2	4E	R5	5E	R14	8F	R23
C6	5E	C15	9C	E1	11D	Q3	6D	R6	4F	R15	9E	R24
C7	7E	C16	7C	E6	6A	Q4	8E	R7	6E	R16	7D	R25
C8	6F	C17	6C	J3	2D	Q5	9E	R8	6E	R17	9F	T1
C9	9D	C18	5C	J6	2C	Q6	8C	R9	7E	R18	10E	T2

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
C1	6E	R2	2F
C2	5D	R3	2E
C3	2D	R4	3D
C4	2C	R5	3D
C5	2E	R6	1D
C6	2F	R7	2F
C7	2F	R8	2E
C8	4G	R9	3D
C9	4D	R11	3F
C10	5E	R12	3F
C11	6G	R13	4G
C12	8F	R14	5F
C13	6C	R15	5F
C14	7F	R16	5E
C15	7F	R18	4F
C16	7D	R19	7G
CR1	4D	R20	6F
CR2	2D	R21	8G
CR3	2D	R22	7F
CR4	4E	R23	6E
E1	4H	R24	5C
E2	6B	R25	8E
E3	3B	R26	7E
E4	5H	R27	7D
J5	9D	R28	7D
L1	6D	R29	8D
Q1	2D	T1	7E
Q2	1F	TP1	3F
Q3	2G	TP2	2G
Q4	5F	TP3	5F
Q5	6F	TP4	7G
Q6	6D	TP5	7F
R1	6E	TP6	8F

NOTE:
REF. DESIG. PREFIX 2A2A6A5.

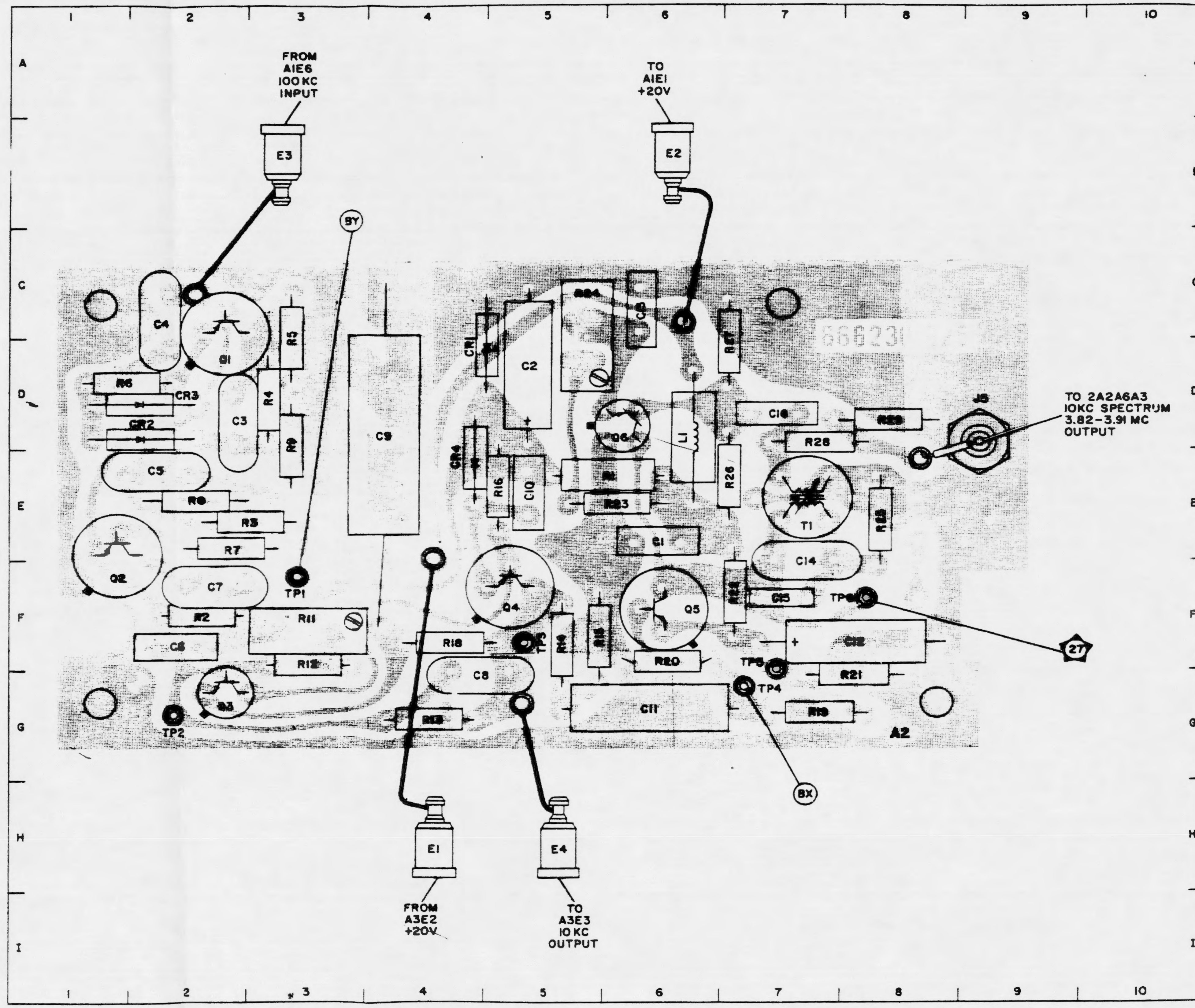


Figure 5-106. 10 KC Spectrum Generator (Foil Side Up), Component and Test Point Location

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	6E	E3	2B	R14	5F
C2	5C	E4	2B	R15	5F
C3	2D	J4	9D	R16	5D
C4	2C	L1	6D	R17	3F
C5	2D	Q1	2C	R18	4F
C6	2F	Q2	1E	R19	7F
C7	2E	Q3	2F	R20	6F
C8	4F	Q4	5E	R21	8F
C9	4D	Q5	6F	R22	7E
C10	5D	Q6	6D	R23	6E
C11	6F	R1	6D	R24	5C
C12	8F	R2	2F	R25	8E
C13	6C	R3	3E	R26	7D
C14	7E	R4	3D	R27	7C
C15	8C	R5	3C	T1	7D
C16	7D	R6	1C	TP1	3E
CR1	4C	R7	2E	TP2	2F
CR2	2D	R8	2D	TP3	5F
CR3	2D	R9	3D	TP4	7F
CR4	4F	R10	3C	TP5	7F
CR5	4D	R11	3F	TP6	6E
E1	3H	R12	3F		
E2	6B	R13	4G		

NOTE:
REF. DESIG. PREFIX 2A2A6A5.

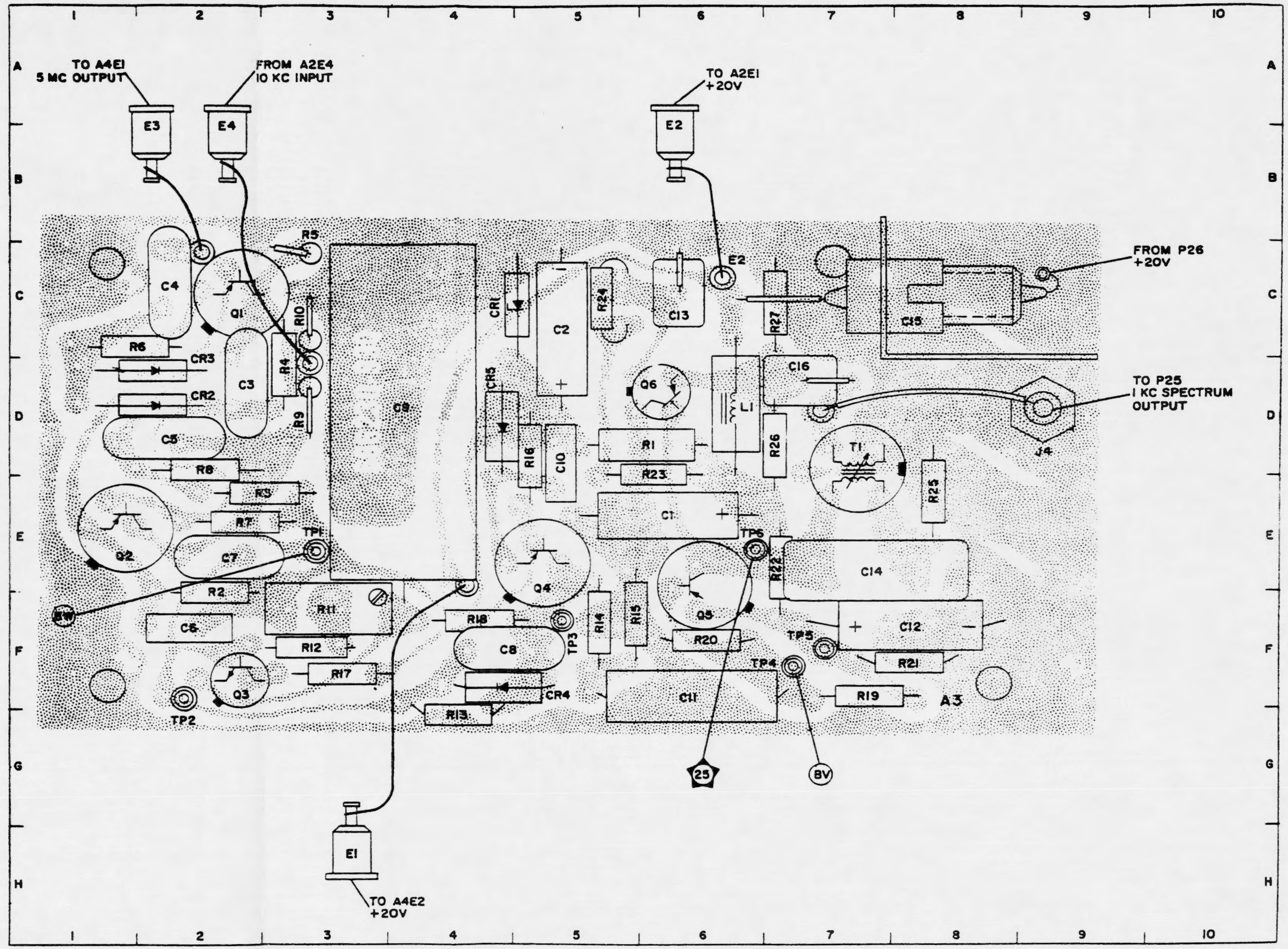
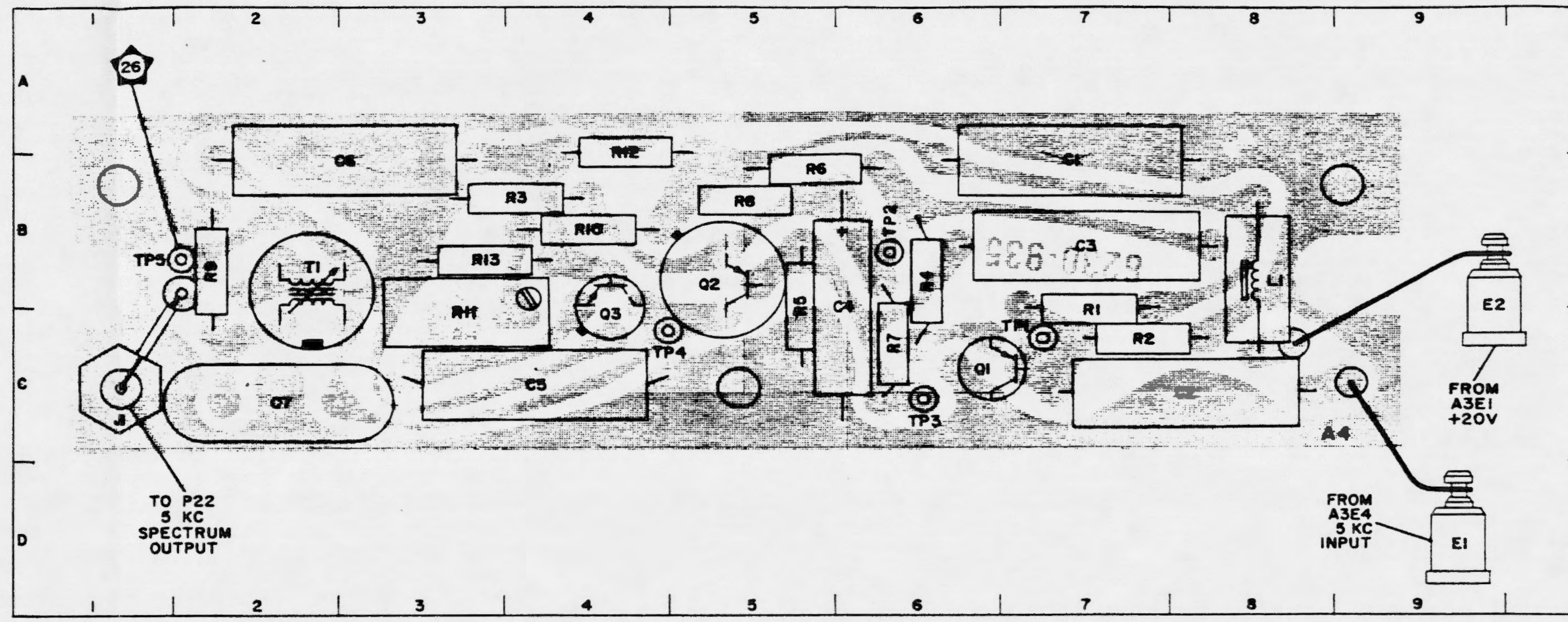


Figure 5-107. 1 KC Spectrum Generator (Foil Side Up), Component and Test Point Location



PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	7B	Q1	6C	R9	2B
C2	8C	Q2	5B	R10	4B
C3	7B	Q3	4C	R11	3C
C4	6B	R1	7C	R12	4A
C5	4C	R2	7C	R13	3B
C6	3B	R3	4B	T1	2B
C7	2C	R4	6B	TP1	7C
E1	9D	R5	5C	TP2	6B
E2	9C	R6	5B	TP3	6C
J1	1C	R7	6C	TP4	4C
L1	8B	R8	5B	TP5	2B

NOTE:
REF. DESIG. PREFIX 2A2A6A5.

Figure 5-108. 5 KC Spectrum Generator (Foil Side Up), Component and Test Point Location

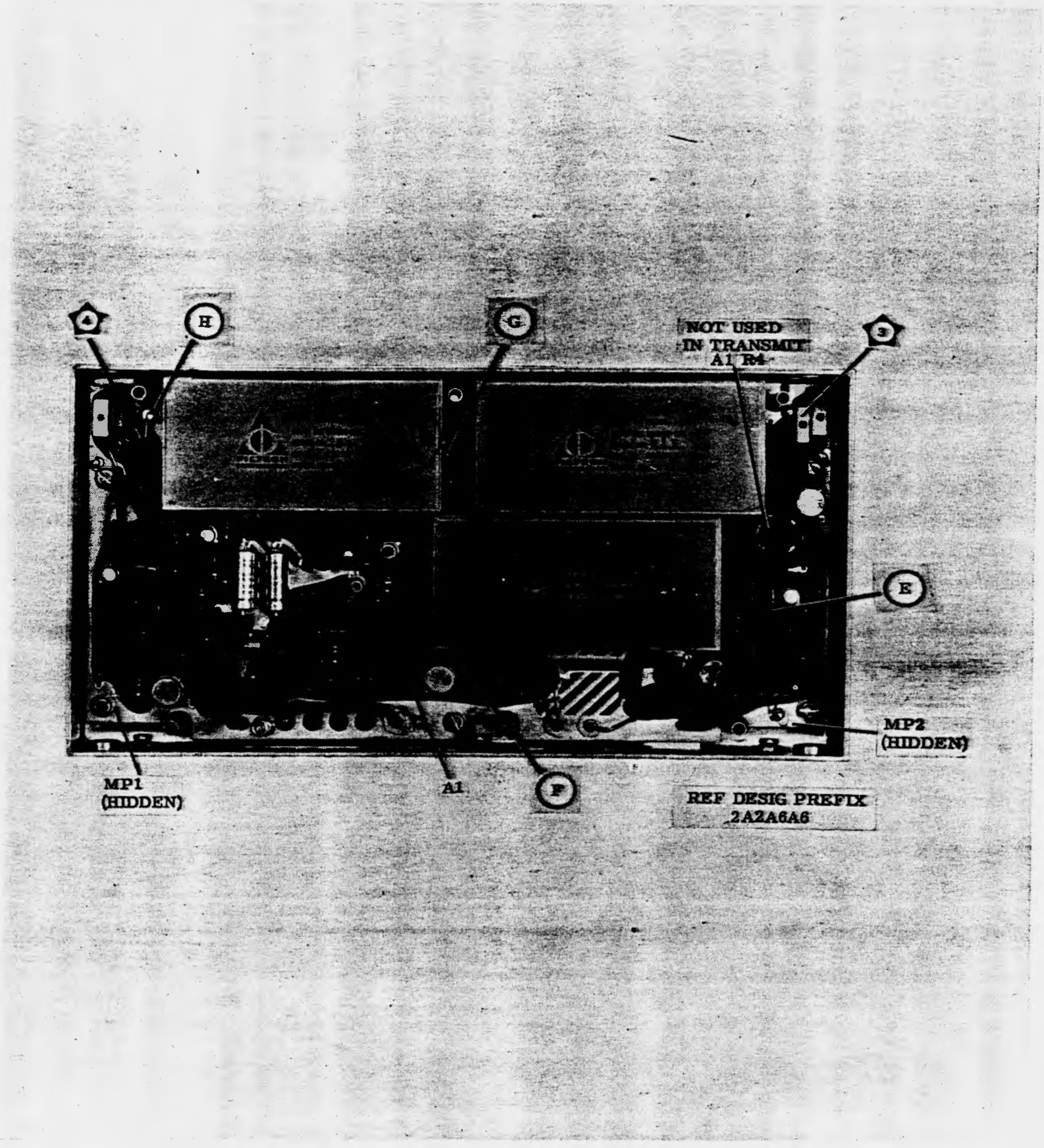


Figure 5-109. RF Translator Electronic Subassembly, Component Location

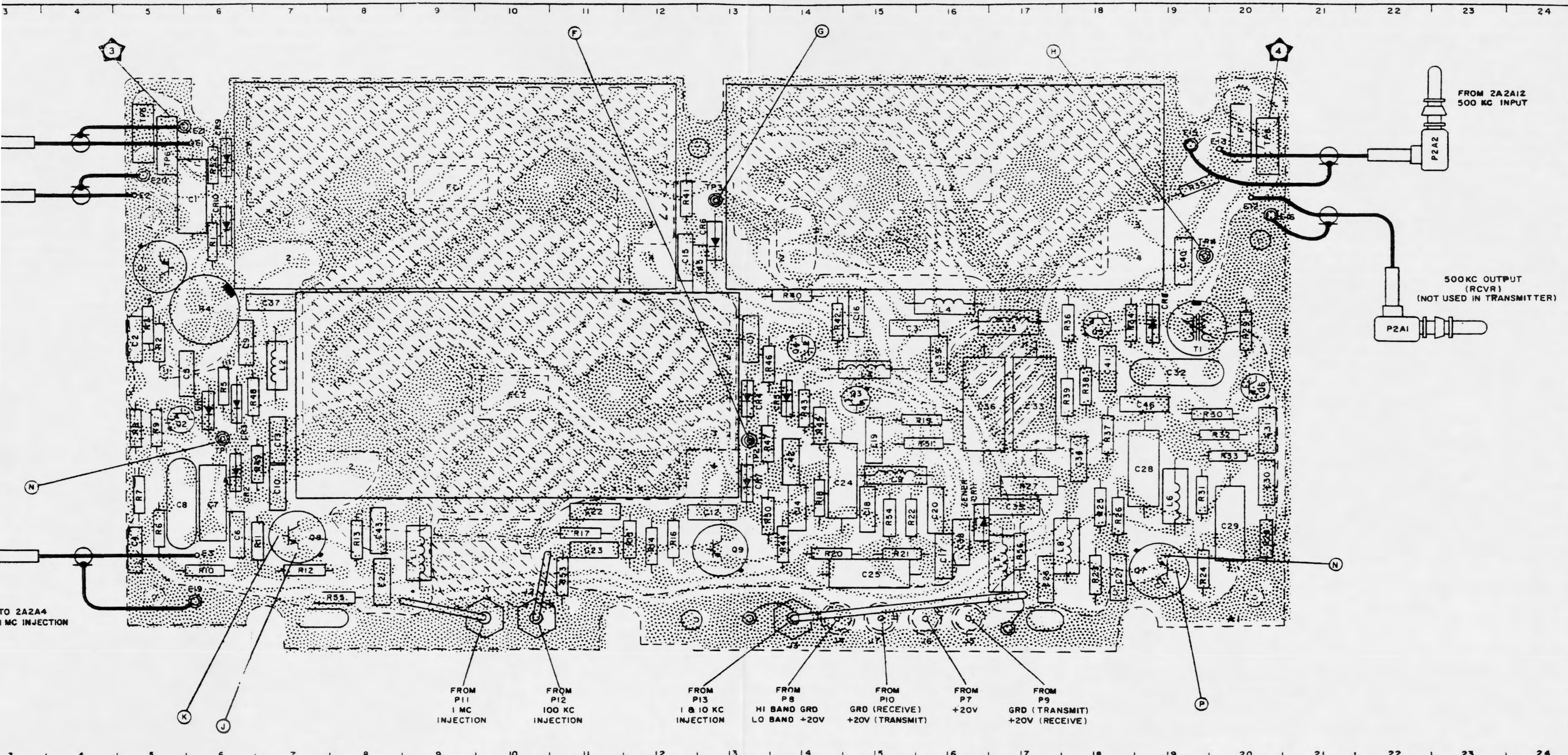
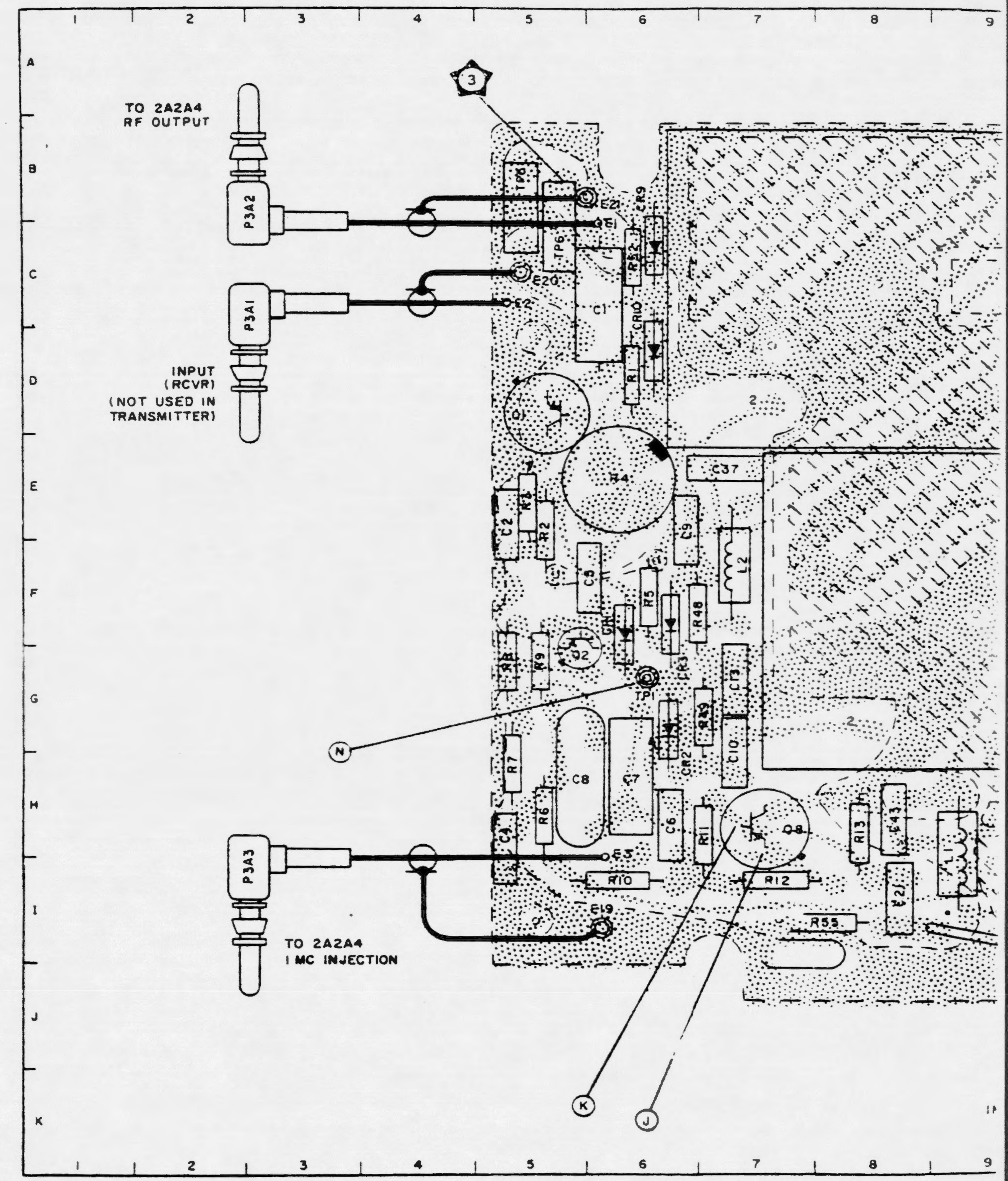


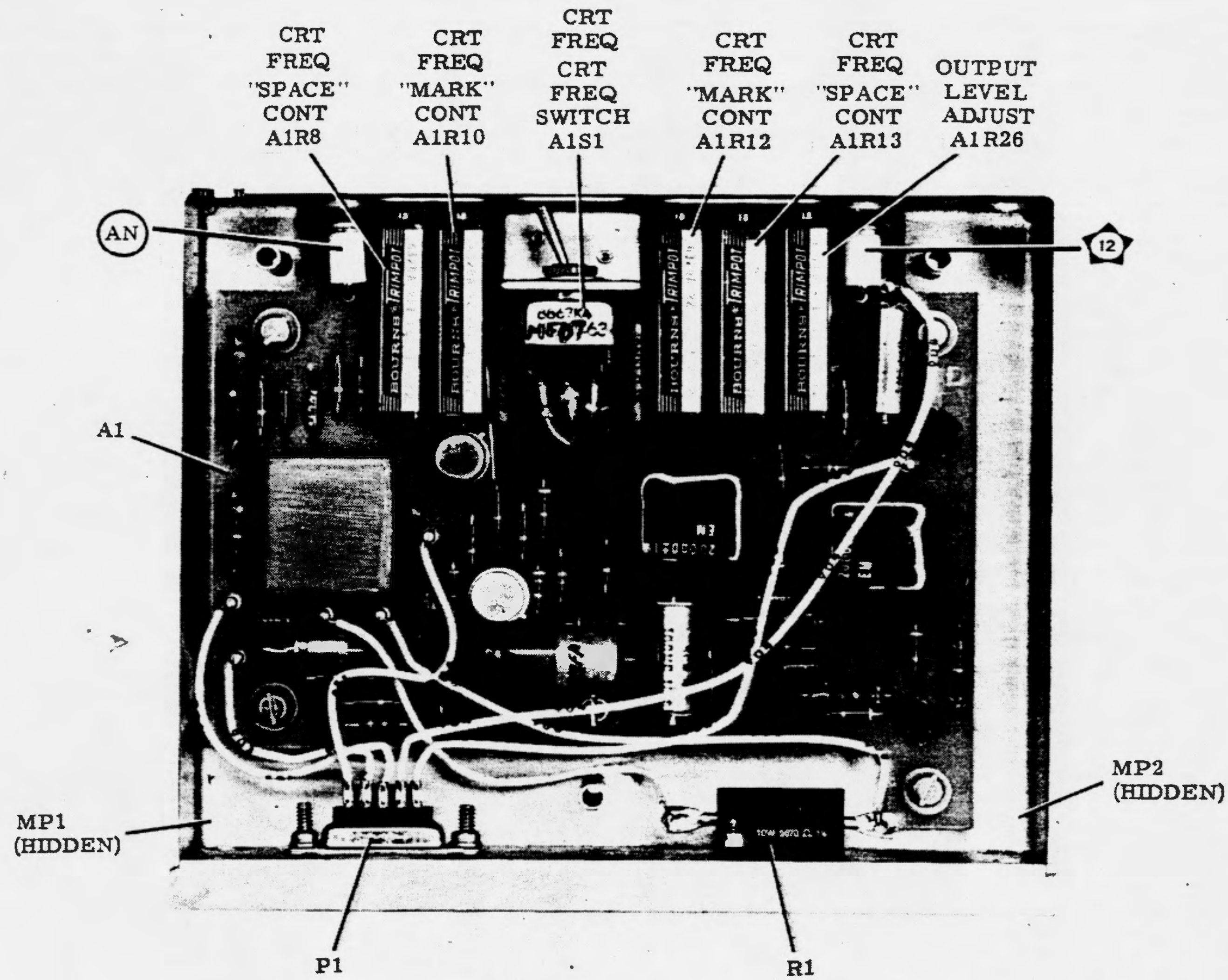
Figure 5-110. RF Translator (Component Side Down), Component Location

NOTE:
REF. DESIG. PREFIX 2A2A6A6.

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC	REF DESIG	LOC
C1	6C	CR11	16H	R13	8H
C2	5E	E2	5C	R14	12H
C3	15E	E3	6H	R15	12H
C4	5H	E12	20C	R16	12H
C5	6F	E13	20C	R17	11H
C6	6H	E15	19C	R18	14H
C7	6H	E16	20D	R19	16G
C8	5I	E19	6I	R20	14H
C9	6E	E20	5C	R21	15H
C10	7G	E21	6B	R22	15H
C11	13E	FL1	9C	R23	18I
C12	13H	FL2	10F	R24	19I
C13	7G	FL3	16C	R25	18H
C14	14H	J1	10I	R26	18H
C15	12D	J2	10I	R27	17G
C16	15E	J3	15I	R28	20H
C17	16I	J4	15I	R29	20E
C18	15H	J5	16I	R30	20F
C19	15G	J6	16I	R31	19H
C20	16H	J7	15I	R32	20G
C21	8I	L1	9H	R33	20G
C22	11H	L2	7F	R34	18E
C23	11H	L3	15F	R35	19C
C24	14G	L4	16E	R36	18E
C25	15I	L5	17E	R37	18G
C26	17I	L6	19H	R38	18F
C27	18I	L7	17I	R39	18F
C28	19G	L8	18H	R40	14E
C29	20H	L9	15G	R41	12C
C30	20G	P2A1	22E	R42	14E
C31	20G	P2A2	22C	R43	14F
C32	19F	P3A1	3C	R44	14H
C33	17F	P3A2	3B	R45	14G
C34	18G	P3A3	3H	R46	13F
C35	17H	Q1	5D	R47	13G
C36	16F	Q2	5G	R48	6F
C37	7E	Q3	15F	R49	7G
C38	16H	Q4	14E	R50	13H
C39	16F	Q5	18E	R51	16G
C40	19D	Q6	20F	R52	6C
C41	18F	Q7	19I	R53	11I
C42	14G	Q8	7H	R54	15H
C43	8H	Q9	13H	R55	8I
C45	13D	R1	6D	R56	17H
C46	19F	R2	5E	T1	19E
CR1	6F	R3	5E	TP1	6G
CR2	6G	R4	6E	TP2	13G
CR3	6F	R5	6F	TP3	13C
CR4	13F	R6	5H	TP4	19D
CR5	14F	R7	5H	TP5	5B
CR6	13D	R8	5G	TP6	5C
CR7	13G	R9	5G	TP7	20B
CR8	19E	R10	6I	TP9	20C
CR9	6C	R11	7H		
CR10	6D	R12	7I		





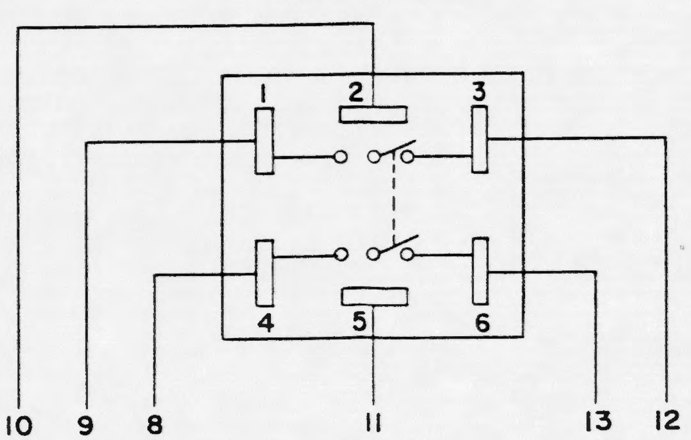
REF DESIG PREFIX
2A2A9

Figure 5-111. FSK Tone Generator Electronic Assembly, Component Location

NOTE:
REF. DESIG. PREFIX 2A2A9.

REF DESIG	LOC	REF DESIG	LOC
C1	11E	R2	9G
C2	8G	R3	9H
C3	11D	R4	9H
C4	7G	R5	10D
C5	5E	R6	8F
C6	4G	R7	9C
C7	3G	R8	9C
C8	2G	R9	7C
C9	5G	R10	8C
C10	3C	R11	6C
C11	3F	R12	5C
CR1	10F	R13	4C
CR2	9G	R14	7F
CR3	10D	R15	7E
CR4	10D	R16	7E
CR5	6F	R17	6F
CR6	4F	R18	7E
CR7	4G	R19	8F
CR8	4F	R20	4G
E1	11F	R21	3H
E2	11G	R22	5G
E3	9F	R23	4E
E4	9F	R24	2G
E5	8E	R25	3D
E6	3B	R26	4C
E7	3D	R27	3E
Q1	8H	R28	9C
Q2	8D	R29	7F
Q3	6E	S1	6C
Q4	7F	T1	9E
Q5	4H	TP1	9B
Q6	2H	TP2	3B
Q7	2D		

CONTACT DETAIL
SWITCH SI



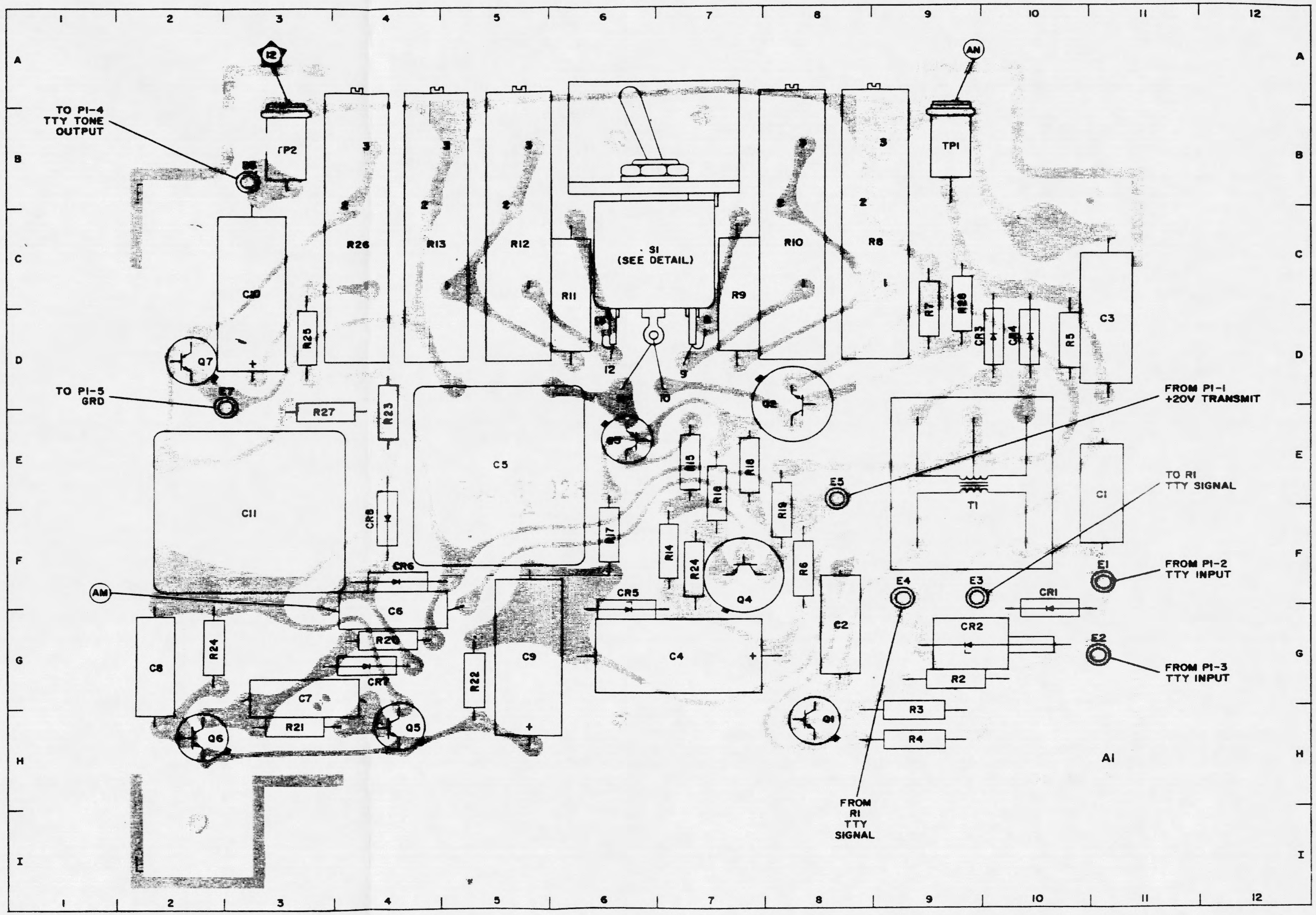


Figure 5-112. FSK Tone Generator
(Foil Side Up), Component Location

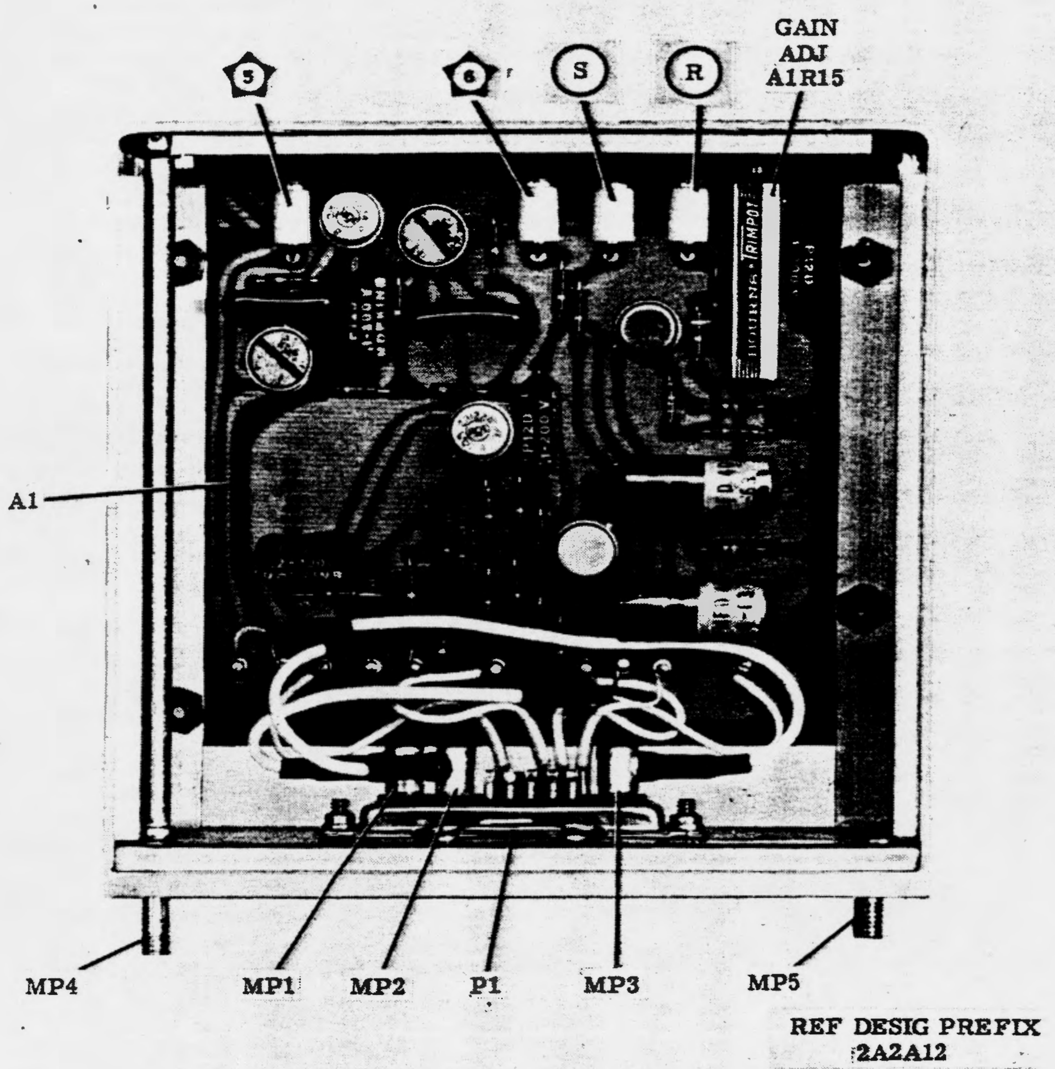


Figure 5-113. Transmitter IF. Amplifier Electronic Assembly, Component Location

PARTS LOCATION INDEX

REF DESIG	LOC	REF DESIG	LOC
C1	5D	R4	5E
C2	7F	R5	5F
C3	3E	R6	5B
C4	6F	R7	6D
C5	6C	R8	6C
C6	2B	R9	7D
C7	7C	R10	5E
C8	8C	R11	5G
C10	3G	R12	5F
CR1	3D	R13	3C
E1	8G	R14	3D
E2	8G	R15	3C
E3	7G	R16	6C
E4	3G	R17	3D
E5	4G	R18	8C
E6	4G	R19	3C
E7	3G	R21	7F
E8	5G	R22	6G
E9	7G	R23	5C
E10	6G	R24	3F
Q1	4F	R25	4C
Q2	6D	T1	6B
Q3	7B	T2	8D
Q4	4C	TP1	5B
R1	5G	TP2	8B
R2	5F	TP3	4B
R3	6F	TP4	3B

NOTE:
REF. DESIG. PREFIX 2A2A12.

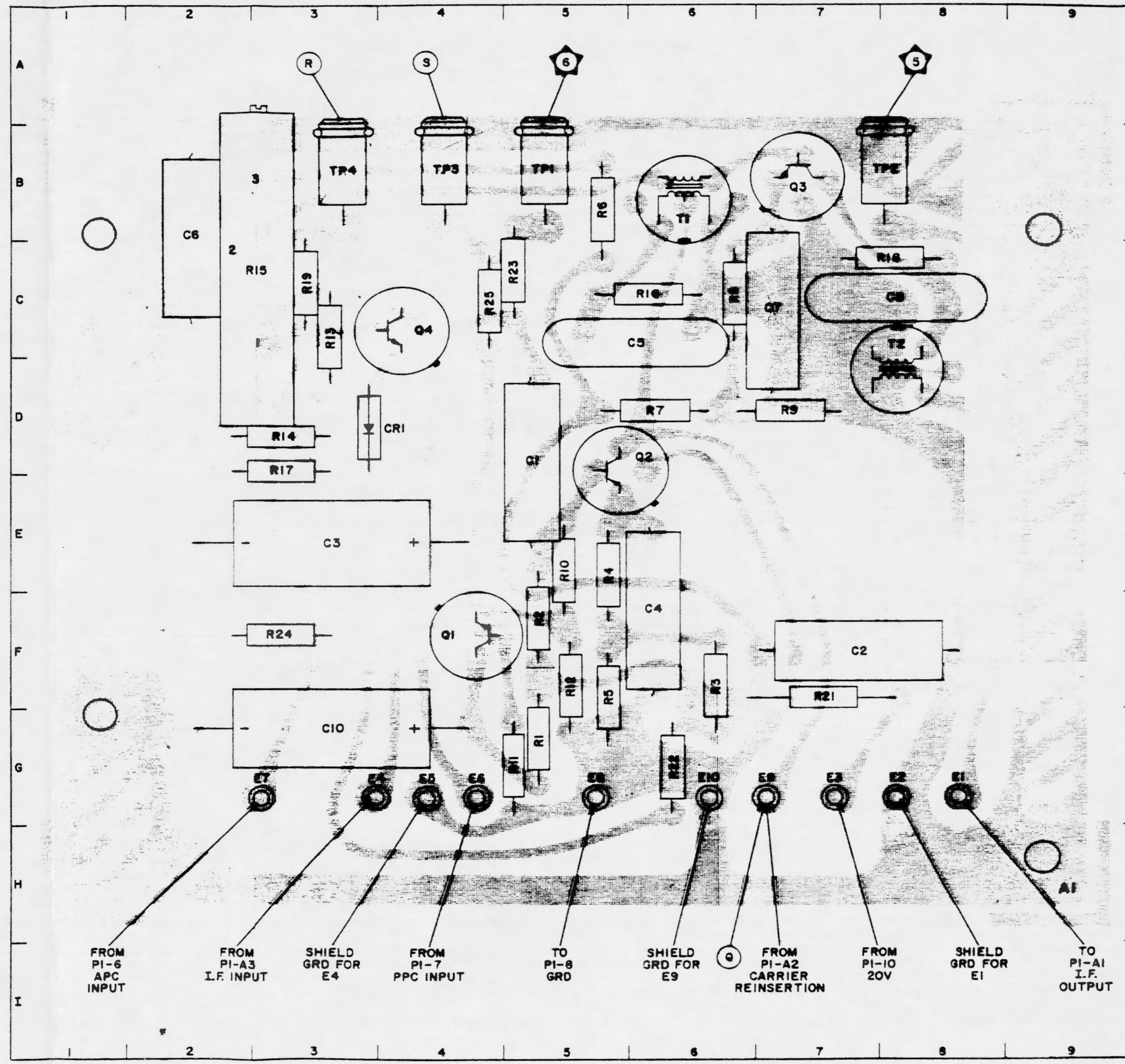


Figure 5-114. Transmitter IF. Amplifier (Foil Side Up), Component Location