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Rapid Developments in Communications Open New Vistas

To Our Readers:

At the stockholders meeting on April 14, 1965 President McFall made the first public announcement of Western Union's intentions to become a national information utility—a nationwide, interconnected facility for real-time communications and data processing. He followed this shortly with an announcement of the formation of the Information Systems and Services Department dedicated to providing information systems and related services to industry, the government and to Western Union itself.

The rapid developments in communications and data processing tech-

R. W. HODGERS, JR.

nology have opened new opportunities and challenges. Computers, satellites, lasers and many other scientific advances yet to be discovered shall make this an exciting and fast moving field—a field with which I am most happy to be associated.

It is particularly appropriate that this 18th Anniversary issue of TECHNICAL REVIEW *highlight the developments related to information systems and services technology. I would personally like to commend the authors of this anniversary issue on their contributions.*

Robert W. Hodgers Jr

VICE PRESIDENT
Information, Systems and Services

J. J. McManus & J. D. Dorgan, Engineers—Information Systems & Services Dept.

Integrated Circuits

Western Union is participating in the "quiet revolution" now underway in the electronics industry. This modern technological development concerns the field of microelectronics, the successor to the transistor. As pioneer in record communication Western Union has become more involved in high-speed data switching systems. Therefore it became necessary that switching systems engineers study and compare the various high-speed logic circuits such as—the discrete component, hybrid and monolithic integrated circuits to ascertain which met the new high-speed requirements of our systems. As a result of a carefully planned testing program, Western Union concluded that our future high-speed requirements would best be satisfied by using the monolithic integrated circuit. New systems currently being developed will incorporate these devices.

History

The Government Agencies and Aerospace industry have accelerated the need for miniature and microminiature electronics in the decades since the Second World War. The military, concerned with small, lightweight, and reliable equipment, increased the pressure for miniature and subminiature tubes. The development of solid state devices, such as the transistor in the early 1950's, furthered the improvement of electronic packaging.

The strong influence of the aerospace industry and its use of the more complex electronic devices in rocket control and guidance, increased the requirements for greater reliability, reduced size, and lighter weight units.

Until recently, the term "microelectronics," meant any circuit technology that permits electronic functions to be performed in a very small module or package. Micro-electronic circuitry, in equipment, was generally restricted to modules constructed from miniature, but discrete components. One example of a miniaturized but discrete component circuit is the standard Western Union printed circuit card shown in Figure 1. This standard card contains two flip-flop circuits. Logic circuit cards of this type are in current use in our switching systems. This illustration shows that circuits are made up of discrete elements such as transistors, diodes, resistors, and capacitors mounted on a printed circuit board.

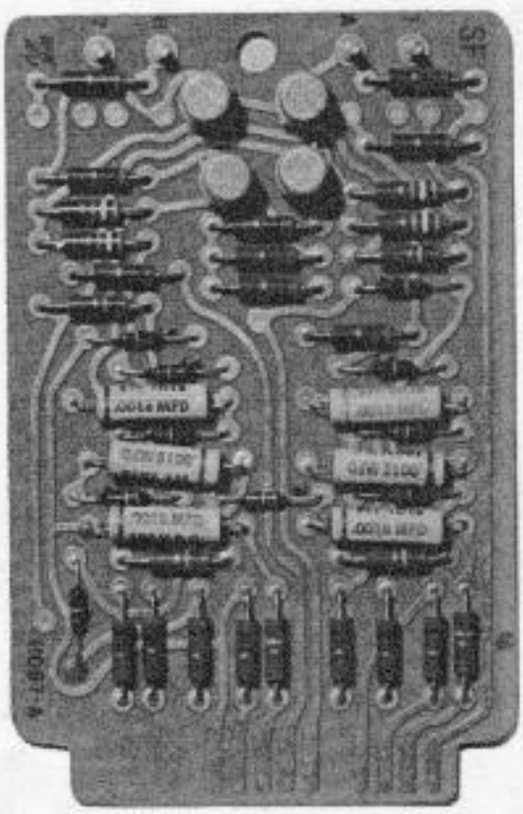


Figure 1. Standard W.U. Circuit Card containing Two Flip-Flop Circuits

The semiconductor techniques used to develop the transistor were expanded to provide further miniaturization. This led to the development of a complete circuit consisting of several elements, on or in a single block of material, called the "integrated" circuit. Figure 2(a) shows an industrial integrated circuit package which contains a J-K Binary element. This package is fabricated within a monolithic silicon substrate by means of the planar technique. The circuits contained within two of this type package perform many functions similar to those of the printed circuit card shown in Figure 1.

Several types of integrated circuit packages are shown in Figure 2. Figure 2 (a) shows a TO-5 package and Figure 2 (b) a flat package form of integrated circuit. Figure 2 (c) shows a hybrid form of microcircuit containing a combination of thin film substrate and conventional transistors.

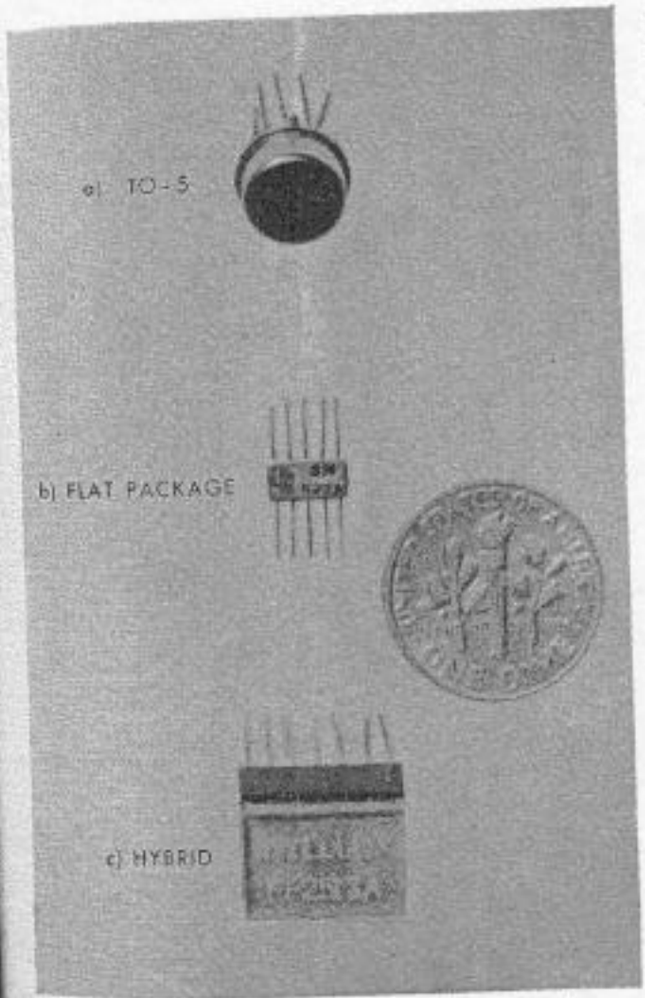


Figure 2. Three Types of Integrated Circuits

Microelectronic Techniques

The integrated circuit in microsystems may be defined as a number of circuit elements associated on or within a continuous body which perform circuit functions. These circuits have many forms; three of these are described as follows:

Thin-Film Techniques

This technique develops an integrated-circuit design by means of thin-film deposition. Circuits are made by depositing passive elements on inert or passive substrates. Elements such as resistors and capacitors, with the associated wiring, are deposited by means of either spray, vapor, sputtering or plating processes. These depositions are made on inert or passive substrates usually made of glass or ceramic. These provide a base for the circuitry. This method can be viewed merely as another way of miniaturizing conventional discrete component circuits and their interconnections. Close control over tolerances and the thickness of the film can be maintained. Resistance of a thin-film resistor depends only on the deposited shape. Metal film can be shaped to particular resistor values. Capacitors are formed by a vacuum-deposited dielectric material, sandwiched between two conducting layers. Noble metals are usually used because of their high conductivity and inertness to oxidation. The thin-film techniques have a major drawback, the difficulty in depositing active devices such as transistors or diodes.

Hybrid Integrated Approach

The inability of thin-film methods to successfully deposit active devices led to the development of the "hybrid" circuit. The hybrid circuit is usually made up of individual active components in combination with thin-film passive components, wired to each other by means of bonded leads. This technique, called the "hybrid integrated" approach, combines the advantage of the uniformly closely controlled tolerance of the deposited passive (resistor-capacitor) elements and the separate semiconductor active elements. The thin-film and hybrid processes do not re-

sult in the fully-integrated, solid-state circuit; wherein the single semiconductor block contains all the circuit elements such as transistors, diodes, resistors, and capacitors.

Fully Integrated Process

To produce a fully integrated circuit, in contrast to the thin-film technique, both passive and active elements are formed on a semiconductor substrate, usually a silicon wafer. The forming is done by a diffusion or epitaxial growth process, followed by vapor deposition. This process permits a large number of circuits to be simultaneously produced on one piece of material. The solid-state integrated circuit is the most dramatic example of space saving in the field of microcircuitry. Besides reducing the large number of wiring interconnections and the size of the wafer, other important factors such as element uniformity and low production costs are possible with this process.

To fully understand the integrated circuit it is necessary to describe the manufacturing techniques and packaging of these solid-state devices.

Manufacture of I-Cs

Since the fabrication of integrated circuits is an extension of the fabrication of the transistor, a review of the construction of this device may be of interest.

Epitaxial Planar Transistors

Let us consider the steps involved in the making of an NPN, junction type, epitaxial planar transistor. Figure 3 (a) is an elementary diagram of an NPN transistor, which consists of a P layer, the base, sandwiched between two N layers which represent the collector and emitter elements. This type of transistor is usually represented by the symbol shown in Figure 3 (b).

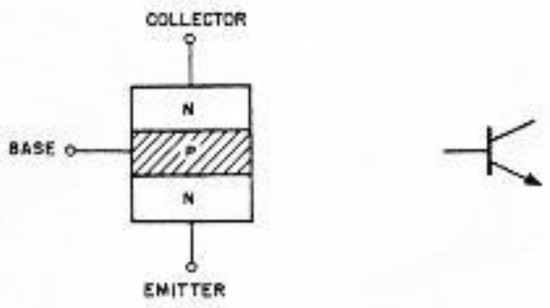


Figure 3(a) NPN Transistor and its symbol 3(b)

The fabrication process is shown in Figure 3 (c). It starts with: (1) a slice of purified silicon cut from a crystal; (2) an epitaxial N-type layer is grown on a P-type silicon substrate, becoming a single crystal extension of the substrate wafer; (3) a thin layer of silicon oxide is then formed on its surface; (4) part of the oxidized layer is etched using photo-proces-

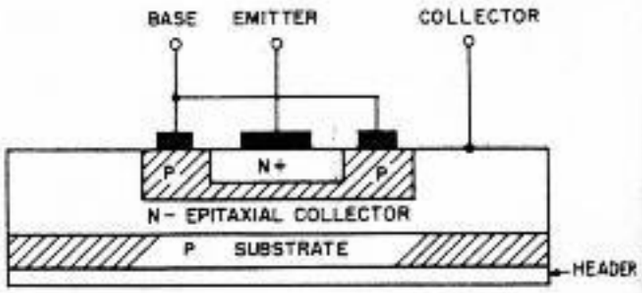


Figure 3(c) Build up of Epitaxial Planar Transistors

sing methods; (5) a P layer is diffused in the epitaxial layer and the surface reoxidized; (6) the reoxidized layer is again selectively etched by a masking and etching process; (7) the N layer for the emitter is diffused and the surface reoxidized; (8) oxidized areas are again selectively etched; (9) metal contacts are deposited and alloyed to the substrate at the etched area. This process results in the NPN planar transistor shown with the leads attached to the emitter, base and collector layers.

The substrate provides the necessary bulk for ease of handling. This type of transistor has low saturation resistance and lower collector storage time than other non-epitaxial types.

Integrated Transistors

The process for making discrete transistors described above can be extended by making many NPN junctions on a single silicon wafer. A typical integrated circuit is fabricated by depositing a layer of silicon oxide on the prepared silicon wafer. Holes are etched in the oxide using a photographic mask, called a photoresist. The transistors, diodes and resistors are built up on the holes by the sequence of

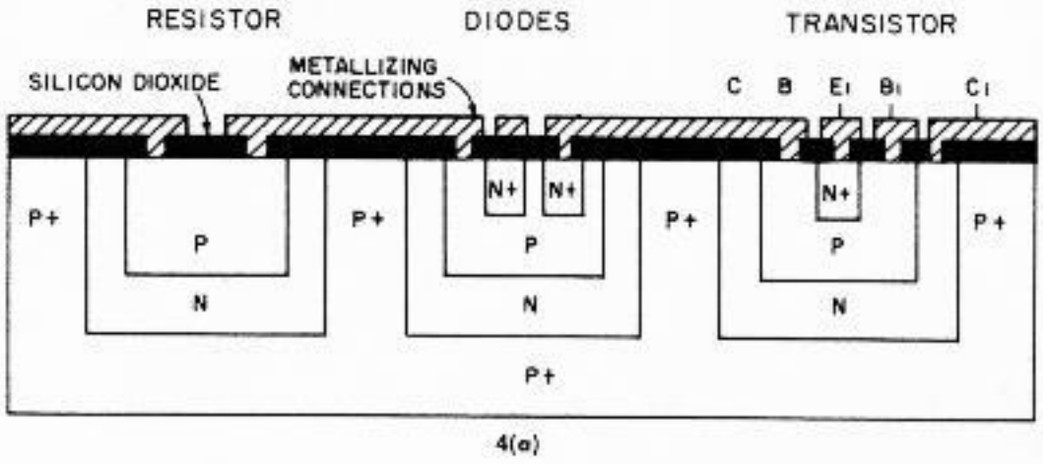
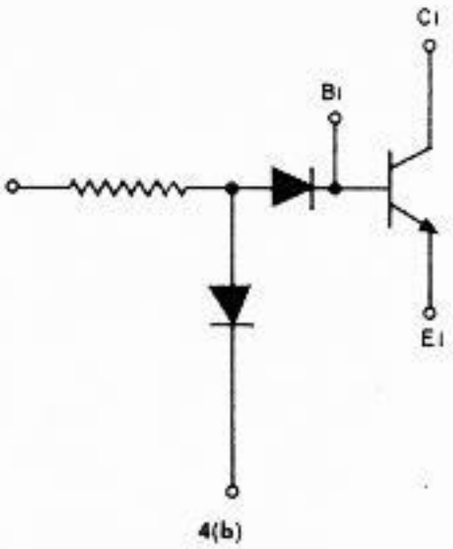


Figure 4. Build Up of an Integrated Transistor 4(a) and its Schematic Symbol is shown in 4(b)



diffusion or epitaxial growth operations described in the previous paragraph on discrete transistors. Figure 4 (a) shows three NPN layers which have been built up by integrated circuit diffusion and etching techniques on a silicon wafer. The schematic circuit for this type build up of junctions is shown in Figure 4 (b).

Although this is not a practical circuit it shows the possibilities which integrated circuit techniques have for uniformly producing simultaneously many transistors, diodes and resistors and providing for circuit interconnections at the same instant of manufacture. It is possible to produce as many as 4200 resistors and 1100 transistors on one silicon wafer.

Integrated Diodes

Diodes are easily produced in the monolithic circuit processes by simply stopping the diffusion and etching process, in the making of a transistor, and making only PN or NP junctions, as shown in Figure 5. In this figure three diode junctions are diffused on the same

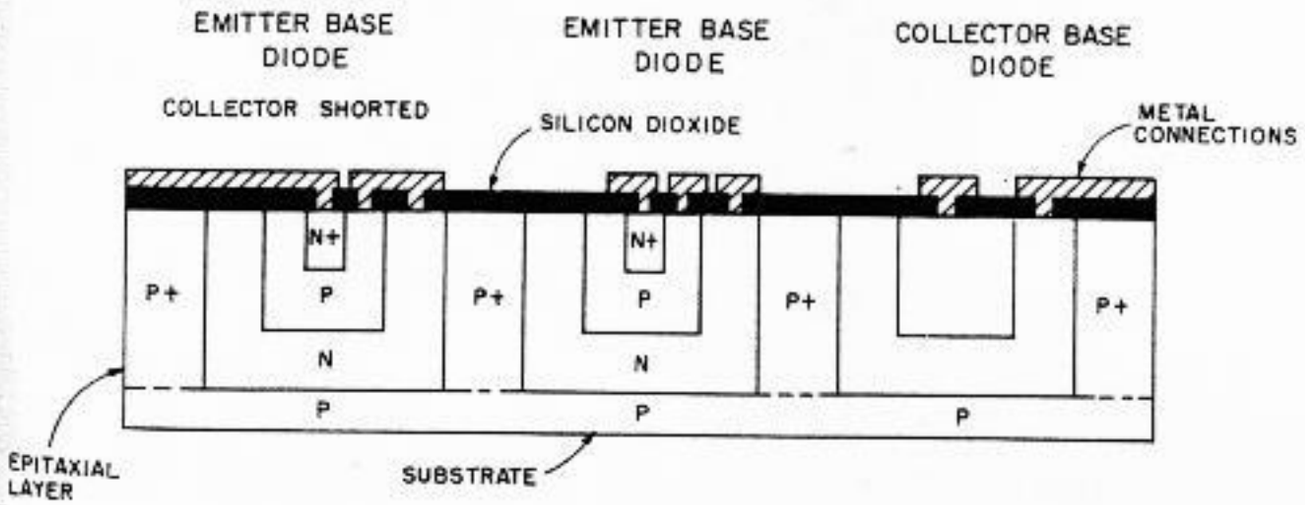
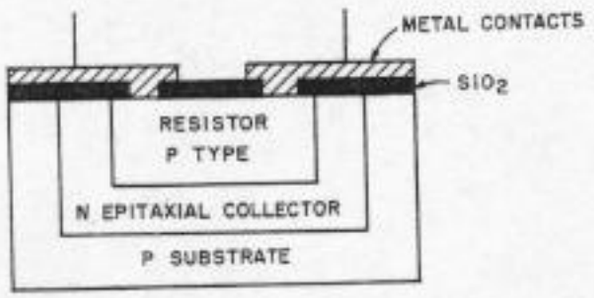


Figure 5. Build-up of Integrated Diode

substrate. Diodes are easily made out of transistors by using the base-emitter or the base-collector junctions as shown. The transistor collector can be shorted or left open to provide various characteristics.

Integrated Resistors

Resistors, in monolithic solid-state circuits, are usually made by the same diffusion processes used in making the emitter, base or collector elements of a transistor. The resistance value is a function of the sheet resistance of the diffused P layer, the length and cross-sectional area. The resistors are made by "snaking" to get maximum use of the limited surface area. If a PN junction formed by diffusion is reversed-biased, current flow can be restricted to the resistive region. Figure 6 (a) shows a PN junction with ohmic contacts and Figure 6 (b) shows a long P region diffused in the N region to give the necessary length.



6a PN Junction with ohmic contacts

6b N Region diffused in a P Region

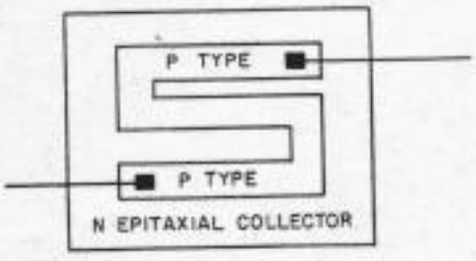


Figure 6. Build-up of Integrated Resistor

Integrated Capacitors

When capacitors are used in an integrated circuit, back-biased PN junctions are used. In this junction, the depletion layer functions as the dielectric, and the capacitance depends on the width of the layer, which, in turn, depends on the back-bias voltage and the junction area. Figure 7 shows a PNPN four-layer device built up by the diffusion process with the necessary connections to form a capacitor.

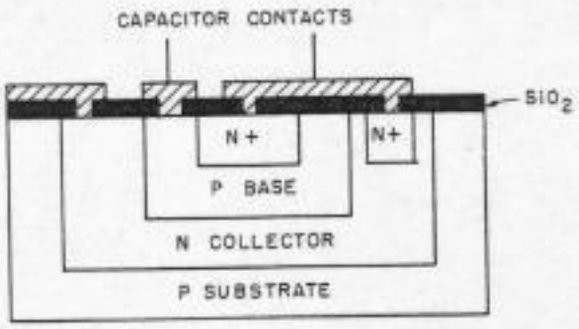
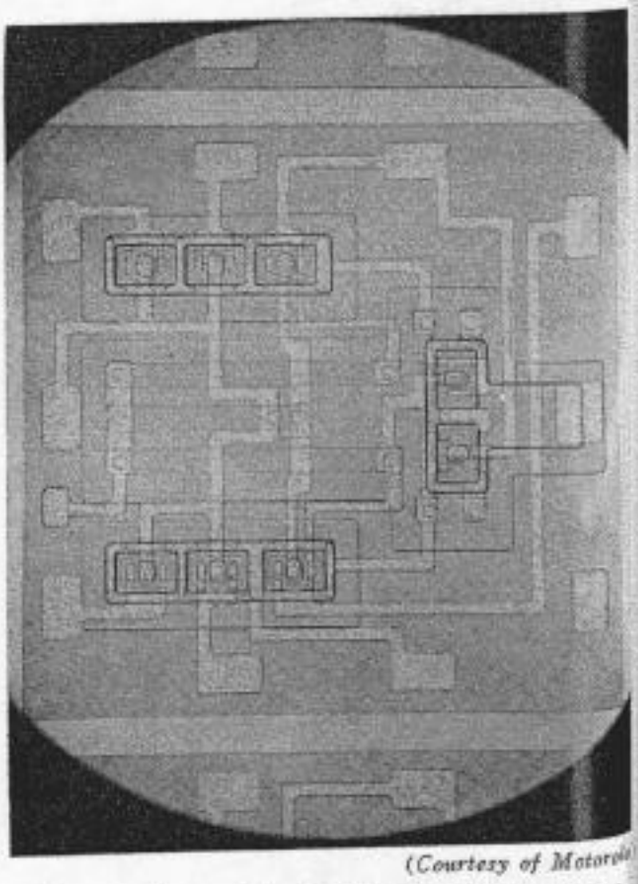


Figure 7. Build-up of PNPN Integrated Capacitor

A microphotograph of a complete integrated circuit flip-flop (current mode) on a single chip, with the diffused resistors and transistors and connecting leads, is shown in Figure 8.



(Courtesy of Motorola)

Figure 8. Integrated circuit Flip-Flop (current mode)

It is evident from the material presented in the previous paragraphs that the diffused layer transistor process is the heart of the integrated-circuit concept. Consequently, the circuit designer who formerly tailored his own circuit, by using discrete components (selected according to his requirements) must now learn the characteristics of the total circuit package offered by the various vendors.

The integrated circuit, although spectacular in development, is not without its own peculiar problems. One problem of the multilayer transistor employed in these circuits, is the "capacitance" formed by isolation diodes which are the result of junctions formed between the transistor elements and the header material.

The manufacturers of integrated circuits — in attempting to design simple circuits with few interconnections has developed a wide range of integrated logic circuits for use in switching systems. The ease with which manufacturers can produce integrated circuits has led to a wide variety of circuits. The principles of some of these circuits and the characteristics will be briefly described here.

Transistor Logic Circuits

Transistor Logic circuits are usually built up from three basic logic function circuits, namely: AND gates, OR gates, and Inverters. Other logical blocks such as the NOR, NAND, and the FLIP-FLOP are obtained by using the three basic blocks. These functional blocks can be combined for different circuit configurations. These circuits are classified according to the elements used for interstage coupling, for coupling between gates and inverters, for amplifiers. Coupling elements used are transistors, diodes, resistors, capacitors, and resistor-capacitor combinations.

Since the terms "fan-out" and "fan-in" are frequently referred to in integrated circuit literature it may be helpful to define these terms. Fan-out is the term used to describe the number of transistors or following circuits simultaneously connected to the output of a logic circuit. Fan-in, on the other hand, is a term applied to the number of solid-state circuits applied simultaneously to the input of a logic configuration.

DCTL Circuit

The DCTL, Direct Coupled Transistor Logic, circuits belong to a class of logic circuits which do not use any of the coupling elements mentioned above. Figure 9 is a schematic of a series DCTL-NAND gate circuit with a following transistor stage which can easily be developed in monolithic integrated circuit form. Positive signals on the inputs A and B will give a potential at C close to ground. The potential will be the sum of the Vce (sat) of Q_1, and Q_2 in series. This DCTL configuration has a disadvantage in that it is necessary that the two series transistors be fully saturated in order to turn off transistor Q_3. The sum of the two Vce (sat) of the series transistors must be less than the Vbe (on) of Q_3. Some of the advantages of DCTL are the low voltages required, low power dissipation and the absence of interstage coupling devices which make its production natural for integrated circuit techniques. However,

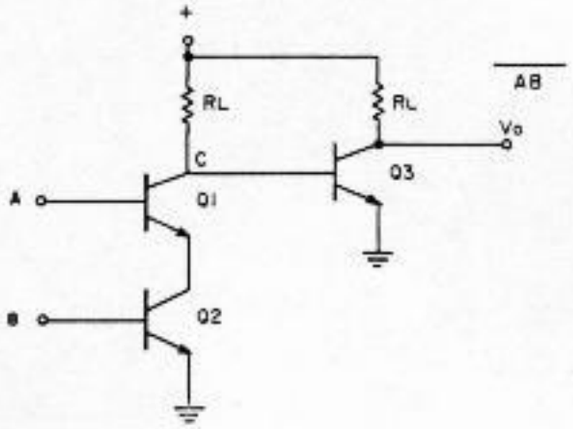


Figure 9. DCTL Circuit

noise potentials developed in high-speed systems can interfere with the operation of DCTL circuits since the operating and signal voltages in these systems are naturally low. DCTL circuits are also susceptible to power supply and stray noises as well. DCTL logic has one of the lowest noise margins, typically 0.1 volt at 125°C and about 0.21 volt at room temperatures

depending on the fan-out and whether the transistor is "on" or "off."

RTL Circuit

The RTL, Resistor-Transistor Logic, circuit is characterized by the use of resistors in combination with transistors. Resistors are usually cheaper and more reliable than semiconductors. RTL, although not often used in fully integrated circuits, has several advantages over other forms of logic. Figure 10 shows a simple 3-input RTL circuit which can function as either a NOR or a NAND circuit, depending on signal definition. The circuit functions as a NOR circuit, i.e. if any one input has a positive applied voltage which causes the base of Q_1 to go positive and turn on Q_1. Q_1, driven into saturation, causes the output voltage to be near ground.

The use of resistors allows for larger signal swings, which in turn permits larger fan-ins and fan-outs. Wide signal swings improves the noise immunity of the circuit. The speed of RTL is limited by the speed of the transistor. RTL is a simple and inexpensive logic circuit, well suited for moderate speeds of operation. Some of the disadvantages of RTL are (1) increase in signal swing requires transistors with higher voltage ratings, and (2) turn-on delay may be appreciable.

DTL Circuit

Figure 11 shows a DTL Diode-Transistor Logic NOR circuit, in which any

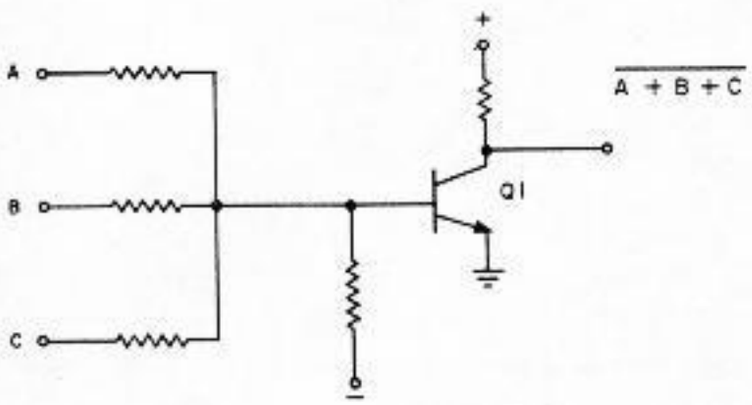


Figure 10. RTL Circuit

ground input causes the base of transistor Q_1 to go negative and causes Q_1 to be cut off, so that Vo is at the supply potential.

The DTL circuit has a disadvantage in the limitation of fan-ins. When Q_1 is saturated, the following fan-out stages, that it drives, are "off." The turn-off voltage seen by the transistors of these stages is the sum of Vce (sat) of Q_1 and the forward drop across the conducting gating diode of each stage. The result of this is that the fan-out transistors demand large turn-off currents which limit the fan-in capability.

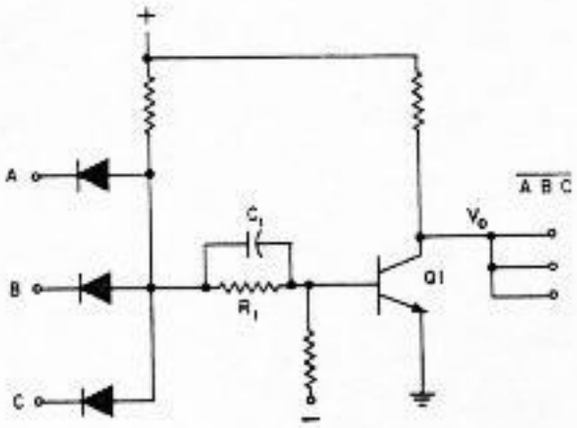


Figure 11. DTL Circuit

LLL Circuit

A modification of DTL, replacing the base limiting resistor, R1, and the speed up capacitor, C1, by a diode is a circuit referred to as Low-Level Logic. Figure 12 shows such a circuit. When simultaneous positive signals are applied to the input diodes, the point A will be positive and since the diode is forward-biased, node B will also be positive. This turns on transistor Q_1. The positive voltage excursion of A will depend on the drop across diode and Vbe drop of Q_1. This voltage drop improves the noise immunity of the circuit and one or two additional diodes are often used to further improve the noise immunity. LLT reduces the number of resistors required and can operate with lower voltages.

CML Circuit

A Current Mode Logic Circuit involves transistors which are biased from constant current sources to keep them far out of saturation. Both inverted and non-inverted outputs are available. Figure 13 shows a CML circuit with two outputs

CML has the following advantages:

a) Non-saturating switching and low impedance drive give high speed operation.

b) Noise on power supplies can be attenuated to prevent changing the switching signals.

TTL Circuit

One form of logic circuitry, well adapted to integrated circuits, is the so called TTL or T^2L circuit. Figure 14 shows a three-input, integrated NOR gate circuit. It will be observed that the gating diodes employed in the LLT circuit of Figure 12 are replaced by transistors, which gives rise to the Transistor-Transistor Logic designation given to this type of circuit.

Operation of TTL is similar to the LLT circuits, but it has the following additional advantages:

a) TTL uses transistors in place of diodes and resistors because transistor fabrication is easily performed in integrated circuit design.

b) The TTL circuit requires only one power supply.

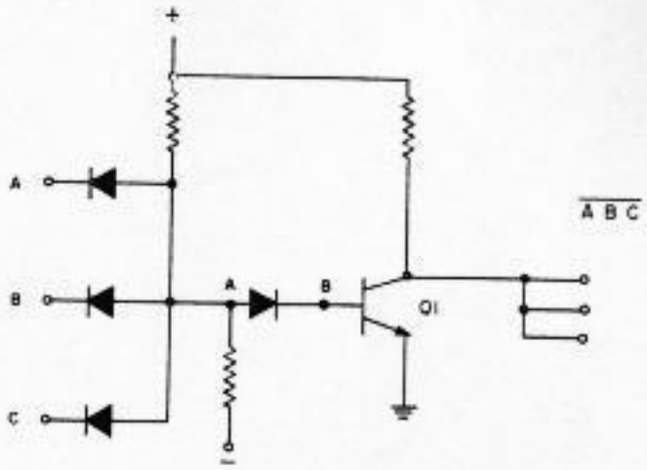


Figure 12. LLL Circuit

c) Since the coupling transistors are never back-biased, the charge storage problem is reduced thus increasing the speed of operation.

d) TTL has a lower noise margin than other types of logic circuits.

e) TTL is flexible; its low-level operation makes it possible to operate these circuits in conjunction with conventional DCTL circuits.

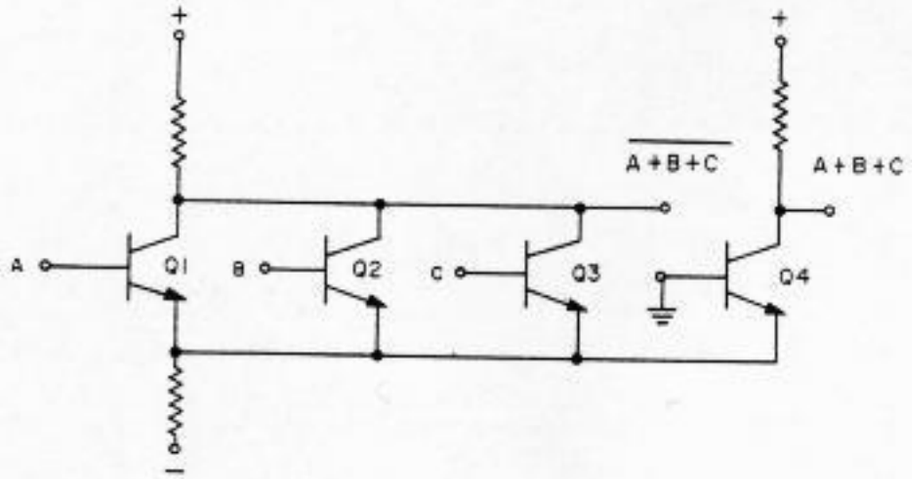


Figure 13. CML Circuit

Criteria for Use in W. U. Application

The factors which are considered most important to Western Union in considering integrated circuits over discrete logic in communications and data processing applications are *reliability, maintainability, propagation speed, uniformity, packaging density and cost.*

Reliability

Since the integrated circuit processes produce a number of planar transistors simultaneously and the circuit interconnections are reduced to a minimum, the overall effect is a more reliable circuit than a circuit comprised of a number of discrete elements. The nature of the integrated circuit process permits the manufacturer to design such circuits as the transistor-transistor logic which is a more reliable circuit than could be economically obtained with a discrete component design.

Maintainability

The maintainability of a circuit is a function of the frequency of failures and the cost of correcting them. The probability of failure of a printed-circuit card containing integrated circuit packages is less than the discrete component printed-circuit card because the number of connections and individual components are reduced. When the individual integrated circuit package develops a malfunction, it is necessary to replace this individual package because the integrated circuit cannot be repaired. While this may appear to be expensive, the considerable savings in time for test and removal of the integrated circuit module will far outweigh the cost of repairing faulty cards made up of many discrete components. The inherent reliability of integrated circuits is such that maintenance problems should be greatly reduced.

Propagation Speed

The reduction of the length of wiring interconnections plus the uniformity of the transistor fabrication, with low leakage and uniform beta spread, results in propagation speeds adequate for many Western Union applications. For example, a 7-input NOR gate of integrated design now being used in a prototype unit has a switching time of 25 ns (nanoseconds), with high capacitive loading.

Uniformity

The fabrication process of the monolithic integrated circuit with its mass production of transistors per wafer insures that the gain or beta of the transistors is close to design specifications.

Packaging Density

Western Union does not usually place a premium on packaging density in circuit design. Integrated circuits offer the circuit designer small units which provide complete circuits. Switching circuits using the digital computer as a processor requires increasingly higher speed operation. The standard logic card and the associated wiring in the connecting cable, limits the propagation speed. Therefore, it is necessary to consider the small packaged integrated circuits with the reduced interconnections and low beta gains, in current and future applications.

Cost

Integrated Circuits are much more economical to manufacture than a discrete transistor because thousands of components can be obtained from a single wafer. In making discrete transistors, 2000 is about the limit per wafer because individual dice must be large enough for handling and attaching wires. In I-C s, the interconnections are made within the wafer and the only limitation is the resolution of the circuit processes. The cost of processing a wafer does not depend on what the wafer contains—one transistor or a thousand, one circuit or a thousand. The cost of processing an I-C is somewhat more than a transistor because more steps are involved (etches, diffusions, etc.) but when processing is prorated against many circuits, the cost per circuit function is low. For example, an I-C employing 10 transistors per circuit can reduce the cost per transistor to one-tenth that of an industrial discrete transistor. In more complex integrated circuits the cost per transistor can be reduced by a ratio of as much as 100 to 1.

I-C in Western Union Switching Circuits

In the application of integrated circuits to Western Union switching circuits consideration is given to the criteria listed above in the selection of available types of integrated circuits for use in new equipments.

Three additional factors are considered in the final selection of an integrated circuit for industrial use. These are:

High noise immunity
High dc fan-out
High capacitive drive capability

a) *High noise immunity* is an important factor in the selection of I-Cs. Digital systems are often plagued with electrically noisy environments associated with peripheral equipment such as teleprinter motors, switching relays, and other generators of wide band noise. Noise problems in large systems require much effort in debugging circuits.

b) *High dc fan-outs* mean system economy because buffers required to drive long chains of gates or flip-flops can be eliminated. High fan-out is desirable in both gates and binaries.

c) *High capacitive drive capability*, is necessary in large systems, such as those employed by Western Union, where long lines and connecting wires constitute a considerable capacitive load. In large systems a considerable amount of power is relegated to charging and discharging line capacitance.

A typical low-cost I-C circuit family, developed in accordance with these general criteria, are now being tested. Some of the characteristics are as follows:

Circuit Type	Noise* Immunity (volts)	Propagation** Speed (nanoseconds)	DC Fan-Out
Dual Nor	1.2	30	17
Flip-Flop	1.2	65	17

* Noise immunity is defined as the difference between the worst case output level and the worst case input threshold.

** Measured driving a 1.6K ohm resistor in parallel with a 130pf capacitor.

The logic circuit group now under consideration at Western Union which generally meets the factors given above consists of the following three basic circuits: Dual Nor Gate, 7-Input Nor Gate, and J-K BINARY ELEMENT.

Dual Nor Gate

One half of the basic DUAL NOR GATE circuit is shown in Figure 14, since the other half is symmetrical. In this circuit which employs TTL logic, the liberal use of transistors provides the necessary gain without requiring high betas. The integrated circuit permits the use of many transistors, at a minimum cost. This obviously is not the case in discrete circuit designs. The NOR circuit of Figure 14, uses emitter-follower inputs (Q_1, Q_2, and Q_3) to provide low input currents necessary for high fan-outs. The input thresholds are determined by the resistance ratios of the dividers in the base circuits of Q_4 and Q_6 and the Vbe of the input transistors. These ratios are adjusted so that Q_4 always turns "on" at a lower voltage than does Q_6. This insures that both output transistors cannot be turned on simultaneously, which minimizes the possibility of "turn on" due to supply voltage noise.

Diode D1 is a form of saturation clamp. Transistor Q_6 is allowed to saturate so that the low level outputs of saturated operation is obtained. Resistor R7 has an important function in that it provides limiting in cases of accidental output grounding.

7-Input Nor Gate

A 7-INPUT NOR GATE circuit is shown in Figure 15. This TTL circuit is identical to the NOR GATE of Figure 14 except that provision is made for seven inputs. The use of 10 transistors in this gate circuit is a good indication of the ease with which integrated circuit fabrication can produce uniformly designed, low-cost transistors. A similar discrete component standard logic card, employing a like number of transistors, would be very expensive and would occupy a large package.

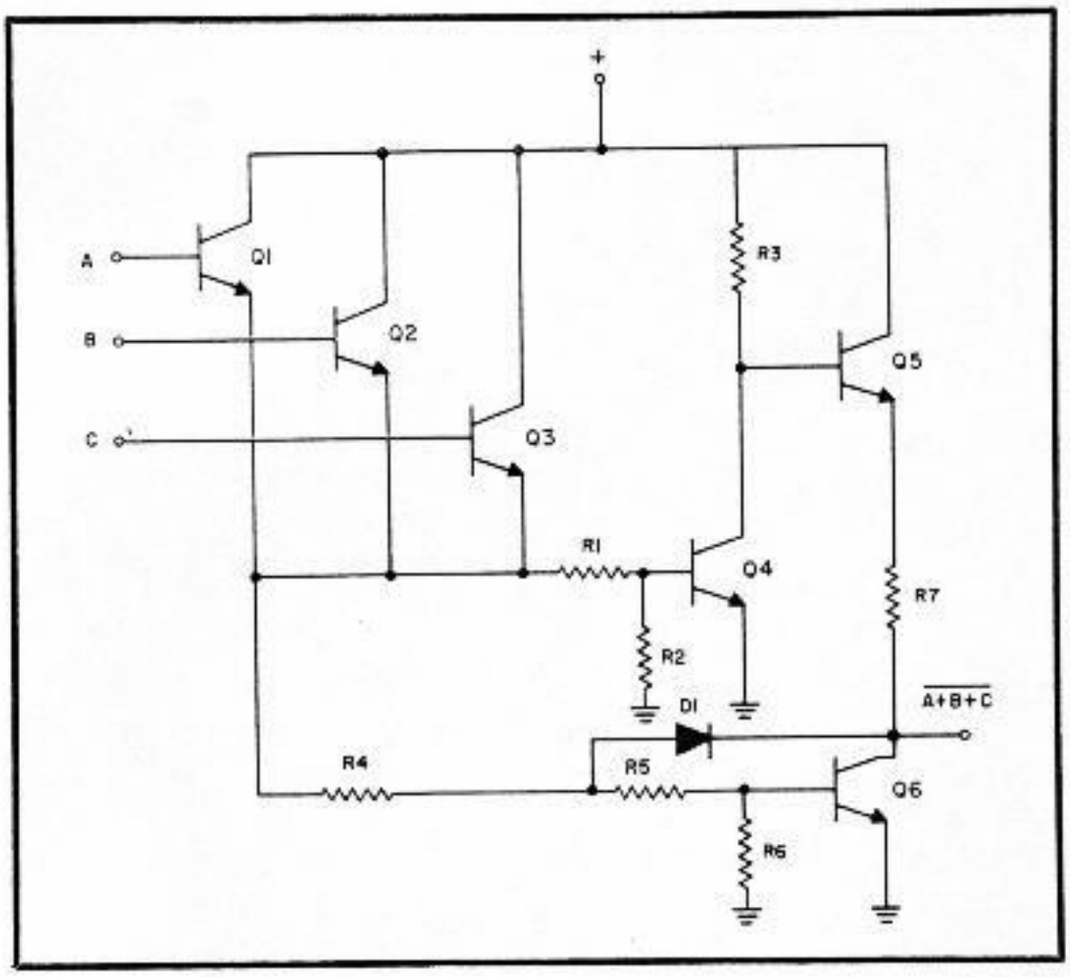


Figure 14.
DUAL NOR GATE

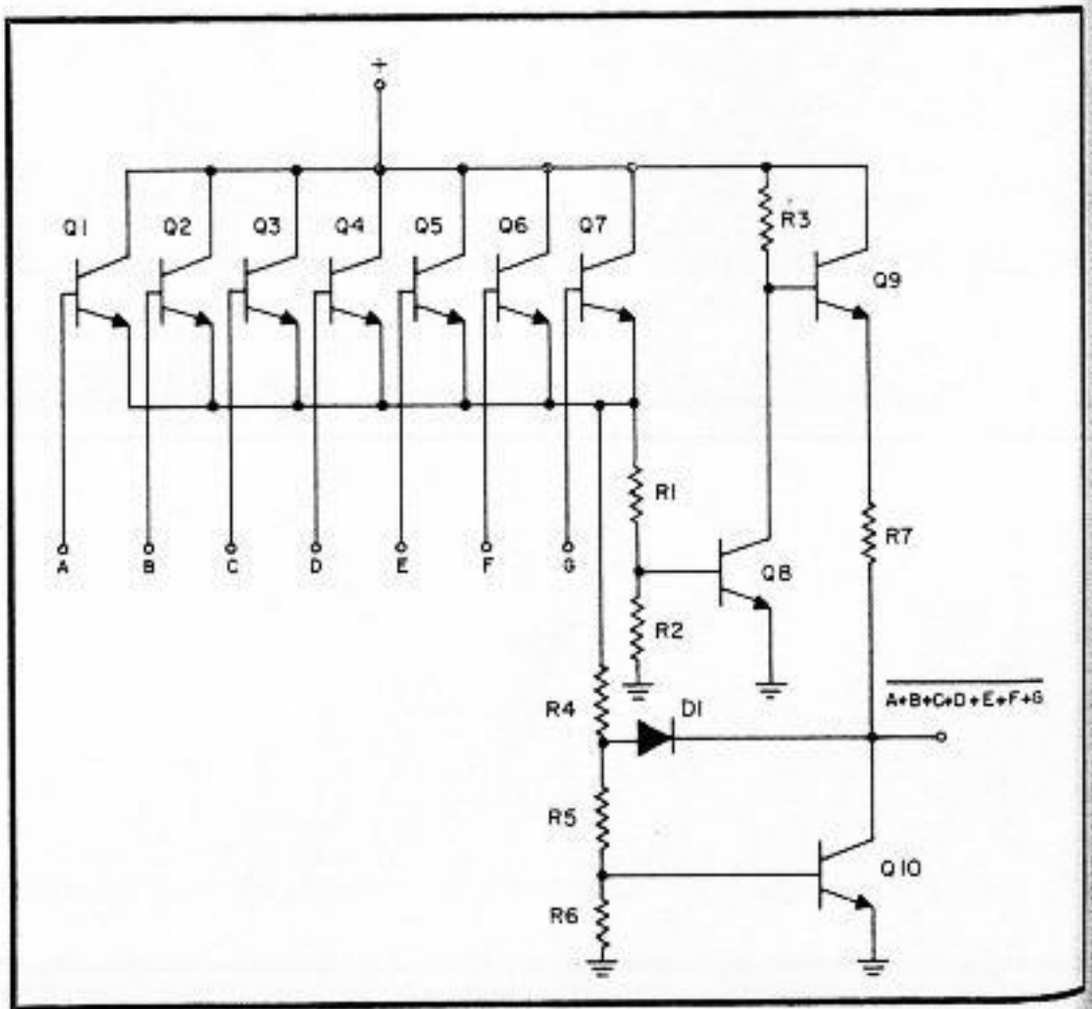


Figure 15. 7-Input
NOR GATE

12(a)

J-K Binary Element

Figure 16, shows the circuit schematic for a J-K BINARY ELEMENT. The J-K BINARY ELEMENT or flip-flop can be described as a circuit which is capable of changing to the complement of its previous state when a logical "1" is applied simultaneously to the J-K inputs. The illustration shows a large number of diodes and transistors in this circuit. All these elements of the circuit are contained on a silicon wafer within the TO-5 package shown in Figure 2(a). The diameter of the TO-5 package may be compared with the dime which is used for comparison. The degree to which complete circuits can be compressed is obvious.

into a customized switching circuit, must now reorient his design approach. The engineer is required to work with functions rather than components.

The reduced size of the package, whether the TO-5 can, or the flat package requires new connection concepts. There is considerable difference of opinion in the electronics industry as to whether soldering, welding, or the use of individual sockets are the most satisfactory means for connecting these compact devices.

Monolithic integrated circuits operate at much lower voltages than the previous standard discrete component logic circuits. For example, typical I-Cs, operate with a standard voltage of —(minus) 4.5V applied to the collector terminals.

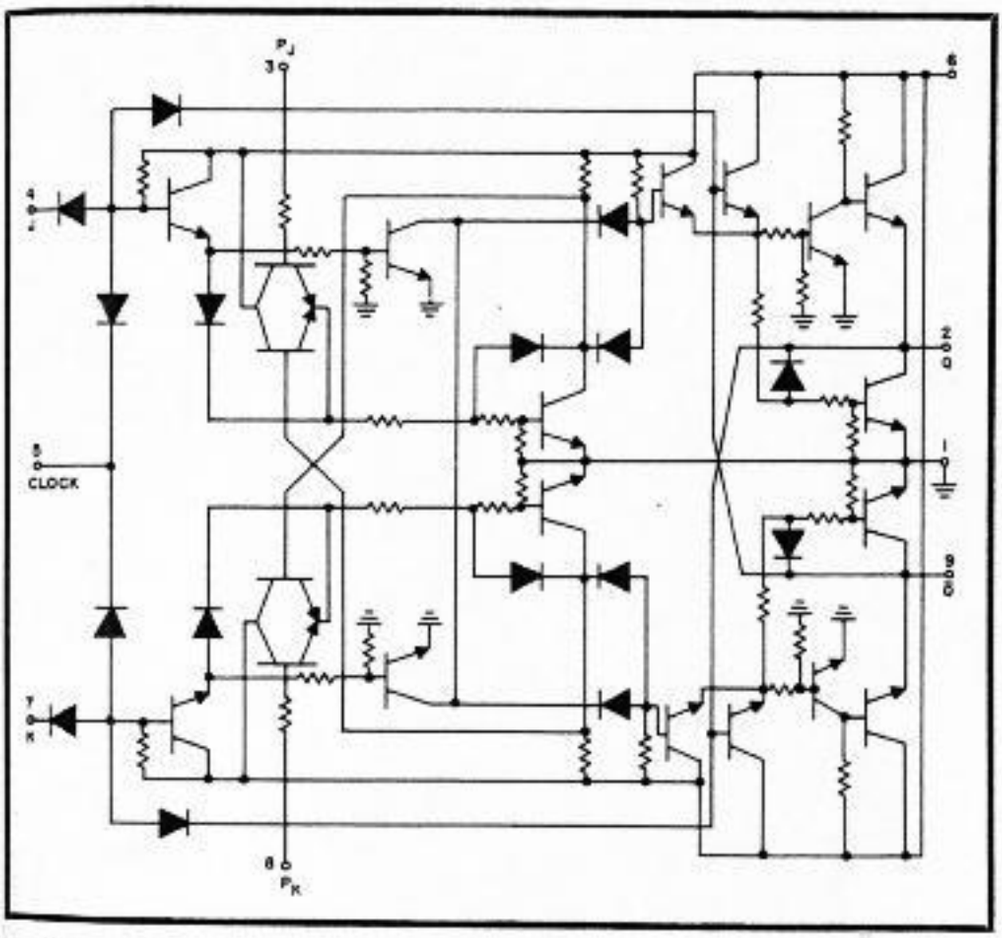


Figure 16. J-K Binary Element

Problems Peculiar to Integrated Circuits

As pointed out earlier in this article the integrated circuit concept entails problems which call for new demands on the ingenuity and skill of the development engineer, such as:

The use of the integrated package with the complete circuit requires that the switching engineer, previously concerned with circuit components and assembly

The power supplies used with these circuits must have overvoltage protection to prevent damage to the I-C circuits.

The use of low voltages requires that all mechanical contacts such as relays and switches must be plated with non-oxidizable noble metals and that adequate contact pressures must be used to reduce contact resistance.

The Future Potential of I-Cs

There is every reason to believe that in digital circuit design the monolithic I-C will rapidly replace the standard printed circuit card using discrete components, just as the latter replaced the vacuum tube and the relay.

As system designs become more standardized and are reproduced in quantities, the completely integrated logic functions for such systems will be contained within one TO-5 can. Complete shift register circuits are now being produced for the computer, military, and aerospace industries in this type of package.

Since the I-C circuit is a low-power device there will still be a need for the peripheral devices such as the discrete component package, and fast acting relays.

The use of mass produced I-C will lower system costs and make possible more efficient systems.

Integrated circuits can be used to provide other system elements used as amplifiers and oscillators.

Acknowledgement

The authors wish to acknowledge the suggestions and guidance of J. Elich, Senior Project Engineer in the Switching System Division.

Further Reading

A bibliography such as the following is recommended for additional reading:

1. Motorola Monitor, Vol. 2 No. 2, Motorola Semiconductor Products Inc.
2. "Microelectronics—Where, Why, and When?", Electronic Industries, Sept. 1965 Pgs. 32 to 36.
3. Custom Microcircuit Design Handbook, Fairchild Semiconductor.
4. Motorola Integrated Circuits, Advanced Fabrication Techniques, brochure by Motorola Semiconductor Products Inc.
5. Utilogic, Integrated Circuits for Military GSE and Industrial Applications Signetics Corp.
6. Integrated Circuits for Commercial/Industrial Applications, Willard T. Booth, Data Systems Design Dec. 1964, Vol. 1 No. 12. Pgs. 15 to 18.
7. Reliability Report, 1962 Semiconductor Networks, Texas Instruments, Inc.
8. The Major Design Principles of Digital Monolithic Circuits, A. B. Philips Computer Design, Vol. 4 No. 2 Feb. 1956, Pgs. 12 to 26.
9. Transistor Manual, Seventh Edition, General Electric Co.
10. Introduction to Integrated Semiconductor Circuits, Adi J. Khambata, John Wiley and Sons, Inc. 1963 Edition.
11. Microelectronics, The Lenkurt Demodulator Vol. 13 No. 4, April 1964.

MR. J. J. MCMANUS, Senior Project Engineer in the Switching Systems Division of the Information Systems & Services Department, has been engaged in the development and engineering of automatic switching systems such as facsimile concentrators, facsimile relaying by means of magnetic storage, Plans 57 and 59, and EMATS.

He joined the Western Union Telegraph Company in October 1952 and was assigned to the staff of the Switching Development Engineer of the R & D Department.

Mr. McManus received his BEE in Electrical Engineering from the College of the City of New York, in February 1938.

He holds a registered New York State Professional Engineers License and is a senior member of Institute of Electrical and Electronic Engineers.

Mr. J. D. Dorgan, Project Engineer in the Switching Systems Division of the Information Systems & Services Department, has been actively engaged in the design of the Communications Multiplexer, the development of printed circuit card testing equipment, and the preliminary design of magnetic drum storage circuits using integrated circuits.

He received his B.S. degree in Electrical Engineering from Villanova University in June 1961, after which he joined the Western Union Telegraph Company. He is a member of Etta Kappa Nu and Tau Beta Pi.

Western Union's Hot Line Service makes "COMMUNICATIONS NEWS"

Editorial Note: Our new service gained top publicity coverage in the July 15 issue of COMMUNICATIONS NEWS

Western Union Introduces Business Hot Line Service

Western Union is now offering a new inter-city private line business telephone service featuring instant automatic connections, with no dialing and no minimum-time charges.

The service is being offered initially between New York and Chicago at 2½ cents for each six seconds of use. A full minute's use, for example would cost only 25 cents.

The new private-line voice service, using a new "no-dial" Western Union telephones, was offered in a tariff filed with Federal Communications Commission and scheduled to become effective on June 20.

Service will be available only from a customer's station in one city to a station in another city. Charges are based on the total monthly time used which is meter recorded. There is a fixed monthly service charge of $40 at each city. Service will be available on a 24-hour, seven days a week basis.

The direct, automatic service, called Hot/Line, works like this: the caller lifts the telephone handset causing the distant-city telephone to ring instantly and automatically. There are no multi-digit numbers to call, no dialing and no telephone operators involved.

Hot/Line remembers to complete a call should a circuit be busy. The caller simply replaces the handset and the phone automatically rings back the caller and the called party the moment the circuit is available.

Extension telephones will also be offered shortly. Incoming calls will be received first on the master telephone. A call for an extension phone will be completed by the simple push of a button on the master phone to ring the extension. Extension telephones will be able to originate calls.

Conversation on the master telephone will be protected from eavesdropping by touching another special button. This will prevent any conversation from being heard on an extension telephone, thus permitting confidential matter to be discussed in privacy.

Voice circuits for the new Hot/Line service will be provided by Western Union's new transcontinental microwave system, insuring static-free operation.

"The fractional-minute charge makes our new Hot/Line service particularly attractive to a business with short-duration calls between two points" said G. S. Paul, Western Union's vice president of operating and marketing. The businessman who must have immediate access to key people in his organization's distant offices will find Western Union's Hot/Line service uniquely useful."

E. T. Finnegan, Senior Project Engineer—Information Systems & Services Dept.

Telex Switching Table

Traffic on Western Union's Public Message System is switched through the network and eventually directed to a tieline where it is delivered by messenger, facsimile or teleprinter. As the efficiency of the system has increased, little has been or could be done to reduce the time consumed delivering the "hard copy" into the hands of the addressee. One major advance in speeding up this delivery problem has been made with the Telex Switching Table, shown in Figure 1.

The automatic dial teleprinter exchange system introduced in 1958 as Western Union's U.S. Telex Network and the large subscriber acceptance of it has eased the message delivery problem within Western Union's Public Message System. What was originally intended only as a nationwide teleprinter exchange has become, by serendipity, an efficient and reliable message delivery system.

The original version of the equipment was conceived in 1962 and has operated with success in New York City. The solid-state version with improved automatic operating features has recently replaced the original model.

Utilization of the Telex Exchange for delivering traffic from a Public Message System is accomplished with a Telex Tieline Switching Table. The equipment operates as a tieline out of Plan 38 Switching System in New York and as a Telex subscriber set into the Telex Exchange. A message received in the Plan 38 Switching System with an addressee who is a Telex subscriber, is routed into the switching table where it is received on a printer-perforator. For record purposes, a "hard copy" is made on a burster printer located externally to the table.

The message is switched on a torn-tape basis into a sending position that simulates a Telex subscriber set. Three sending positions are available on the table to allow more rapid handling of traffic. Each sending position consists of a transmitter-distributor, a remote control unit (dial box), a monitor printer, and supporting solid-state control circuitry. Common to all three positions are a keyboard, by which correction of text is made, and a Teletype LABD 500 Answer-Back Unit which is used to identify the sending station at the beginning of each message. This identifying format is suffixed with a FIGURES D which automatically triggers the answer-back mechanism of the "sub-set" to verify that the correct connection has been executed.

After a message is received on the printer-perforator, it is placed in one of the transmitter-distributors and the addressee's Telex number is dialed for a connection. Once a connection has been established and verified as correct, the message is transmitted.

The incompatibility of the PMS and Telex keyboards is resolved by an automatic translating circuit. The Upper Case D or the $ sign on the PMS keyboard is not compatible with that on the Telex keyboard. On the Telex keyboard, the answer-back triggering character is the upper case "D." This circuit reads the upper case D as it appears over the transmitter pins and converts it to an upper case F before the character is transmitted to the line. The original version of the equipment required the operator to manually convert the upper case D to an upper case F with a tape editor.

The standard End-of-Message charac-

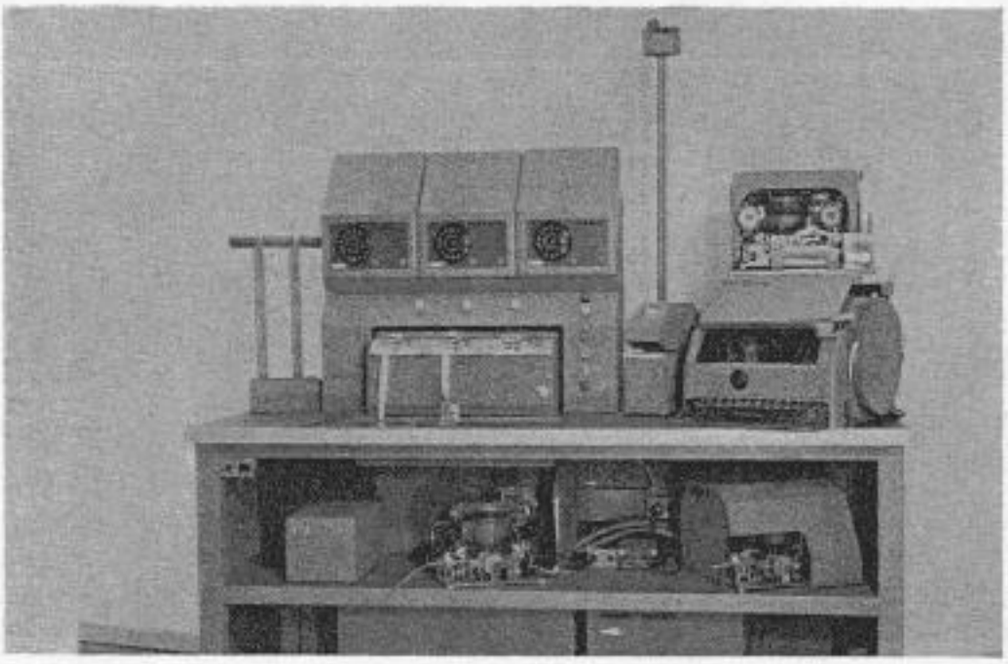


Figure 1. Telex Switching Table

ters (a double carriage return) are read by the control circuits to initiate a disconnection from the Telex line loop. To permit the form-feed sequence of line feeds to be sent to the line, the actual disconnect is delayed until the "tape-out" pin on the transmitter-distributor is actuated.

Text corrections are made by notching the tape at the errored character prior to placing the message in the transmitter-distributor. This notch actuates the "tape-out" pin which halts transmission. The operator then pushbuttons the keyboard into the Telex line loop, makes the necessary corrections, moves the tape to reclose the contacts of the "tape-out" pins, and cuts out the keyboard to resume normal transmission.

While the application of Telex Tieline Switching Table is limited to the larger Telex exchange cities (where the volume of traffic in the PMS is substantial), its success has warranted additional installations. Present plans indicate installations to be made at New York, Chicago and Los Angeles.

Mr. E. T. Finnegan, senior Project Engineer in the Telegraph Equipment Division of the Information Systems and Services Department, has been associated with the development of solid state telegraph equipment since 1962. Recently he was responsible for the design of a new solid state regenerative repeater and certain aspects of the Data Card Transmitter. He played a major role in the design of the transmission plant recently installed for the American Stock Exchange and is well-versed in all aspects of the Western Union Public Message System.

Mr. Finnegan received his BEE degree from the Polytechnic Institute of Brooklyn in June, 1953, after which he joined the Western Union Telegraph Company. He was assigned to the Electronics Applications Engineer where he engaged in the Development of terminal equipment for the Ocean Cable Division. This included design of cable test equipment, multiplex systems and automatic switching systems and several special systems such as the one for the Italcable Company.

S. A. Romano, J. F. Gross, A. Portnoy

Engineers—Information Systems & Services Dept.

Solid State Facsimile Transceiver

The Transceiver is a 300-rpm, solid-state, drum-type, facsimile transmitter/receiver that handles letter-size copy. It utilizes a 3-kc voice-band and requires only three minutes for transmission of a full 8½" x 11" copy over a four-wire switched system.

When used on the Broadband Exchange Service with a broadband telephone, it provides a terminal for alternate voice-facsimile operation. The use of facsimile provides the customer with a basically error-free, record communications system.

The introduction of switched four-wire networks such as the Broadband Exchange Service has produced a facility for alternate voice-facsimile transmission between subscribers on the network. This enables a subscriber to dial a distant number, establish a voice connection, and switch to facsimile transmission to send a letter, sketch or diagram over the same network. Line charges are based on actual time used on the network instead of fixed monthly lease charges as for a non-switched system.

To implement this service a 300-rpm Facsimile Transceiver 11567-A has been designed, which:

a) operates as either a facsimile transmitter or receiver over a voice band,

b) sends or receives facsimile of letter-size text such as typewritten letters, sketches, diagrams, handwriting and the like,

c) transmits an 8½" x 11" copy over a voice band in 3 minutes, which is half the time required by conventional equipment,

d) uses solid-state electronics throughout (no warm-up time or standby power is required),

e) is a drum-type, manually-loaded unit using TELEDELTOS* paper for recording,

f) accommodates several types of dry electrosensitive paper,

g) incorporates a simple synchronizing system which uses the return line pair to transmit a sample of the distant power line frequency, and

h) automatically controls the gain of received line signals, to maintain a constant density of recording.

A subscriber's voice-facsimile terminal is shown in Figure 1. The Facsimile Transceiver and Broadband Pushbutton Telephone is shown on top of a cabinet which contains a telephone control unit, a power supply and a motor-drive amplifier. A modem unit is not required in most data installations. Three push buttons on the front of the Transceiver operate as follows: The OUTGOING button to send a message, the INCOMING button to receive a message, and the STOP button to halt operation of the machine.

* Registered Trademark

Operation

When a subscriber in one city desires to transmit a document or message to a subscriber in another city, both are connected to the network with the equipment shown in Figure 1. The procedure for sending the message is as follows:

The calling subscriber places the message around the drum of the Transceiver, moves the carriage lever to the START position and presses the OUTGOING pushbutton. The subscriber then lifts the handset of the telephone and depresses the pushbuttons on the telephone unit in a sequence corresponding to the called party's Broadband Exchange number. This causes the called party's telephone to ring. When the handset of the called subscriber is lifted out of the cradle, both phones are connected via a four-wire voice network. The first subscriber then informs the second that he wishes to transmit a message by facsimile. The second subscriber, whose Transceiver has previously been loaded with a recording blank, now presses the INCOMING button, and both parties place their handsets in the data cradle located at the rear of the subset. This causes the four-wire line connections to switch from the telephones to the facsimile machines.

The transmitter drum now rotates and sends phasing pulses to the Receiver. The recorder drum, at the Receiver, runs at a speed slightly less than that of the Transmitter until the drums on both machines are properly aligned. At this time, the recorder drum rotates at the same speed as the Transmitter drum and actual facsimile transmission takes place. The carriages on both machines begin to move, the copy is scanned photoelectrically at the transmitter, and a facsimile recording of the copy is made on electrosensitive recording paper at the Receiver. When the transmission of the message is completed, buzzers sound at both facsimile machines thus signalling the subscribers to return the carriage to the LOAD position. This stops the buzzers and allows the copy to be removed. The subscribers then lift their handsets, thereby switching back to the "voice mode" where they can confirm the satisfactory reception of the message by telephone. Both parties then return their handsets to the phone cradle which causes the circuit to be disconnected.

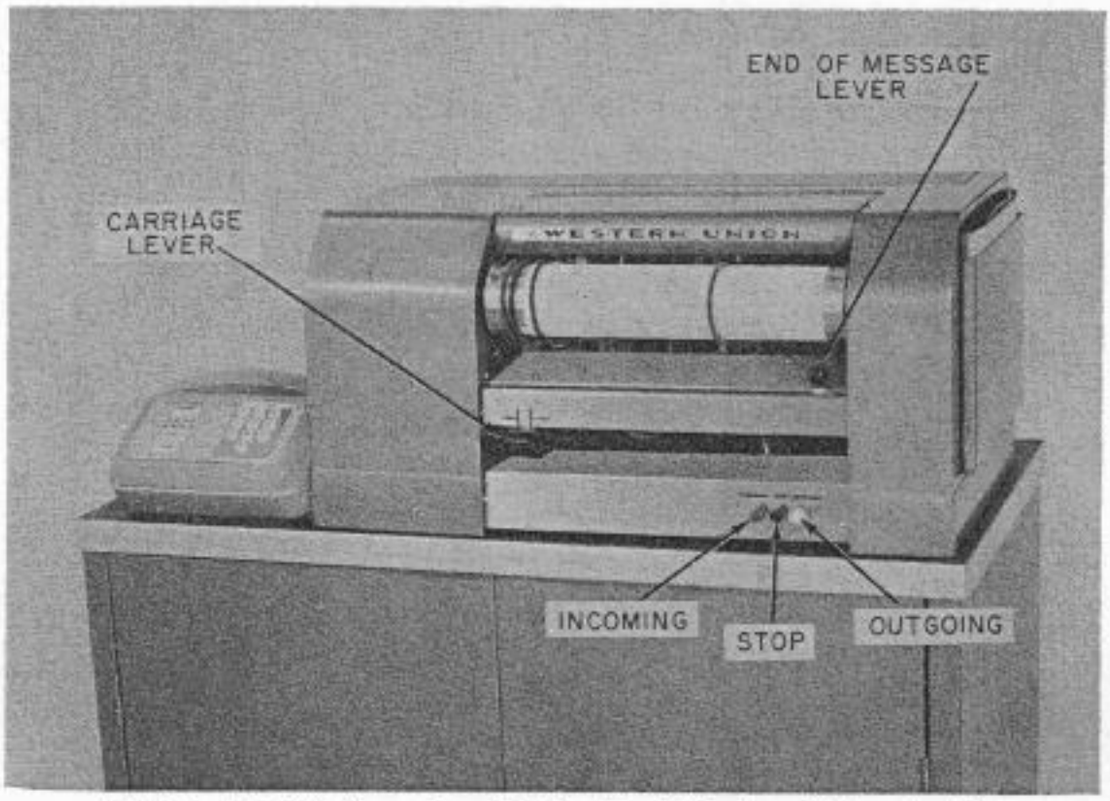


Figure 1. Facsimile Transceiver with Broadband Telephone Unit on the left

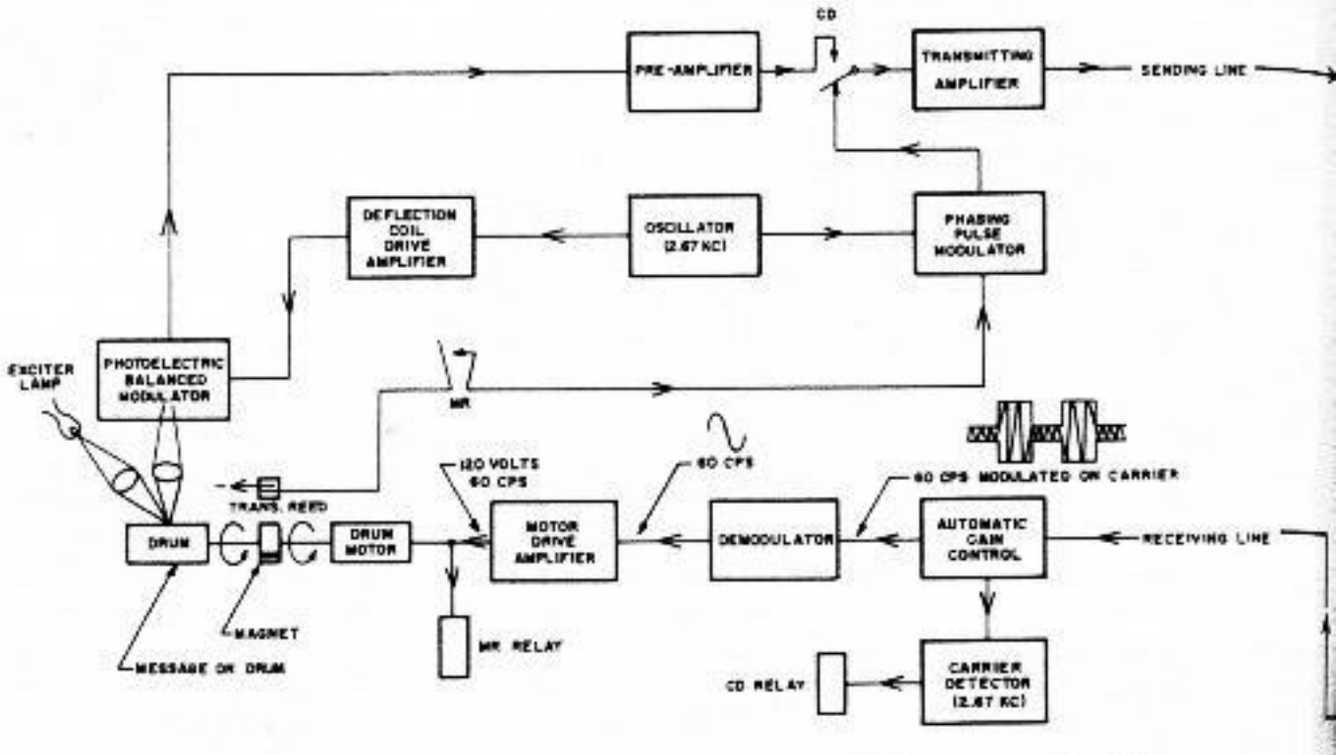


Figure 2(a). Block Diagram of Transmitting Circuitry and Signal Shape Transmitted

The functional block diagrams are shown in Figures 2(a) and 2(b). These diagrams also illustrate the signal shape at various points in the circuitry. Figure 2(a) shows the condition of the circuits when the OUTGOING button of the Transceiver is depressed. Figure 2(b) shows the condition of the circuits when the INCOMING button is operated.

(a) Transmitter

In Figure 2(a) the subject copy is scanned by a light beam originating from an Exciter Lamp, mounted on a moving carriage with the Photoelectric Balanced Modulator and the Pre-Amplifier. The light reflected from the subject copy into the Photoelectric Balanced Modulator causes a carrier signal to be amplitude modulated.

The modulator produces a maximum amplitude of carrier signal, when white subject copy is scanned—and minimum amplitude, when black copy is scanned. The contrast, or ratio between the maximum and minimum level of carrier signal, is adjusted in the Modulator to be approximately six to one.

The Deflection-Coil Drive Amplifier takes the 2.67-kc carrier signal from the Oscillator and amplifies it sufficiently to drive the deflection coil of the Photoelectric Balanced Modulator.

The signal from the Modulator is then coupled to the Pre-Amplifier, which provides a suitable impedance-match between the Transmitting Amplifier and the Photoelectric Balanced Modulator.

The Transmitting Amplifier accepts the low-level signal from the Pre-Amplifier and delivers an amplified signal to the sending line. The amplifier contains a vestigial filter which passes the lower sideband and a small portion of the carrier and upper sideband of the modulated signal.

The signal for the Motor Drive Amplifier originates at the Receiver, where a sample of the 60-cps power line frequency is used to modulate the carrier, and is sent to the Transmitter. Here it passes through the Automatic Gain Control circuit, shown in the lower portion of Figure 2(a), where the sample is recovered in the Demodulator. This sample is amplified to 120 volts at a power level

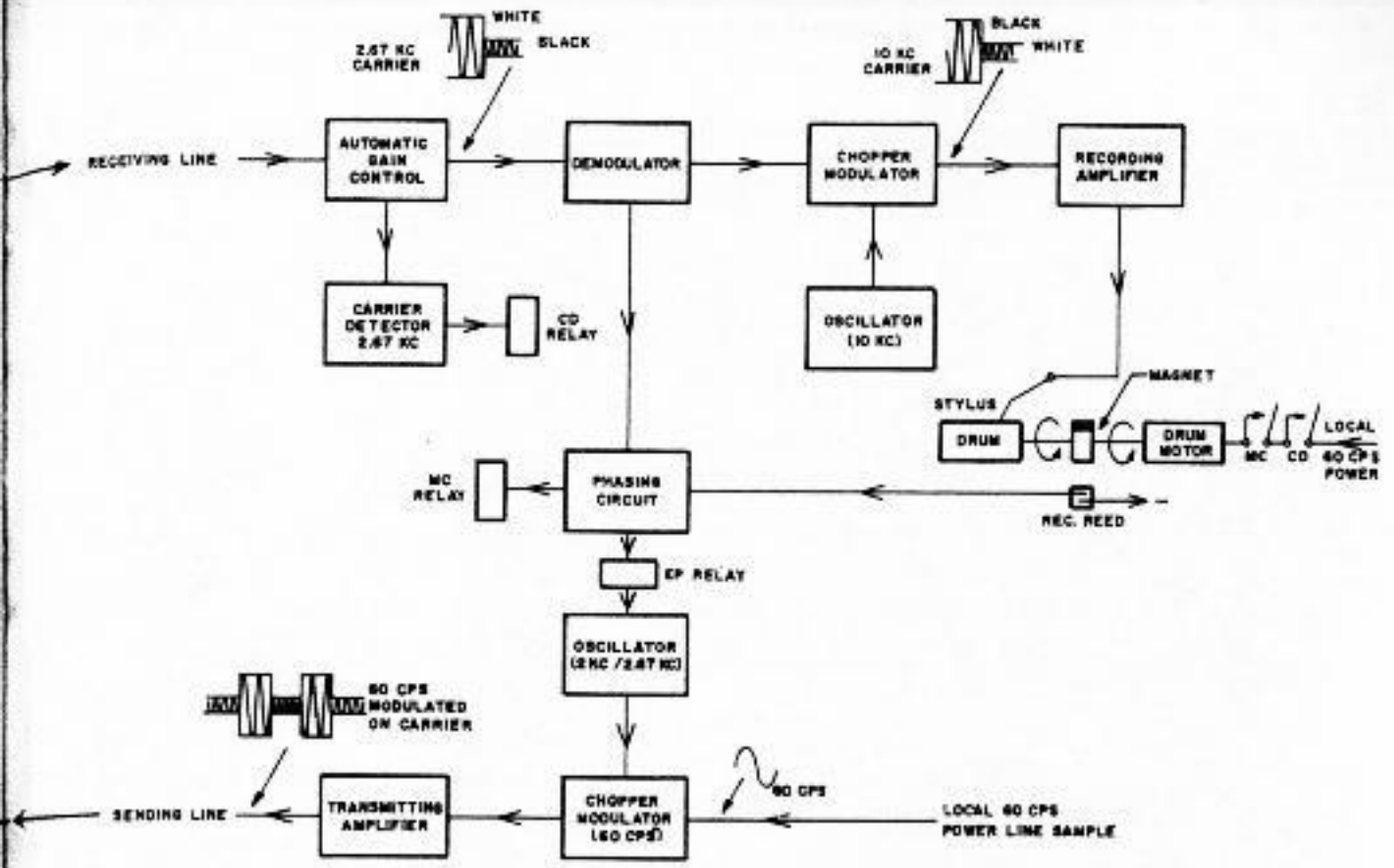


Figure 2(b). Block Diagram of Receiving Circuitry and Signal Shape Transmitted

sufficient to drive the drum motor in the Transmitter.

(b) Receiver

In Figure 2 (b) the "Incoming" signal to the Receiver may be subject to many variations due to differences between various transmission facilities. For this reason, an Automatic Gain Control circuit is used to correct signal-level variations of as much as 40db.

Because the maximum line signal (full carrier) represents the white background of the subject copy, the signal must be inverted to record correctly. To invert the signal, the envelope of the modulated wave is recovered in the demodulator stage and is then used to modulate a 10-kc carrier in the Chopper-Modulator in such a manner that the maximum carrier represents black subject copy. The inverted signal from the Chopper-Modulator is then fed to the Recording Amplifier, where it is amplified sufficiently to record. A 10-kc carrier is used to achieve optimum recording on a variety of recording papers. The higher frequency also results in a more dense recording mark.

At the Receiver terminal a sample of the local 60-cps power line is used to modulate a 2.67-kc or 2-kc carrier (depending on whether or not phasing has occurred) in a Chopper-Modulator. This signal passes through the Transmitting Amplifier to the Sending Line. This signal eventually serves to operate the drum motor at the Transmitter.

Carrier Detection

Proper drum alignment is detected by producing commutator pulses at both drums. The Transmitter pulse information is sent to the Receiver. When both pulses occur simultaneously, the drifting of the recorder drum stops and a signal is sent to the Transmitter in the form of a change in carrier frequency. The change in carrier frequency operates the carrier detector (CD) relay. This relay switches the signal path, so that the Transmitter sends facsimile signals and causes the transmitter carriage to move thus completing the phasing sequence.

Fundamental Principles

The fundamental principles of a drum-type facsimile transmitter are well known.[1] They may be reviewed briefly here:

At the Transmitter

a) a light source produces a small bright area on the message;

b) the reflected light is imaged through an aperture onto a photocell;

c) when the drum rotates, the variations in reflected light—from the dark and light areas on the message—combined with the alternating magnetic field applied to the photocell, produce an amplitude-modulated facsimile signal. This is an analog of the black and white portions of the message; white portions produce a large carrier amplitude while dark portions produce a small amplitude;

d) The amplitude-modulated signal is amplified and sent out on one of the two line pairs of the 4-wire transmission circuit.

At the Receiver

a) the signal is passed through an Automatic-Gain-Control (AGC) unit which maintains a constant output signal level despite input signal changes of as much as 40db;

b) the amplitude-modulated signal is "inverted" thus dark areas generate large amplitude signals and light areas generate small amplitude signals;

c) these signals are amplified and applied to a stylus in contact with the recording paper on the drum. The result is a facsimile reproduction of the original message.

Synchronization and Phasing

For true facsimile reproduction, the transmitter and recorder drums must rotate at the same speed. To accomplish this, the drums are operated by synchronous AC motors. Thus, the receiver motor is operated directly from local AC power, while the transmitter motor is operated from a sample of the same power frequency.

Framing of the message, or "phasing," is accomplished as follows: At the beginning of each transmission, the transmitter sends drum-position information in the form of modulated phasing pulses. The leading edge of these pulses occurs when the spot of light crosses the overlapped edge of the copy. The pulses are produced by a commutator comprised of a magnet on the drum shaft which operates a reed switch once every revolution of the drum. The recorder drum produces phasing pulses also, the leading edges of which occurs when the recording stylus crosses the edge of the record sheet.

At the Receiver the drum is rotated at a reduced speed by periodically interrupting the power to the drum motor. The receiver and transmitter phasing pulses are compared and when the leading edges are coincident, both drums are aligned. A "coincidence circuit" recognizes this fact and causes (a) the Receiver motor to run at normal speed, (b) the Receiver carriage to move and (c) a signal to be sent to the Transmitter in the form of a change in carrier frequency. The change in frequency operates a carrier-detector relay, which in turn, starts the transmitter carriage moving and starts the sending of facsimile signals.

Controls

The control circuits in the Transceiver provide automatic operation so that, when the transceiver drums have been loaded and the voice connection established, it is only necessary to depress an OUTGOING or INCOMING button to operate the Transceiver. It will proceed to phase, transmit facsimile signals, and sound the buzzer at the completion of the transmission. The operator at either Transceiver terminal may turn the machine on first, but transmission will not take place until (a) there is a powered transceiver at both ends of the circuits, (b) the push buttons at *both* machines are operated, and (c) both line pairs are connected with the handsets in the DATA position. An adjustable "End-of-Message Lever" is provided to permit sending short messages.

Packaging

For ease of handling, the Transceiver has been divided into three separate units: a main unit and two auxiliary plug-in units called the Power Supply and a Motor Drive Amplifier. A Console is provided so that the Transceiver and Broadband Telephone may be placed on top. The auxiliary unit and circuit equalizers are inside the console.

The Transceiver may be described as having four sections: a) Cover, b) Chassis, c) Recording Stylus Mechanism, and d) Electronics and Control Section.

a) The front of the removable Cover exposes the drum. It has a hinged section that opens to provide access to the stylus and carriage mechanisms. A second hinged section opens to expose the electrical controls and test points for adjustments, as shown in Figure 3.

b) The Chassis is the base to which the mechanism is shock-mounted and the circuit board assembly is attached.

c) The Mechanism consists of the motor-driven drum and carriage assembly. The carriage rides parallel to the drum and is driven by a synchronous clock-type motor.

The Recording Stylus may be removed easily from the carriage by loosening a knurled thumbscrew. The wire is positioned around the tabs of the stylus clip and is held rigidly in position as shown in Figure 4. A spare assembly is mounted in the cover.

d) The Electronics and Control Section comprises six circuit boards and a relay panel mounted at the rear of the unit. The circuit boards are mounted in two rows of three. These two rows of boards are pivoted at the bottom and may be folded out individually to permit accessibility for servicing. Interconnections to the boards are made with spade lugs on screw terminals, thereby providing easy replacement and servicing of these circuit boards. The relay panel is held in the same manner as the circuit boards and offers free access to the plug-in relays for servicing or replacement.

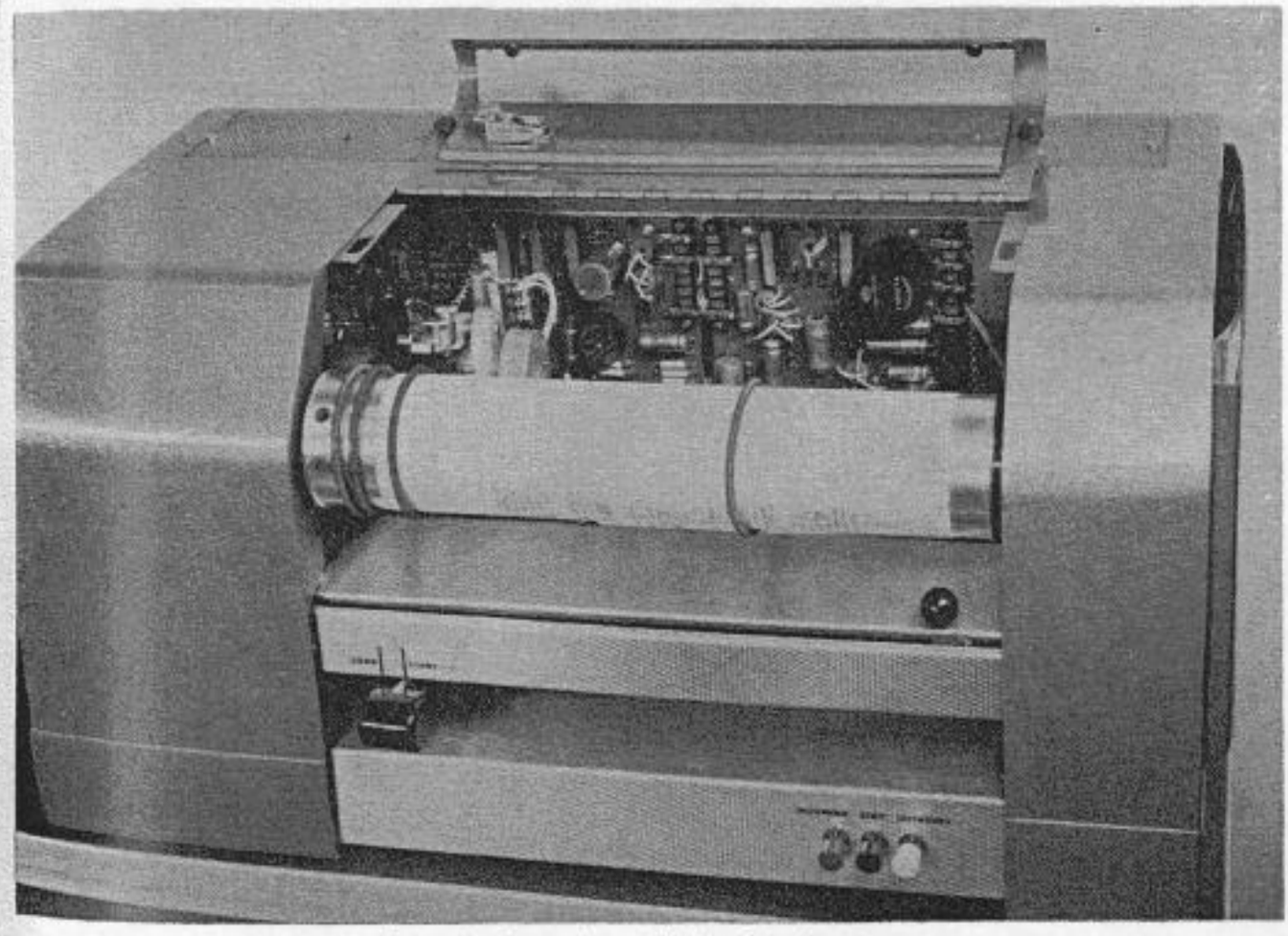


Figure 3. Transceiver with Hinged Section Open

Figure 4. Stylus Clip

Signalling

The following types of signals are sent over the two line pairs. Before phasing the Transmitter sends phasing pulses modulating a 2.67-kc carrier. For synchronizing purposes the Receiver sends back to the Transmitter a sample of the Receiver power line frequency modulating a 2-kc carrier. This sample is amplified and powers the transmitter drum motor. During this period the drum of the recorder is drifted into phase alignment with the transmitter drum. When alignment is completed, phasing at the Receiver occurs; the recorder is caused to run synchronously and the 2-kc carrier is changed to 2.67-kc. This operates a 2.67-kc carrier detector relay at the transmitter that switches the outgoing signals from phasing pulses to facsimile signals. The carriages on both machines now start moving. When the entire message has been scanned, the carriage trips the push buttons to remove power from both machines, a reed switch on the carriage of both machines is operated sounding the buzzers, thereby signalling the subscribers that transmission is completed.

When the copy is short, the operator at the Transmitter moves the "End-of-Message Lever" to a position opposite the end of the message. When the carriage has reached this position, it operates the reed switch which sounds a buzzer. This signal alerts the transmitter operator to stop the transmitter by depressing the STOP button. This sequentially removes the facsimile carrier from the line, releases the carrier detector relay at the receiver, and sounds a buzzer. Thus both subscribers receive an audible signal at the completion of the message.

Circuitry

The Transceiver is designed to operate continuously in ambient temperature as high as 55°C.

The Automatic Gain Control Amplifier changes an input signal of 40db to less than ¼ db at the output, with less than 1% total harmonic distortion. Gain control is achieved by varying the impedance of a shunt diode-bridge by changing the d-c current through the bridge.

The Transmitter Carrier Oscillator is designed for frequency stability and low distortion. A frequency stability of 5 cps for a temperature change of 20°C to 60°C and a 0.2% total harmonic distortion is achieved.

The Photoelectric Balanced Modulator consists of a photocell, which has a single photoemissive cathode and two symmetrically spaced anodes, with a magnetic deflection coil surrounding the photocell. Amplitude modulation is achieved by the inter-action of the electron beam and the magnetic field within the photocell.

The Pre-Amplifier converts the high-impedance output of the Photoelectric Balanced Modulator to a low-impedance output, so as to reduce noise pickup and capacitive effects. Any change of this impedance due to temperature or component change, will have a negligible effect on the output of the Photoelectric Balanced Modulator.

The Chopper-Modulator system of Carrier Translation and Signal Inversion obviates problems associated with direct-coupling. The original facsimile modulating signals are detected at a high level and then re-modulated by the chopper at a 10kc rate, with maximum carrier representing black copy.

Special Feature

The solid state circuitry of the Transceiver makes for greater reliability and low maintenance.

* * *

Reference

1. Facsimile Imaging Systems, Part I.
G. H. Ridings
Western Union TECHNICAL REVIEW
Vol. 18, Number 4. October 1964.

Acknowledgement

The authors wish to acknowledge the engineering assistance of other members of the Facsimile Division in the design of the Transceiver, and that of R. C. Taylor in the design of coils and transformers. In particular, we wish to acknowledge the supervision of D. Zabriskie for the mechanical design, G. B. Worthen for electronic design.

Mr. S. A. Romano, Project Engineer in the Data Systems Division of the Information Systems and Services Department has specialized in Solid State Circuit Design, and worked on many R & D projects for the company. He is responsible for most of the circuit design of the Transceiver described in this article.

Mr. Romano, received his Bachelor of Electrical Engineering Degree from Pratt Institute in June 1955 at which time he joined the Facsimile Division of Western Union. He has done some graduate study at Polytechnic Institute of Brooklyn.

Mr. Romano is a Senior Member of the I.E.E.E. He is a member of the Professional Groups on Engineering Management and Audio in the I.E.E.E.

Mr. Joel F. Gross is a Senior Project Engineer in the Facsimile Division, Information Systems and Services Department. Since joining Western Union in January 1954 Mr. Gross has been engaged in the design development and testing of facsimile equipment. His work has included optical and mechanical design of a Flat-Bed Involute Facsimile Transmitter. Recently he has been involved in the Mechanical design of the Broadband Transceiver.

Mr. Gross received his degree of Bachelor of Mechanical Engineering from New York University in 1953. He is a member of A.S.M.E.

Mr. A. Portnoy, Senior Engineer in the Facsimile Division of the Information Systems and Services Department, is engaged in the development and engineering of circuits and equipment. This has included work on Brokerfax, Slot-Transmitter, Desk-Fax Concentrators and Involute Flat-Bed Scanners.

He received his BEE from CCNY and joined Western Union in February 1948. He received his M.S. in E.E. from Columbia University in June 1964. Mr. Portnoy has a Professional Engineering License in New York State, is a Senior Member of the I.E.E.E., and is a member of the Study Group Committee of Communication & Electronics Division of I.E.E.E.

N. L. Feld, Project Engineer—Information Systems & Services Dept.

New
Punched Card Transmitter
For
Data Communications Systems

Part II
Punched-Hole and Pencil-Mark Sensing Modes

The Type 11890 Punched Card Transmitter was designed for low-to-medium volume transmission of data recorded on cards. It is capable of automatically feeding cards, one at a time, from a stack of up to 150 cards, and transmitting the information recorded on these cards to a telegraph line. The first model, which was described in Part I, was designed to sense numeric information recorded as punched holes in the 12-level Hollerith (IBM) code, and translate this information to the 5-level Baudot code.[1] The information can be transmitted over a telegraph line at speeds up to 100 words per minute.

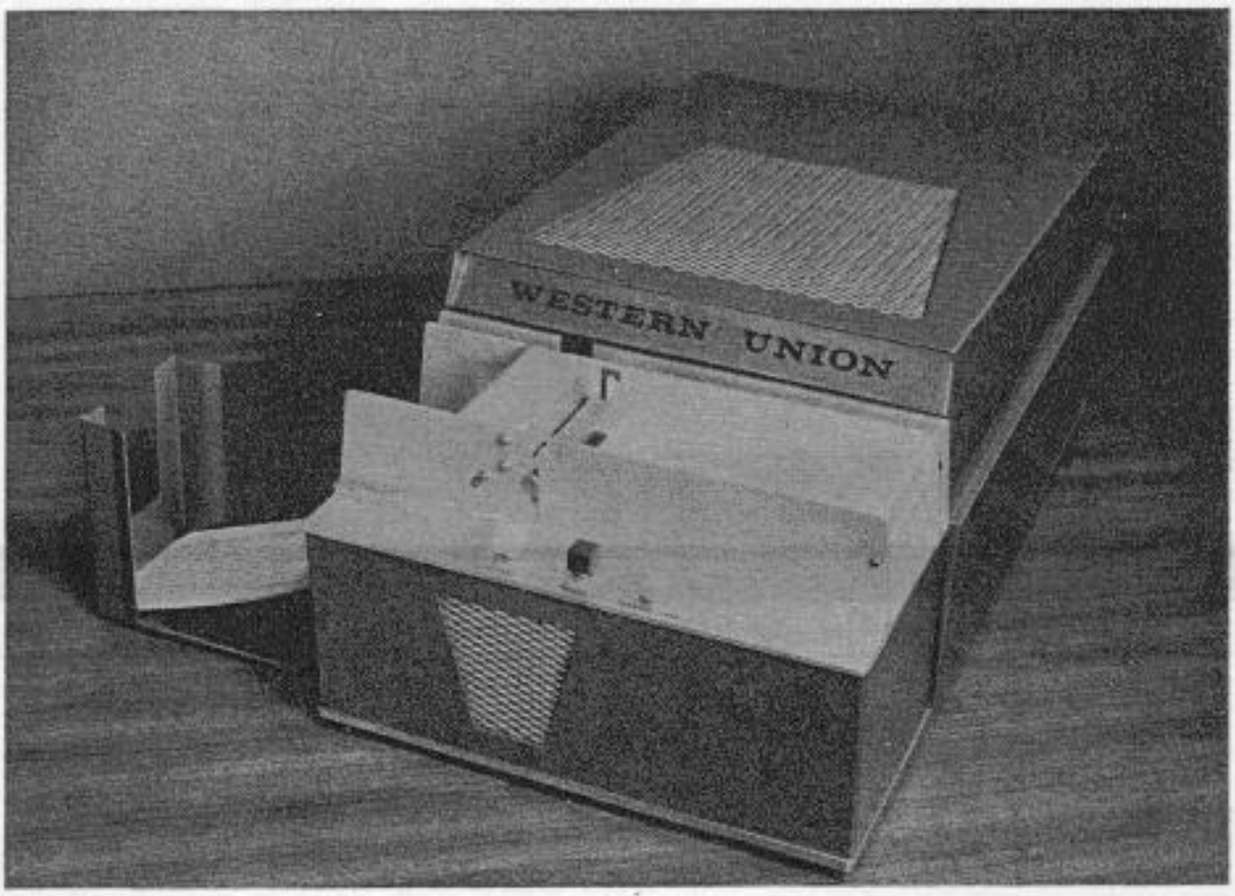


Figure 1. Punched Card Transmitter (second model)

Added Features of the Second Model

An improved model of the Punched Card Transmitter is shown in Figure 1. The following new features have been incorporated into this unit to give the transmitter added flexibility as a data input device:

a) Transmits ASCII as well as Baudot code.

The unit has been designed to translate information recorded in the Hollerith card code to either the 8-level ASCII or 5-level Baudot transmission codes. This makes the transmitter compatible with the new Model 35 8-level telegraph equipment as well as the Model 28 5-level equipment.[2]

b) Transmits information in proper format.

The Transmitter can transmit recorded information while retaining the original field format. That is, when columns on a card are not punched, the transmitter senses the blank columns and transmits a space character. When the transmitted information is recorded at the receiving station, the field format will be identical to that which appears on the original card.

c) Senses Alpha as well as numeric data.

Both letters and numbers represented in the Hollerith code can now be translated to either the ASCII or Baudot output codes. When translating from the Hollerith to the ASCII code, letters may follow numbers, in the transmission, without the necessity for transmitting a shift character. When translating to the Baudot code, however, the translation operation is different. Since some letters and numbers are identical in the 5-level Baudot code, a shift character must be transmitted to differentiate between the letters and numbers. Therefore, for translating from the Hollerith to the Baudot code, the transmitter has been designed to automatically generate the "Figures" and "Letters shifts," as required, without the need for any extra shift characters in the Hollerith coded cards.

d) Senses pencil-marked as well as punched-hole data.

Perhaps the most significant added feature of the second model is its ability to sense pencil-marked as well as punched-hole data. This feature gives the transmitter greater adaptability to variable-data collection systems.

Fixed and Variable Data

Information punched in a card usually identifies fixed characteristics of a particular item. Variable data related to this item may be represented in some form other than machine-punched information on the card. In some cases, the time or location of transmission of the fixed identification data may, in itself, indicate the variation in status of an item without the need for actual transmission of variable information. In other cases, variable data may be transmitted from a source external to the card. For example, an auto-stop character may be punched in a card at the end of a fixed data field. After transmission of the fixed identification information the card will be stopped, and related variable data may be transmitted manually, from an external keyboard, or automatically from an external tape.

In many data systems, it is required to manually record variable data right on the card, at the source of data collection.[3] The port-a-punch method of manually recording variable information was described in Part I of this article. Since the Punched Card Transmitter 11890 is now capable of sensing pencil mark information, it permits a simpler technique for inserting variable data.

Recording Techniques

Any soft lead can be used for marking cards to be sensed by the transmitter, but an electro-sensitive lead which is commercially available for standard mechanical pencils is recommended. The data may be marked in a variety of configurations.

The second model of the transmitter was designed to sense information recorded in the configurations shown in Figures 2 and 3. In this system, information is marked in the Hollerith code, the pencil

marks having the effect of punched holes on the electronic circuitry. Cards are printed to clearly show the locations for inserting pencil marks.

In Figure 2, the marking of numeric data is illustrated. Any number from 0 to

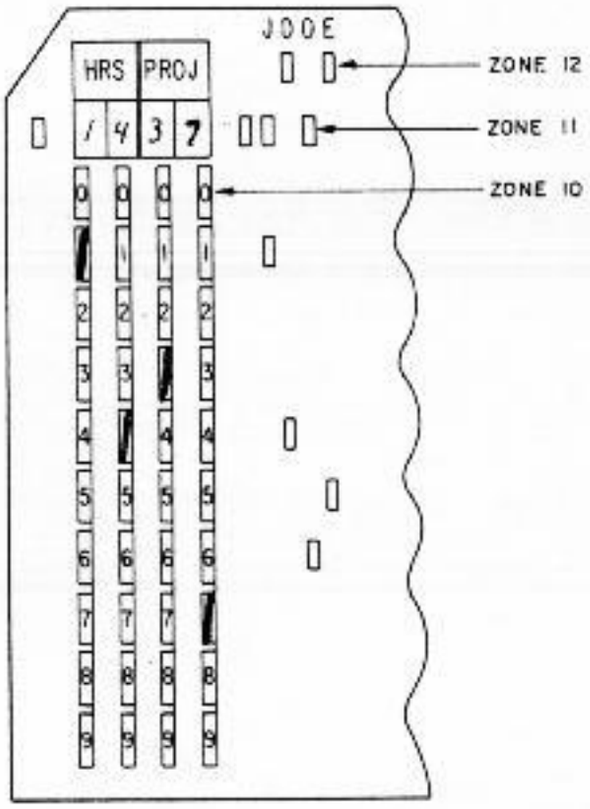


Figure 2. Punched Card with Numeric Pencil Mark Insertions to show J Doe worked 14 hours on Project 37.

9 may be marked in a column by filling in the box in which the number is printed.

Marking a letter in Hollerith code requires that two boxes in a column be filled in. Figure 3 illustrates how cards are printed to permit marking letters without any knowledge of the Hollerith code. Columns are divided into two sections, the top three boxes of each column are separated from the lower nine boxes of the column. Letters are printed in vertical groups of 3 in the lower section. To mark a letter in a column, the box next to the printed letter should be filled. In addition, one of the three boxes in the upper section of each column is filled. Either the top, middle, or bottom of the three boxes is filled depending on whether the letter is printed at the top, middle or bottom of the vertical group of 3 letters in the lower section.

In most data processing applications, the variable data is numeric even though the fixed punched data is both alpha and numeric. Therefore, in most cases the simple single-mark per column method shown in Figure 2 would be adequate.

In Figure 2, it can be seen that a punched hole in Zone 11 precedes the mark sense field, and a similar hole follows this field as the card is moved from right to left. The first hole causes the electronic circuitry to enter a mark-sense mode of operation. In this mode, the circuitry allows two columns for a mark to be sensed before transmitting the character. This feature permits more tolerance in the location of the mark, and therefore, makes mark insertion easier. Furthermore, if no mark is sensed within the two-column spaces in the mark sense field, an alarm signal is generated and the card is stopped. This feature protects against loss of data as a result of an improperly marked card. The second Zone 11 hole which follows the mark-sense field, returns the circuitry to the original punched-hole mode in which characters are recorded in every column, and blank columns are interpreted as "space" signals.

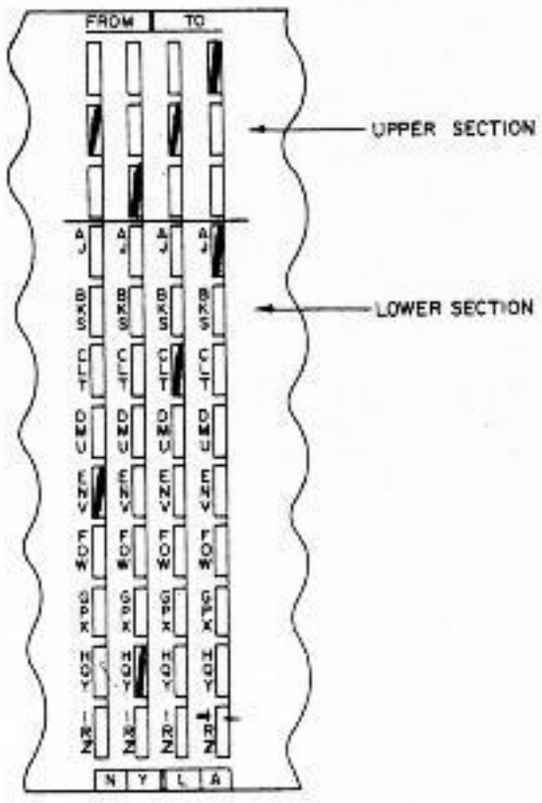


Figure 3. Printing Design for Marking Letters on a Punched Card to indicate from N. Y. to L. A.

Card Design Configurations

The Punched Card Transmitter can be designed to sense configurations other than those shown in Figures 2 and 3. The configuration for any system depends on the specific requirements of that system. For example, the configuration, shown in Figure 3, permits insertion of 38 alpha/numeric mark-sense characters per card. If a system should be limited to alphanumeric punched insertion, and "numeric only" mark-sense insertions (which require only one mark per column), insertions could be made in every column of the card. This means a maximum of 78 mark-sense characters per card in addition to the two Zone 11 control holes. Furthermore, full protection of the mark area can be obtained since "numeric only" insertions permit use of a "two-mark" alarm in addition to a "no-mark" alarm.

An alternate configuration for alphanumeric insertion is shown in Figure 4. One character may be marked in every four-column field by filling in, with pencil, the box in which the desired character is printed. This system permits the ease of a single mark insertion for a letter as well as for a number, and also permits full mark protection by use of "no-mark" and "two-mark" alarms. However, this system allows a maximum of only 20 mark-sense characters per card, if as shown, the full range of letters A-Z and numbers 0-9 are to be permitted as possible insertions for each character.

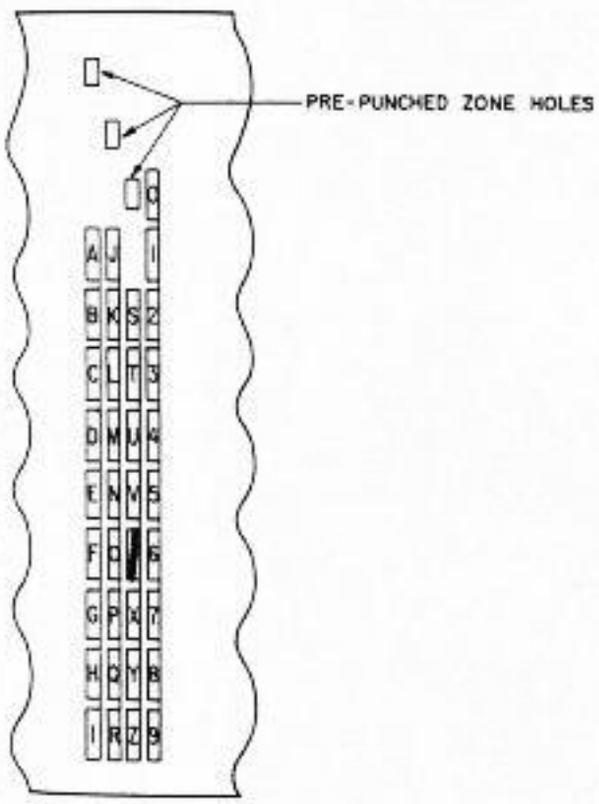


Figure 4. Printing Design for Marking a Letter or a Number by means of a single Mark (The letter "W" is marked)

Combination Cards

When mark-sense variable information is inserted on a pre-punched card, the resulting card is similar to a printed Western Union Data Card.[3] They differ, however, in that both control information and fixed identification data are represented by Hollerith-coded punched holes instead of conductive ink. As in the case of a W.U. Data Card, the control information can automatically select the format and destination of the transmitted variable and fixed data fields.

Cards containing the control and fixed punched information can be readily duplicated at speeds in the 100 card-per-minute range, at low cost, by commercially available card reproducing equipment. These cards may then be distributed for pencil-mark insertion of variable data.

Applications

Combination cards containing both punched-hole and pencil-mark information can be used in systems which require the variable data to be in a fixed format or related to fixed information. In these cases, identical copies of a master card may be reproduced at high speed and distributed for mark-sense insertions.

In addition, combination cards give processing systems the added flexibility of data insertions by field personnel on sequenced cards. Since one of the standard output forms of data processing equipment is the punched card, variable data may be inserted on cards which are the output of some previous stage of information processing. Some examples of this type of application are:

Sales Customer identification data is punched on cards in fixed format and distributed to the salesman

who marks only the variable quantity or product type ordered on each card. He returns the cards to his home office where the information is transmitted from a Punched Card Transmitter to a centralized warehouse for inventory and shipping processing.

Payroll Each employee's identification number, work group code, and wage rate is stored on cards or tape at different group locations. Each week, tape to card, or card duplicating equipment punches out individual cards with this information, at high speed. The cards are distributed to each employee who inserts only the variable "time-worked" information on his card. The marked cards are collected, and read by a Transmitter 11890 at each group location. The information is transmitted from all groups to a computer center for payroll processing.

Meter Reading A utility company representative visits each home in his district to read meters and mark his readings, of the number of kilowatt hours of electricity or cubic feet of gas, on punched cards which identify each home owner. The cards are returned to the district office and the information is transmitted from a Punched Card Transmitter to a processing center for billing procedures.

Special Features

In each of the above cases where the Punched Card Transmitter is used, the transmitted information may be recorded at the receiving station on tape, hard copy, or punched cards.

Since the output of the transmitter is compatible with either the Model 28 5-level teleprinter equipment, or the new Model 35 ASCII code teleprinter equipment, effective use may be made of stunt-box switching in transmitting information over telegraph lines. Finally, although the present transmitter operates at speeds up to 100 words per minute, the possibility of operation at speeds up to 1,000 words per minute is being investigated.

* * * *

References

1. New Punched Card Transmitter for Data Communication Systems, Part I—General Description and Applications, N. L. Feld; Western Union TECHNICAL REVIEW Vol. 18, No. 4, October 1964.
2. New 8-level Teleprinters and ASR Sets, F. W. Smith; Western Union TECHNICAL REVIEW, Vol. 19, No. 2, April 1965.
3. Data Card Transmitter P. F. Recca; Western Union TECHNICAL REVIEW, Vol. 17, No. 1, January 1963.

Biographical sketch of the author appeared in the October 1964 issue.

F. Betron (left) and R. Duswalt (right) discuss a logic design, used in the Punched Card Equipment, with the author, Newton Feld (center)

From the
Editor's Desk

on our

18th Anniversary

As Western Union grows and our engineering developments are implemented in Information Systems and Services, I wish to thank our engineers for their contribution to our success. These developments have been documented in out patents and the articles published over the past eighteen years in the Western Union TECHNICAL REVIEW.

Ours is a Growth Company

Our engineering capability to invent or design, install and maintain our services has been a fruitful one. Western Union engineers and authors have shared this capability with our readers in documenting our growth in this technical publication.

The area of paramount interest to our Company and most possible for future growth is computer-oriented communications coupled with our present public message services. I trust our engineers will continue to develop in these areas and I look forward to documenting their progress in future issues of our growth publication, the Western Union TECHNICAL REVIEW.

Mary C. Killilea

R. Steeneck, Engineer, Data Systems Div.—Information Systems & Services Dep

EDAC

Error Control

on a

Global

High Frequency Radio Circuit

While high frequency radio circuits can reach out into remote spots on the globe, they leave much to be desired in their ability to furnish reliable and accurate channels of communication. Instability of the ionosphere often introduces signal jitter, noise, and complete fading of signals all of which raise the error rate so high, as to render these circuits useless for communication purposes. In general North-South circuits, except perhaps in some polar regions, are more stable than those running East-West. Tropical circuits are the least stable of any.

Editorial Note:

Since submission of this manuscript the author wishes to add:

The very significant results obtained by conducting tests, on one of the most difficult HF Radio circuits in the world, indicate that deviating from what are considered standard techniques has made for unusual success in the EDAC approach to the problem of Automatic Error Control.

ARQ Systems

A solution to the problem of error control was first attempted in the development of the ARQ system. In this system the 5-bit teleprinter code was first converted to a 7-unit code, in which each character contained a fixed ratio of 3 marking and 2 spacing bits. When a received character did not contain the proper ratio of marking and spacing bits, it was recognized as an error. The traffic flow in both directions had to be stopped while retransmission procedures functioned to correct the errored information.

Many versions of the ARQ system were developed, but all had the disadvantage of requiring code conversion and stopping traffic in both directions whenever any error was detected.

Although the fixed-ratio code used for error detection in ARQ systems resulted in considerable improvement in the operation of HF radio circuits, there were times, when errors could pass through the system undetected. A recent test showed the undetected errors to be as high as 17 percent.[1]

The limitation of the ARQ system prompted a new approach to the problem not centered around techniques involving fixed ratio codes. This resulted in the design of a new error detecting system called EDAC, Error Detection Automatic Correction.

This paper was presented at the First Annual I.E.E.E. Communication Convention at Boulder, Colorado on June 6, 1965.

EDAC

In the EDAC system a block of teleprinter signals, four characters in length, is used which includes 20 information bits, 5 redundant check bits, 3 control bits, and 2 synchronizing bits as shown in Figure 1.

necessary to wait for an acceptance signal at the end of each block. A simple retransmission routine follows whenever an acceptance signal fails to return and makes it impossible at the receiving terminals, to drop a block, deliver it more than once, or deliver it out of order.

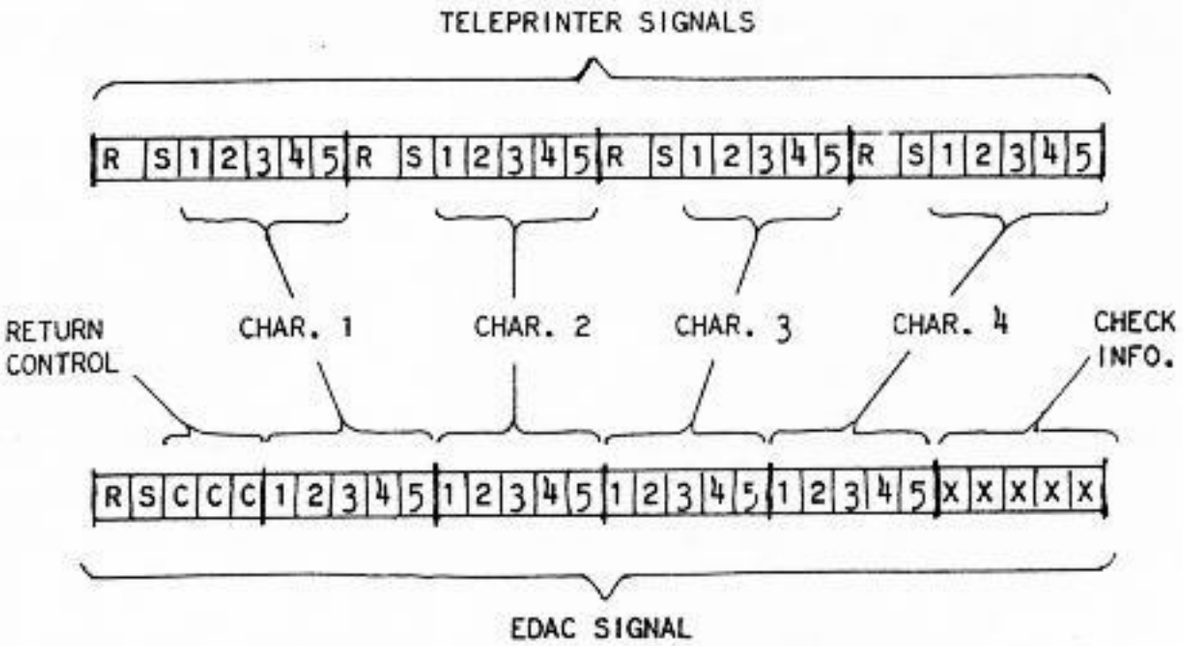


Figure 1. EDAC Block

It will be noted from Figure 1 that the length of the 4 character EDAC block is precisely that of four 7½ unit start-stop characters. Thus, the EDAC character and bit rates are exactly equal to the 7½ unit start-stop teleprinter rates.

EDAC operates on a duplex basis, handling error-protected traffic simultaneously in both directions. EDAC functions with only one 3-bit return control signal, superimposed on traffic in each direction. The return control signal has only one function and that is to acknowledge acceptance of each block of traffic after it has been transmitted and received without error. Each block is transmited from storage and must be acknowledged as having been accepted at the receiving end before a new block can be placed in storage. The return control signal provides this acknowledgement.[2]

By using two-block storage it is not

Check Information

Figure 2 shows the common method employed for the generation of parity bits normally used to protect a block of information. Parity bits, however, do not provide as much protection against undetected errors as five bits are capable of providing. This is due to the fact that a parity bit is effective only when bit failures alter the parity sum by an odd number of bits.

Considerable improvement in error protection can be obtained by connecting together flip flops used to generate each parity bit as shown in Figure 3.

The Flip Flops shown in Figure 3 form a Binary Adder which does not merely count the bits to be protected but produces a binary sum in which each bit level is given a different numerical weight. The #1 bit level entering the #1 counter

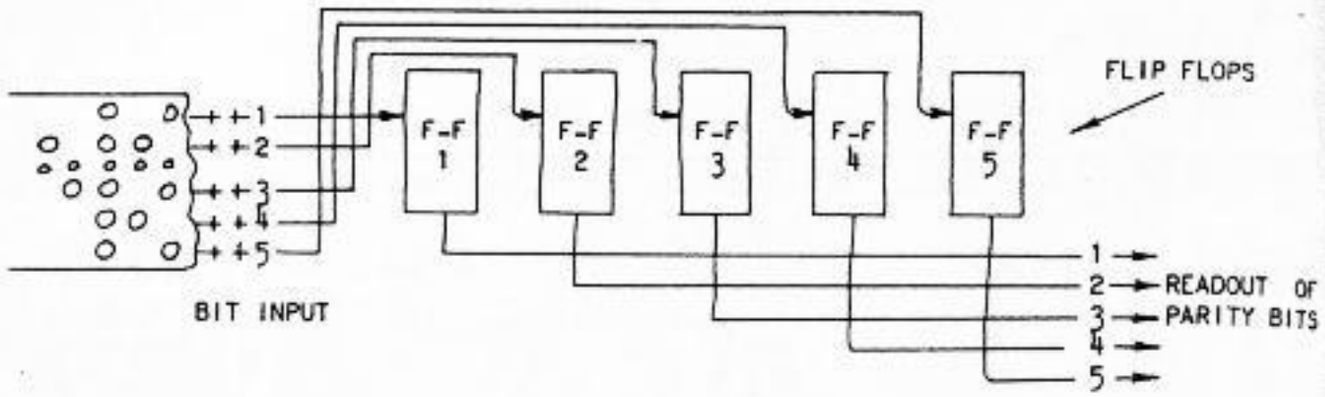


Figure 2. Generation of Parity Check Bits

can generate check sums that affect all five check bits. It is quite obvious that these five check bits give more than the odd-even protection of a single parity bit. It is also obvious that this protection deteriorates since each consecutive code level involves the generation of fewer protection bits. When the #5 code level is reached, it generates its protection only in the #5 bit and this receives only simple odd-even parity protection.

This lowering of protection, however, can be overcome by a simple change in the binary counter. By feeding back the output of the fifth stage of the counter into the first stage of the counter, a new type counter shown in Figure 4, is formed, which might best be described as a binary ring counter.

The input and output circuits shown in Figure 4 are perfectly symmetrical with respect to each other. Each bit level has

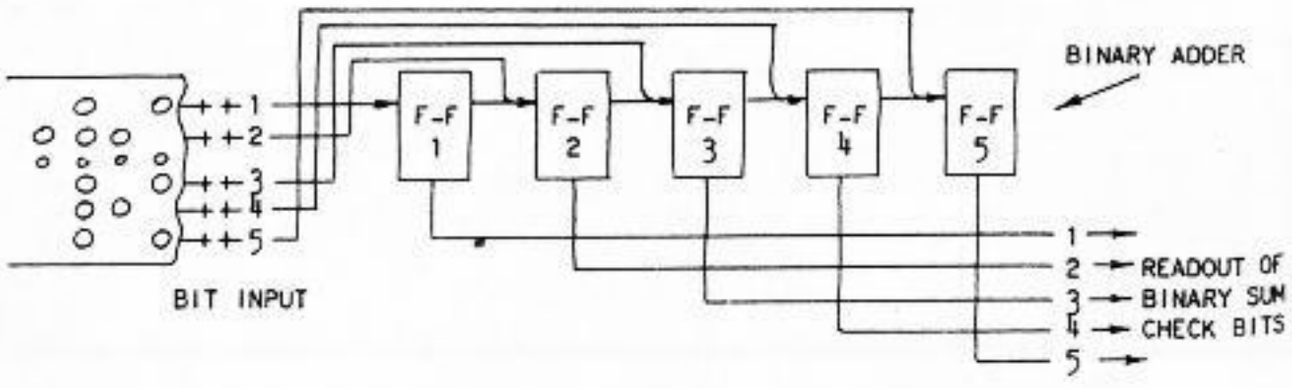


Figure 3. Generation of Weighted Binary Sum Check Bits

the use of all five check bits to protect its information and no bit level has any advantage over any other level. The protection thus generated is far greater than parity alone can provide, and it is logical to expect this to be reflected in test results.

Measurements of the circuit quickly established the actual round trip time to be 450 milliseconds. More than half of this was consumed in the 3,000-mile wire circuit. Some consideration was given to lowering this figure by rerouting the wire facilities. However, this was not done

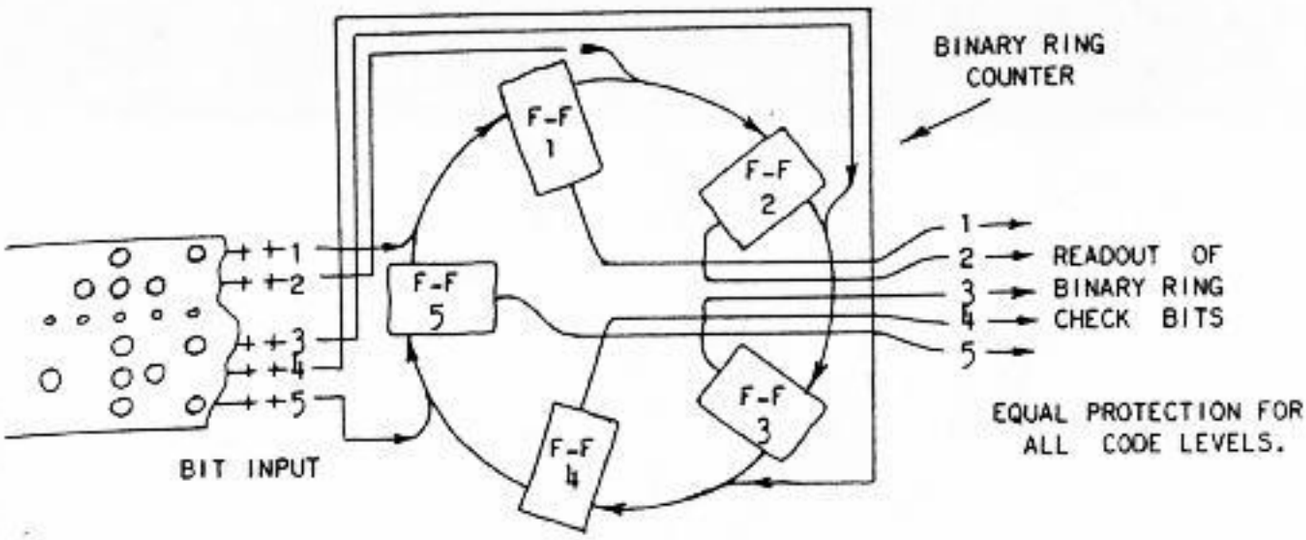


Figure 4. Generation of Binary Ring Counter Check Bits

EDAC Tests

Early in 1964 EDAC models were first tested on a truly global circuit. The complete circuit included 3,000 miles of land line and two tropical High Frequency radio circuits patched in series. Each radio circuit was 4,500 miles long.

Before starting the tests, some preliminary measurements were made to determine the propagation times involved in a circuit of this length. The EDAC equipment can tolerate a total round trip propagation time of 266 milliseconds, when operating at a speed of 100 words per minute. At 60 words per minute this round trip tolerance is increased to 435 milliseconds.

since the best routing available would not allow operation at 100 words-per-minute speed.

Since the error rate on point-to-point domestic wire circuits of this length would be, on the average, only one or two bursts per day, it was decided to install the EDAC equipment at each end of the 9,000 mile two-hop tropical HF Radio circuit. The round trip propagation time of this circuit was 220 milliseconds which allowed tests to be conducted at both 60- and 100 words per minute.

The error rate of this radio link was high even under the best of operating conditions. To quote an average error rate, however, would be meaningless for

communications analysis, because of the wide variations that occurred.

Observations of traffic indicated that errors ranged in frequency from about one per minute to more than 50 per minute. The number of bits destroyed in an error burst varied from a single bit to more than ten thousand bits.

The behavior of this circuit can perhaps best be illustrated by the graph shown in Figure 5. In this graph the number of retransmissions called for by EDAC during each half hour of the test have been plotted against time of day at the mid-point of the radio circuit. From Figure 5 it can be seen that the error rate of this circuit was far from uniform. The behavior of the circuit varied throughout the day and night. The highest error rate seemed to be during the early morning hours. The graph was plotted from data taken during tests made at a speed of 100 words per minute. However, tests at sixty words per minute produced somewhat similar variations but fewer retransmissions were required.

During the test, two teleprinter channels in the same radio circuit were used. One was equipped with EDAC, and the other was not. Figure 6 shows a sample of traffic received by the channel not equipped with EDAC. The time this sample was taken is indicated by the arrow shown in Figure 5.

Although the point of sampling does not represent the worst condition of transmission, the error rate is very high. A quick analysis of the copy shows that both gains and losses of bits are involved in unpredictable patterns. Closer observation however, reveals that there are many places in the copy where good runs of at least four consecutive characters are present. These are points at which EDAC can extract and deliver error-free copy.

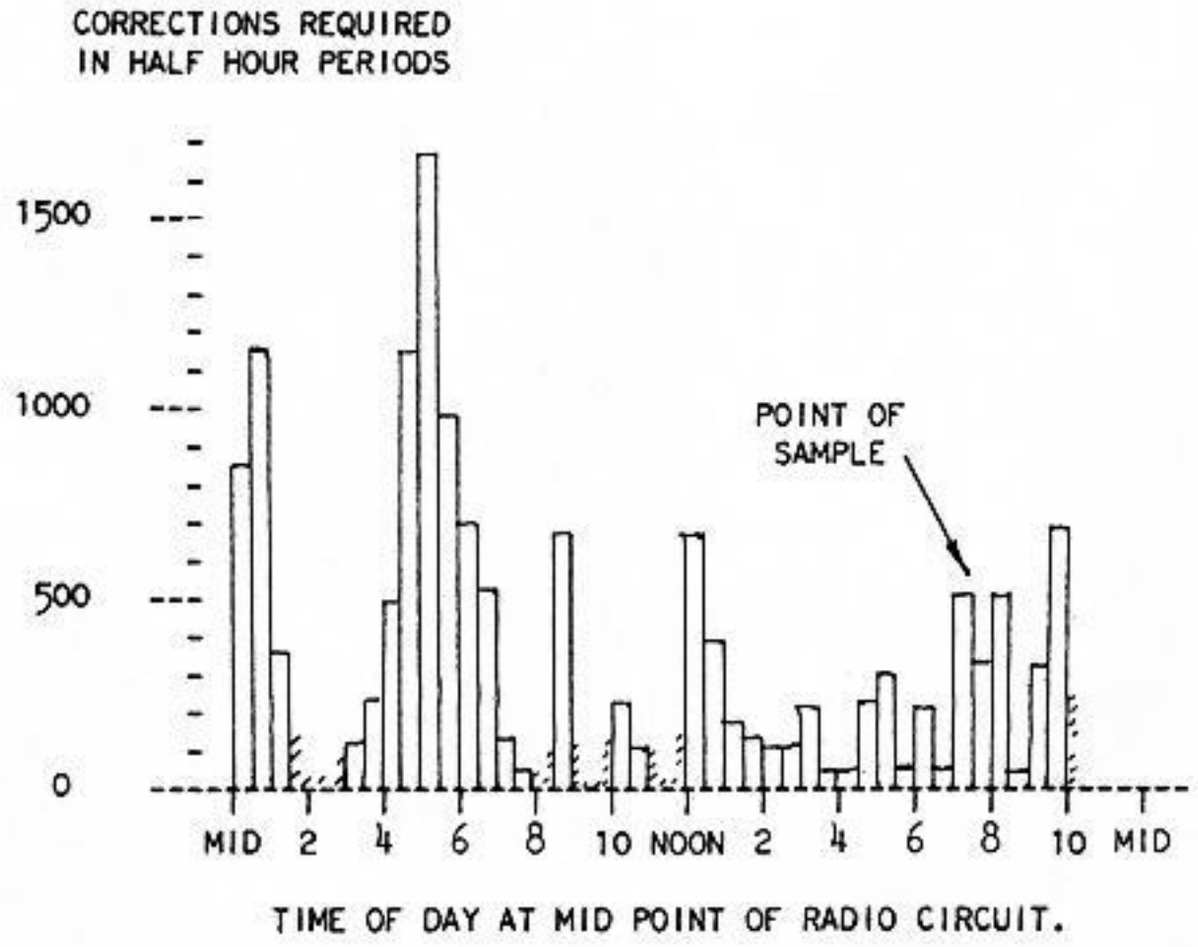


Figure 5. Corrections Required on Radio Channel

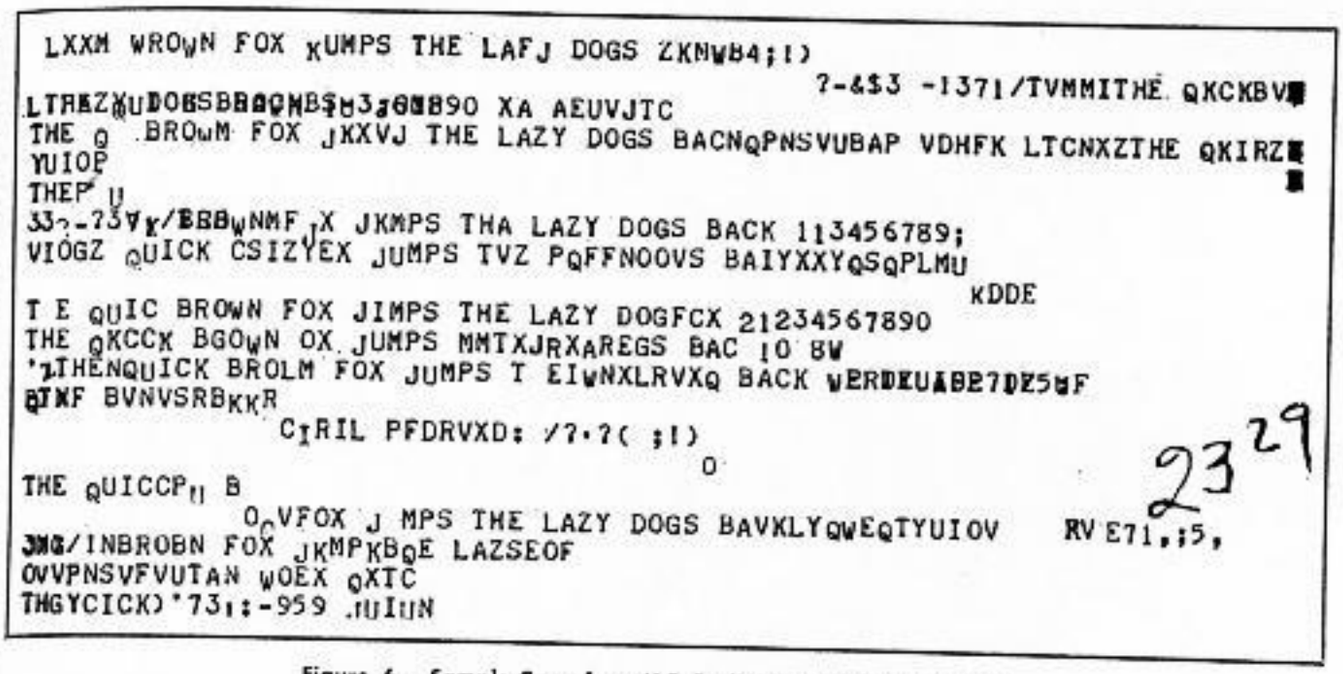


Figure 6. Sample Copy from H.F. Radio Channel without EDAC

Transmission of Short Blocks

The use of short blocks of error protected information is one of the basic secrets of EDAC's ability to successfully handle traffic under the conditions illustrated in Figure 6. If the EDAC block length were increased to include a full line of copy, it could not function under the conditions shown, because there are no error-free lines in the received copy.

EDAC's ability to function successfully, is shown in Figure 7. Here a sample of error-free copy, delivered by the EDAC channel is shown after transmission under the same conditions experienced in Figure 6.

As may be seen by observing the local time marked on the copy both samples were received at the same time. It will be noted that only two errors are shown on the EDAC sample each involving the loss of one bit. These are not undetected transmission errors but are due to trouble in the input tape reader at the sending end of the circuit. Even in the poorest of parity systems it is impossible for an error involving the loss of a single bit to go undetected. The single bit errors shown here developed outside the EDAC system and passed into EDAC as valid information.

```
        TAPE READER ERRORS

RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY 4150
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXY7    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
(V) RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY    23 29
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
RYRYRY    ABCDEFG    HIJKLMN    OPQRST    UVWXYZ    RYRYRY
```

Figure 7. Sample Error-Free Copy from a Channel Equipped With EDAC

Protective Redundancy

EDAC does not use parity, but develops its protective redundancy as previously explained by using a process of binary additions that provides more protection equally to all code levels than parity alone can provide.

EDAC redundancy also provides almost fool-proof protection against errors that involve consistent bit losses or consistent bit gains. This is not true, however, when both the loss and gain of bits are involved. There are patterns of gains and losses that compensate each other, and this is true of any system of redundancy thus far devised.

Fortunately, however, these compensating errors do not occur often in EDAC operation. Some consideration has been given to their elimination through increase of redundancy but it is not considered economical, since only a few errors per day would be involved. Some simple changes can, and will be made however, to further reduce the few undetected errors, without adding more redundancy.

Before the tests were started, some apprehension was felt that in operating at a speed of 100 words per minute, the higher error rates involved might result in the movement of less traffic than could be handled with 60 words per minute operation. This was not true, as can be seen from the graph shown in Figure 8.

Figure 8 shows the effective output speed of the 100 word per minute tests during the period shown in Figure 5. It will be noted, that the output seldom fell below 60 words per minute. The design of the EDAC block being such that its characters rate and bit rate were the same as that of 100 word per minute teleprinter signals, enabled the circuit to approach 100 percent of its capacity during periods when an insignificant number of errors were present. This is quite apparent during some of the half hour periods shown in Figure 8. The use of short blocks that not only quickly detected errors but also quickly corrected them, provided effective error control without drastically reducing the operating speed of the circuit. The average output for the day's run shown in Figure 8 was 82 words per minute.

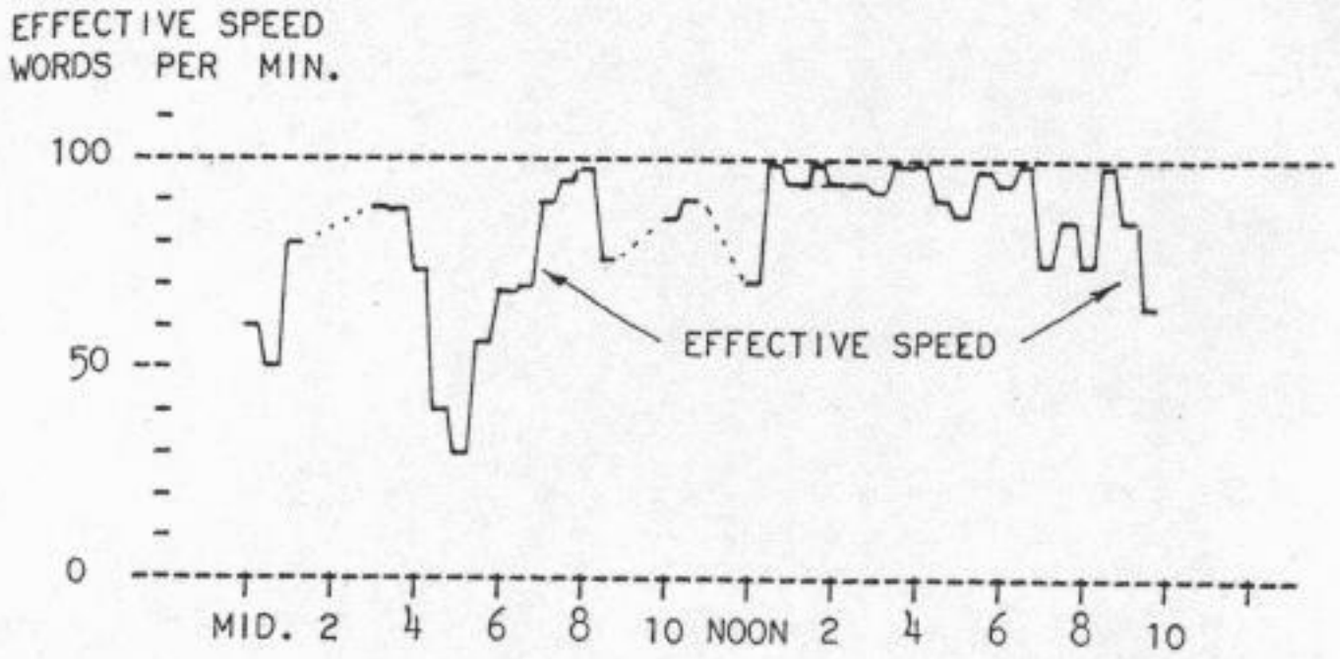


Figure 8. Effective speed with EDAC in Circuit

Conclusion

The testing period embraced a variety of operating conditions, and proved conclusively that the EDAC approach using small blocks of protected information without using parity techniques did provide effective error control even under severe conditions of fading and noise.

The tests also showed, that it was not necessary to add excessive redundancy, or reduce the rate of transmission, in order to obtain error control with a satisfactory output of useful traffic.

Although the test period itself was of short duration, the equipment was not removed after the tests were concluded. The units are still in service and have been successfully handling live data traffic for almost a year. There are many periods when this channel is the only one able to carry information.

* * * *

References

1. North Atlantic Teletype Engineering Study, Final report, Volume IV (ITT Communication Systems Inc., Paramus, New Jersey).
2. Robert Steeneck, The EDAC Solution to the Problems of Error Control in Telecommunications, presented at Scott—St. Louis Chapter of A.F.C.E.A. Nov. 1963 (Western Union, New York).

Mr. Robert Steeneck, Data Systems Engineer in the Information Systems and Services Department, has been responsible for the development of error detection and correction devices for data transmission systems.

He received his M.E. degree from Stevens Institute of Technology in 1926 after which he joined Western Union as an apparatus engineer. He designed components for the Radar Contact Trainer, one of the first predecessors of analog computers. He later concentrated on the development of automatic switching systems.

Mr. Steeneck received the F.E. d'Humy Award for his achievements in electro-mechanical developments. He holds 22 patents and has written many articles for the Western Union TECHNICAL REVIEW.