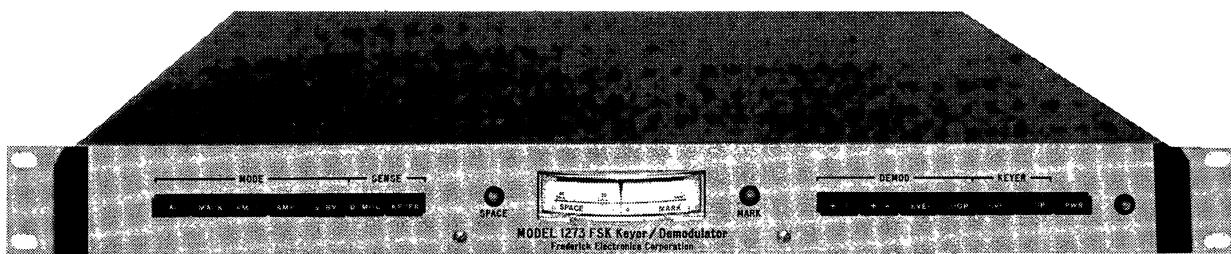


PLANTRONICS

Frederick Electronics

MODEL 1273 FSK KEYER/DEMODULATOR



FEATURES

May be used as a half or full duplex device, or an independent Keyer or Demodulator.

Highly stable and accurate tone keyer output.

Demodulator has active filter input for improved noise rejection.

Low power consumption.

GENERAL

The Model 1273 provides a full or half duplex connection between a digital data device and a communications channel. The unit is intended primarily to interface a data terminal to an HF radio channel.

APPLICATIONS

Outstanding performance is realized in the demodulator section, for signals derived from the HF radio band, due to independent detection of the mark and space tones. "AM" detection of this redundant data has been acknowledged, by both amateur and professional RTTY operators, to be superior to "FM" detection techniques. Wide dynamic range is obtained without the use of limiter circuits. This makes possible good reception of signals with low signal-to-noise ratios and offsets the normal deleterious effects of frequency selective fading which

APPLICATIONS (CONT)

normally plagues HF radio reception. FEC has a long and highly successful history with design of equipment of this nature.

The tone keyer section has also been designed with the requirements of an HF radio circuit in mind. This section features excellent frequency stability and accuracy, spectral purity, and close output level control. All are highly desirable for TTY, FSK operation on HF paths.

The Model 1273 modem may be used in any situation where conversion of digital data to FSK signals and the inverse are required. This includes long distance hard wire circuits and storage or retrieval of audio data from magnetic tapes.

The equivalent of quad-diversity performance is realized by connecting two separate antenna/receiver/demodulator set-ups together. This is easily accomplished by connecting three wires from one Model 1273 to the other. No further equipment, such as a diversity combiner, is required.

DESIGN

The Model 1273 uses all solid-state modular circuitry, packaged on plug-in printed circuit boards. Access to the plug-in modules is provided by an easily removable top cover. The unit is suitable for fixed or slide-mounting in a standard 19" equipment rack.

SPECIFICATIONS

ELECTRICAL

TONE KEYER SECTION

KEYING RATE - Up to 1200 baud.

INPUT SIGNALS/CIRCUITS - Selectable for:
Low level, MIL-STD-188C or EIA-STD-RS-232-C;
High level, polar current loop of 20 ma at
up to ± 65 vdc or neutral 20/60 ma loop at
up to 130 vdc.

OUTPUT CIRCUITS - Isolated and balanced,
600 ohms or 10K ohms, isolated and balanced.

OUTPUT SIGNALS - (Determined by plug-in
crystals.) Audio tones between 400 and
3500 Hz and employing shifts of 60 to 2000
Hz. Output level is adjustable from -45
dbm to +4 dbm. Variations between carriers
at 0 dbm output less than $\pm .25$ dbm. Fre-
quency stability is better than $\pm .5$ Hz.
Waveform is phase coherent within 1% and
contains less than 2% total harmonic dis-
tortion.

DEMODULATOR SECTION

KEYING RATE - Up to 1200 baud, but depen-
dent upon tone frequencies and shift para-
meters.

INPUT CIRCUIT - Isolated and balanced, 600
ohms or 10K ohms, isolated and balanced.

INPUT SIGNALS - Audio tones between 400
and 3500 Hz at a nominal 0 dbm. The dynamic
range is -50 dbm to +12 dbm. However sig-
nals above 0 dbm will be limited. Shifts
of 170 Hz to 2000 Hz may be accommodated,
but are dependent upon keying speeds. Also
accepts ON/OFF keyed CW.

OUTPUT SIGNALS/CIRCUITS - Standard output
signals which are compatable with EIA-STD-
232-C or MIL-STD-188C. TTY current loop
keyers are optional plug-in assemblies
which may be used to key polar or neutral
loops of up to 100 ma at 130 vdc. Low im-
pedance diversity connections are also pro-
vided. Bandpass filter outputs are avail-
able at the rear panel to drive tuning aids
and display devices.

PHYSICAL

DIMENSIONS - 19 inches wide (48.3 cm), 17
inches deep (43.2 cm), 1-3/4 inches high
(4.4 cm).

MOUNTING - Mounts directly into a 19-inch
rack or slide mounting.

FINISH - All front panel lettering is en-
graved and filled; paint is light gray
semigloss, chassis is clear anodized alu-
minum.

WEIGHT - Approximately 7.5 pounds (3.4 kg).

SERVICING - By removal of top cover.

POWER REQUIREMENTS - 115/230 vac, 50-400 Hz
at approximately 10 watts.

ENVIRONMENTAL - Operating temperature range
0° to 50° C; storage -40° to 80° C ambient.
Relative humidity - 0 to 95% (non-condensing).
Atmospheric pressure - sea-level to 15,000
feet (4.57 km).

INSTRUCTION MANUAL

MODEL 1273

FSK KEYER/DEMODULATOR

July 1983

TMC19100

PROPRIETARY INFORMATION

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MANUAL ERRATA SHEET

EQUIP MODEL NO: 1273		MANUAL PART NO: TMC19100	MANUAL DATE: JUL 83										
REFERENCE													
Figure 7-2 Parts List		List of Material Item 47 - Change CD4011A to CD4011BE Item 48 - Change CD4023A to CD4023BE											
Figure 7-9		On Parts List Delete Item 16 and 17 and replace with meter/scale 1136HBC/WB0829 FEC # 524175 on both dwgs.											
-----		AB -----	1983										
Figure 7-9 Swbd Assy		List of Material: Delete Items 16 and 18. Change Item 17 to read:											
		<table> <thead> <tr> <th>ITEM</th> <th>RQD</th> <th>PIN</th> <th>DESCRIPTION</th> <th>MFG</th> </tr> </thead> <tbody> <tr> <td>17</td> <td>1</td> <td>B0829</td> <td>METER/SCALE</td> <td>FEC</td> </tr> </tbody> </table>	ITEM	RQD	PIN	DESCRIPTION	MFG	17	1	B0829	METER/SCALE	FEC	
ITEM	RQD	PIN	DESCRIPTION	MFG									
17	1	B0829	METER/SCALE	FEC									
Figure 7-4 MK-SP BP Filter Bd Assy		List of Material: Item 1 - Change P/N from N01158B to N01158C											
Figure 7-6 Parts List		Item 28 - Change CAT P/N from 602636 to 602180											
--- ECN 6421A/6573/6929 --- SEP 85 -----		<i>HGS</i>											

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NOTE

Operating frequencies quoted in the text and tables of this manual are TYPICAL, used for purposes of explanation and functional description only.

The actual operating frequencies with which individual units are equipped are shown in Appendix A at the rear of this manual.

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SECTION I

INTRODUCTION

1.1 PURPOSE OF EQUIPMENT

The Model 1273 FSK Keyer/Demodulator is a dual function equipment designed to provide demodulation of frequency shift keying (FSK) signals and conversion of high level neutral/polar teletype or EIA input data to FSK output signals. A front view of the Model 1273 is shown in Figure 1-1.

The FSK Demodulator circuits of the Model 1273 accept FSK tones within the range of 400 and 3500 Hz and with keying rates between 30 to 1200 bauds. The audio tone input supplied by a communications receiver is demodulated and used to drive one or more of the following output circuits: a high level neutral or polar loop keyer, a logic level keyer capable of producing polar EIA RS-232-C logic level signals, or MIL-STD-188C logic level signals.

The FSK Keyer circuits convert conventional telegraph input data to an audio frequency shift output. Different AFSK tones can be selected by replacement of the mark-space oscillator crystals.

An active input bandpass filter and limiter circuit render the 1273 unit virtually impervious to 60 Hz hum, noise, and other out-of-band signals, allowing the unit to operate (in the limiter mode) with FSK signals below -60 dbm. The effects of frequency selective fast-fade conditions are reduced through the use of a Decision Threshold Computer (DTC) circuit. In the auto-mark-hold function, the unit can operate with input signals as low as -50 dbm before being placed into a mark-hold condition.

1.2 PHYSICAL DESCRIPTION

The Model 1273 contains the following circuit cards:

1. Tone Keyer N01343 (FEC Assembly D3095)
2. Demodulator N01483 (FEC Assembly D3739)
3. Bandpass Filter N01158 (FEC Assembly D2818) - 2 required
4. Low Pass Filter N01159 (FEC Assembly D2813)
5. Power Supply N01318 (FEC Assembly D2962)
6. High Level Keyer N01452 (FEC Assembly C3240) (Optional) - two required for polar keying applications, one required for neutral keying.
7. Bandpass Filter N01991 (FEC Assembly C3916) (Optional) Replacement for Bandpass Filter D2818. Refer to Appendix A.

The circuits are packaged in an aluminum chassis designed for mounting in a standard 19-inch equipment rack. The required vertical rack space is 1-3/4 inches.

All operator controls required for normal operation of the unit are mounted on the front panel. All input/output connections are made via rear apron terminal strips and a multipin MOLEX connector.

The mark channel and space channel Bandpass Filters and the Low Pass Filter are plug mounted on the Demodulator. The filter circuits determine the frequency shift and baud rate for the FSK Demodulator. These cards are selected at the factory to match customer requirements. Filters are available from Frederick Electronics for any frequency shift and baud rate within the range of the equipment.

1.3 SPECIFICATIONS

Specifications for the Model 1273 FSK Keyer/Demodulator are outlined in Table 1-1.

Table 1-1. Specifications, Model 1273

DEMODULATOR

Input Impedance. Balanced 600 Ω or 10K Ω (selectable on the PC card).

Input AFSK Tone. Center frequency between 400 and 3500 Hz.

Input Sensitivity In Limiter Mode Below -60 dbm.

Operating Rate Between 30 and 1200 baud.

Frequency Shift. Up to 1000 Hz.

Mark-Space Channel Bandwidth. Between 85 and 500 Hz.

Mark Center Frequency . . . Between 400 and 3500 Hz.

Space Center Frequency . . . Between 400 and 3500 Hz.

Outputs. EIA RS-232-C polar logic level signals.

MIL-STD-188C polar logic level signals.

Table 1-1. Specifications, Model 1273 (cont.)

DEMODULATOR (cont.)

KEYER

Polar Logic Level Circuit - Detects EIA Standard RS-232-C or MIL-STD-188C logic level signals.

NOTE

When operating with neutral loop inputs proper polarity must be observed. With neutral or polar inputs loop current must be adjusted to the specified value by an external resistance.

Output Level Adjustable up to +4 dbm.

Output Impedance Balanced. 600 ohms or 10K ohms.

GENERAL

Power Requirements Switch selectable 115 or 230 VAC
±10% 50-400 Hz.

Power Consumption. 10 watts.

Temperature Range. 0 to 50°C.

Table 1-1. Specifications, Model 1273 (cont.)

GENERAL (cont.)

Outer Dimensions	Height: 1-3/4 inches (4.4 cm) Width: 19 inches (48.3 cm) Depth: 17 inches (43.2 cm)
Weight	Approximately 7-1/2 pounds (3.4 kg)

SECTION II

INSTALLATION

2.1 UNPACKING AND INSPECTION

Open the shipping container being careful not to puncture the container with sharp objects which may damage the contents. Remove the packing and the unit(s) from the container. Inspect the unit(s) for damage. If any damage is observed as the result of shipping, file a written claim with the shipping agency and forward a copy of this claim to:

Frederick Electronics Corporation
Hayward Road, Post Office Box 502
Frederick, Maryland 21701

If repacking for storage or reshipment is anticipated, replace the packing material and retain the container for later use.

2.2 POWER REQUIREMENTS

The Model 1273 FSK Keyer/Demodulator is shipped from the factory ready to operate directly from a nominal 115 vac, 50/60 Hz power source. Power is connected by plugging the power cord into a standard 3-prong ac outlet. The input is fused prior to application to the power supply transformer.

2.3 MOUNTING

The Model 1273 is designed for mounting in a standard 19-inch equipment rack. The unit is 1-3/4 inches high and extends approximately 17 inches back into the equipment rack. The unit is secured to the equipment rack by screws inserted through the front panel mounting holes. Optional slide mounting can be incorporated on customer request.

2.4 INPUT/OUTPUT CONNECTIONS

The function of the individual pins of each connector is identified in Figure 2-1. Those connections that do not apply to a particular operating requirement should be ignored. Figures 2-2 through 2-6 show typical input/output connections for loop operation.

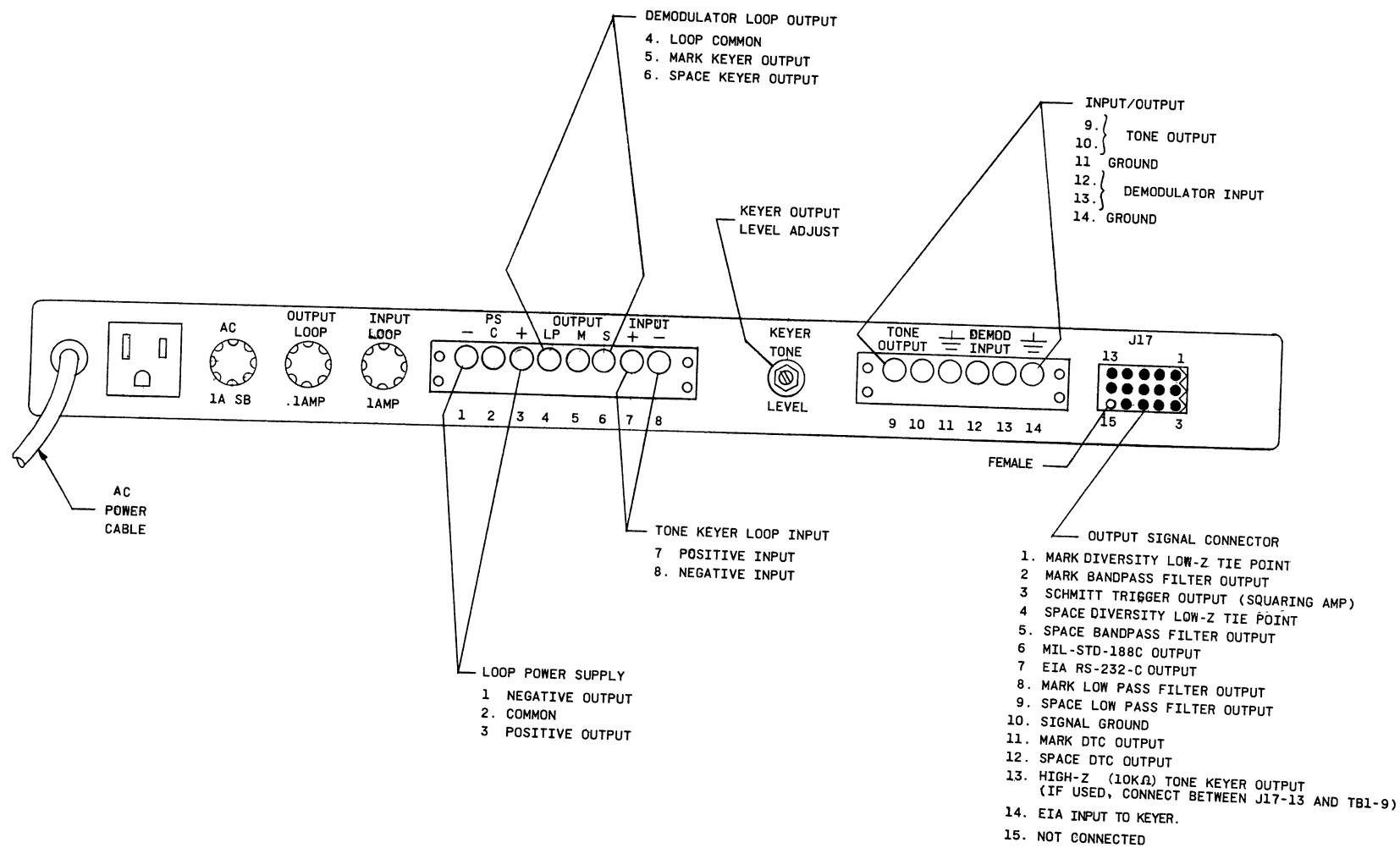


Figure 2-1. Model 1273 Input/Output Connections
C3121A

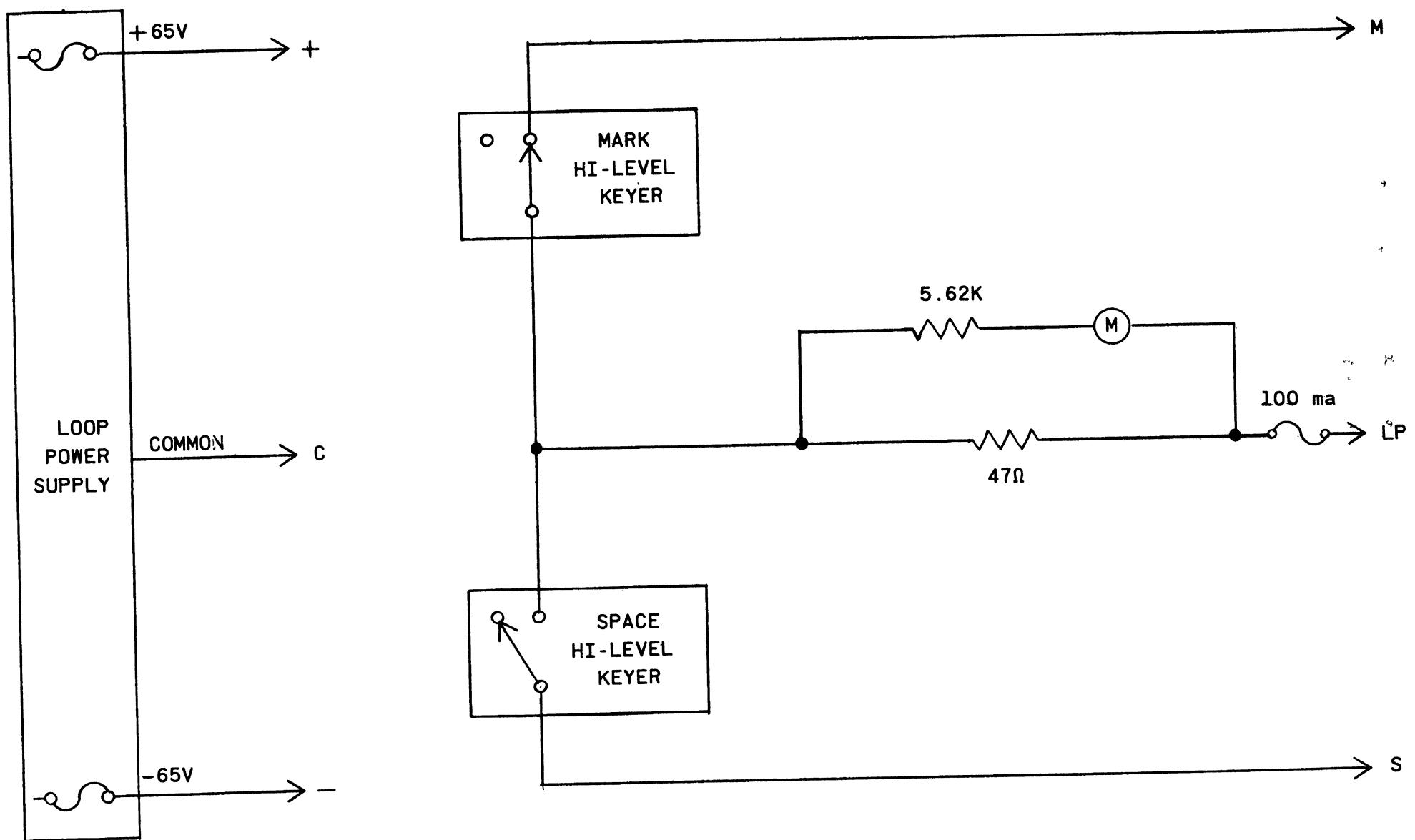


Figure 2-2. Internal Loop Connections
B2115A

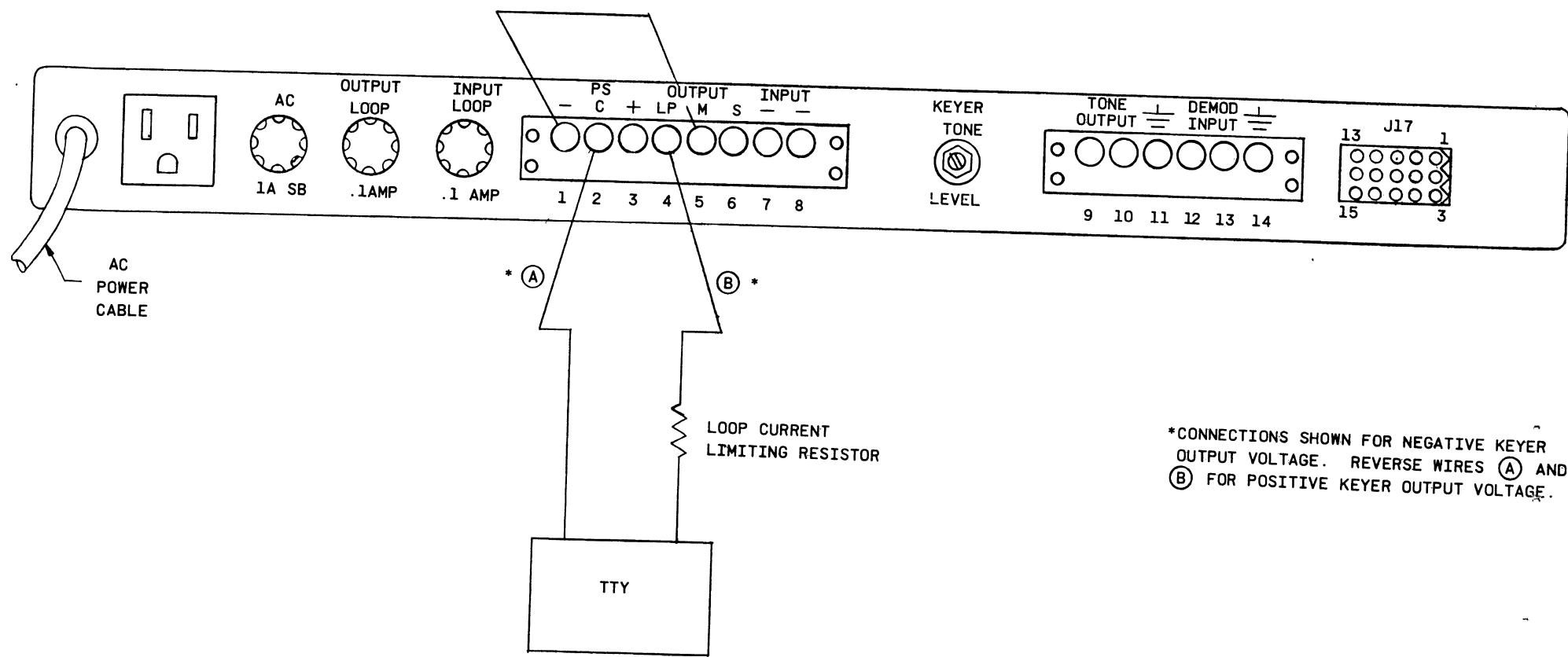


Figure 2-3. External Loop Connections, Internal Power Supply, Neutral Keying
C3120

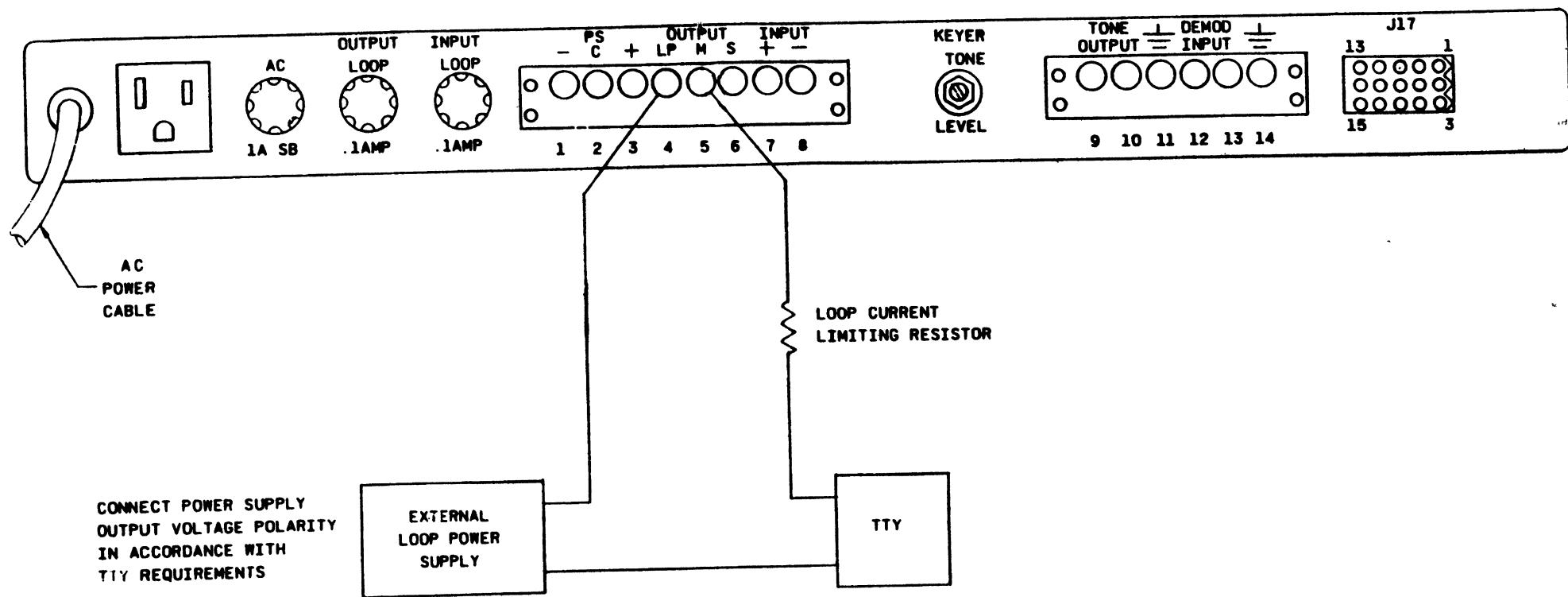


Figure 2-4. External Loop Connections, External Power Supply, Neutral Keying
C3122

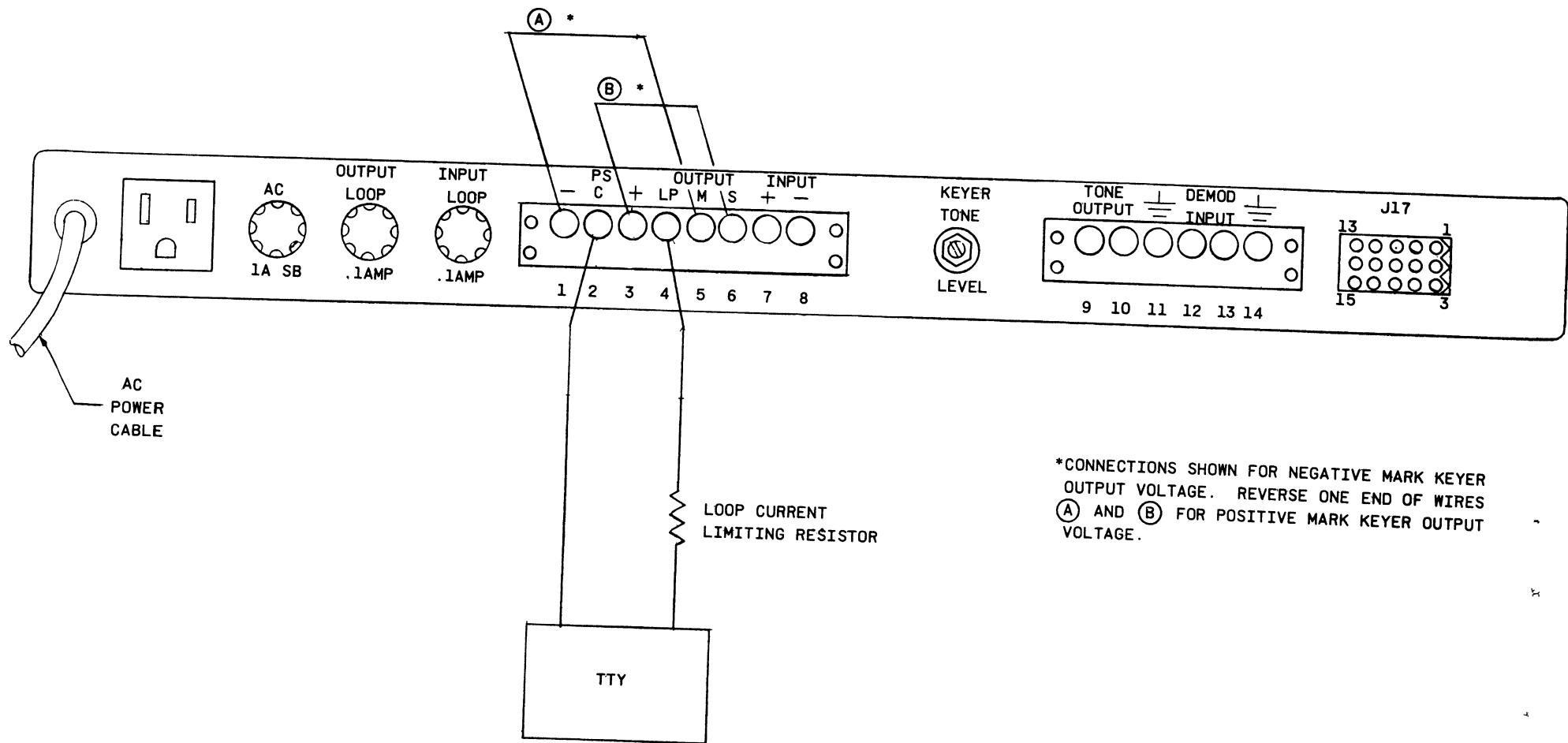


Figure 2-5. External Loop Connections, Internal Power Supply, Polar Keying
C3124

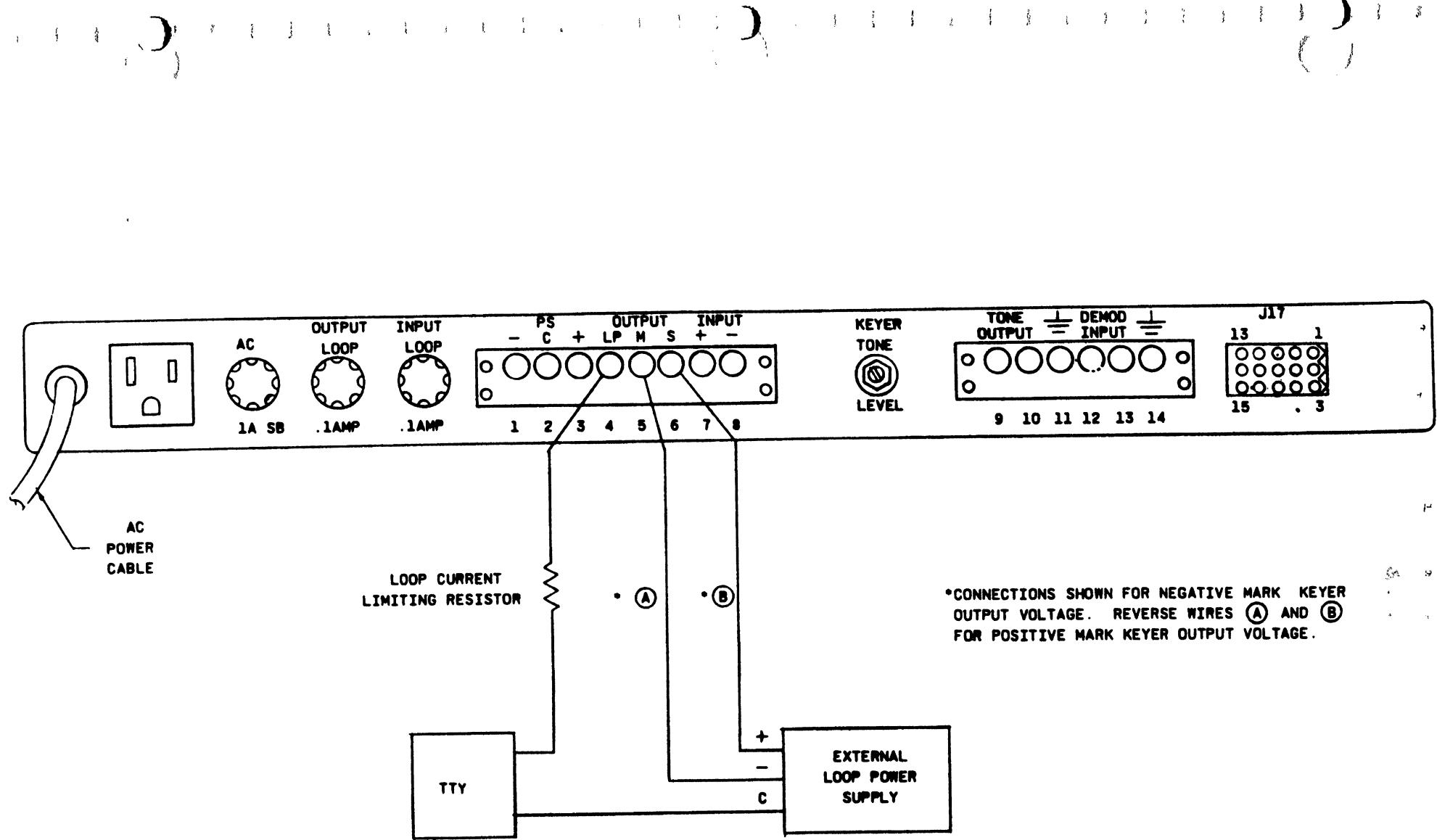


Figure 2-6. External Loop Connections, External Power Supply, Polar Keying
C3123

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SECTION III

OPERATION

3.1 GENERAL

To obtain optimum performance from the Model 1273, it is essential the operator thoroughly understand the functions of the front panel controls and indicators and how to tune the associated receiver to an FSK signal.

The following paragraphs describe the operation of each control and its optimum position for various receiving conditions. In addition, a section on receiver operation is provided.

3.2 CONTROLS AND INDICATORS

Table 3-1 lists the functions of the controls and indicators. Control and switch positions associated with the Frequency Shift Keyer operations are identified with an asterisk (*).

Table 3-1. Controls and Indicators

CONTROL/INDICATOR	REF	FUNCTION
<u>MODE SWITCHES</u>		
SPACE	S1	Disables mark channel output when switch is depressed.
MARK	S2	Disables space channel output when switch is depressed.
AMH1	S3	Commands Mark-Hold circuit to place data output in mark state when either mark or space channel (or both) has signal loss.
LIMIT	S4	In depressed position activates the limiter circuit and provides 30 db minimum of additional gain. In released position linear operation of the limiter is obtained.
STBY	S5	Places 1273 Demodulator loop in a steady mark state when switch is depressed.

Table 3-1. Controls and Indicators (cont.)

CONTROL/INDICATOR	REF	FUNCTION
<u>SENSE SWITCHES</u>		
DEMOD	S6	Reverses mark-space polarity at Demodulator output to select correct mark-space relationship.
KEYER	S7	Selects correct mark-space polarity for signal processing by Tone Keyer.
<u>DEMOD SWITCHES</u>		
++	S8	Used to tune Receiver to an FSK signal. Receiver is properly tuned when meter shows maximum deflection and minimum oscillations.
+-	S9	Indicates input signals by deflecting to the right for mark and left for space.
LEVEL	S10	Monitors level of Demodulator input signal. Normal level is 0 DBM.
LOOP	S11	Monitors current in Demodulator high level output loop.
<u>KEYER SWITCHES</u>		
LEVEL	S12	Monitors output signal level from Tone Keyer. Meter is calibrated at 0 DBM.
LOOP	S13	Monitors current in Tone Keyer high level input loop.
PWR (power)	S14	Controls power to Model 1273.
MARK Indicator	CR1	Illuminates when Demodulator detects a mark signal higher than Mark-Hold level.
SPACE Indicator	CR2	Illuminates when Demodulator detects a space signal higher than Mark-Hold level.

Table 3-1. Controls and Indicators (cont.)

CONTROL/INDICATOR	REF	FUNCTION
Power Indicator	CR3	Illuminates when unit is ON.
KEYER TONE LEVEL (Rear Apron)	R1	Permits adjustment of Tone Keyer output level.

3.3 OPERATING AIDS

3.3.1 RECEIVER

The performance of the FSK Demodulator depends to a large extent upon the type of receiver used, and upon careful tuning. For best results, use a single-sideband receiver with good frequency stability, variable IF bandwidth selectivity, a product detector, slow AVC, and passband tuning. The operator should read the instruction manual for the receiver, and thoroughly familiarize himself with its operation.

3.3.1.1 FREQUENCY STABILITY. Receiver frequency stability is important in the reception of FSK signals. Frequency stability becomes extremely important with the narrower shifts. Any slow frequency drift, even with 850 Hz shift, can quickly interrupt copy from the strongest of signals.

3.3.1.2 SELECTIVITY. The normal AM broadcast receiver passes a band of frequencies five kHz or more in width. If such bandwidths were used in receiving FSK signals, background noise and adjacent-channel interference could ruin reception. Narrow IF bandwidths are thus desirable, since they can reduce and even eliminate much of this interference. Good single-sideband receivers will normally have two or more switch-selectable IF bandwidths. The proper IF bandwidth to use in a particular application depends upon the frequency shift of the received signal. In practice, always use the next widest receiver bandwidth than the bandwidth of the shift frequency. For example, with 850 Hz shift, the bandwidth should be greater than 850 Hz.

3.3.1.3 PRODUCT DETECTOR. A product detector in the receiver will improve the performance of the FSK Demodulator. This type of detector greatly reduces both intermodulation and harmonic distortion, thereby providing a cleaner signal from the receiver. Since automatic volume control can be used with the product detector, a more constant output will be obtained even during fading signal conditions.

3.3.1.4 AUTOMATIC VOLUME CONTROL. Some receivers provide slow and fast automatic volume control (AVC). Slow AVC should be used in receiving FSK signals, since a fast attack and a slow release are necessary. Slow AVC introduces the proper amount of delay in release to suppress noise during momentary absences of either signal frequency. With fast AVC, the receiver sensitivity recovers too quickly, thereby permitting excessive noise to appear.

3.3.1.5 BEAT FREQUENCY OSCILLATOR. Positioning of the mark and space frequencies in the IF passband of the receiver is critical for good performance. The two frequencies must be positioned so that they straddle the center point with equal amplitude. Failure to do this, especially with a very narrow bandpass, can result in a loss of the mark or space frequency. If the receiver Beat Frequency Oscillator (BFO) is varied to produce the mark and space frequencies, the operator must also know whether the BFO is tuned higher or lower than the received signals. This is illustrated in Figure 3-1. If the BFO is set higher in frequency than the received signals, the mark will be the lower frequency and the space will be the higher. This is the correct position for the mark and space signals. If the BFO is set too high, the space signal will be shifted outside the receiver passband, and the mark signal will approach the original position of the space signal.

Figure 3-2 shows the resultant signal relationship when the BFO is set to a frequency below that of the received signals. The mark and space signals have now changed places. Space is the low frequency and mark is the high frequency. If the BFO is set too low, the mark signal will be shifted outside the receiver passband, and the space signal will approach the original position of the mark signal.

All is not lost if the operator tunes the BFO to the wrong side of the signal frequency, provided that the mark and space signals still straddle the center point as shown in Figures 3-1 and 3-2. A wrong choice can be corrected by means of the SENSE switch on the FSK Demodulator. This switch reverses the mark and space signals at the output of the detector, thereby permitting the printer to function with the normal mark-space relationship.

To adjust a variable BFO, the receiver is tuned to noise only (i.e., a no-signal frequency), the +- switch on the Demodulator is selected, and the BFO control is set for a zero reading (center scale) on the meter. This operation balances the noise in the mark and space channels, thereby insuring equal amplitude signals when the receiver is properly tuned to keying.

3.3.1.6 PASSBAND TUNING. Passband tuning in a receiver permits the IF to be shifted a few kHz above and below its normal frequency. The shift is effected without altering the shape of the

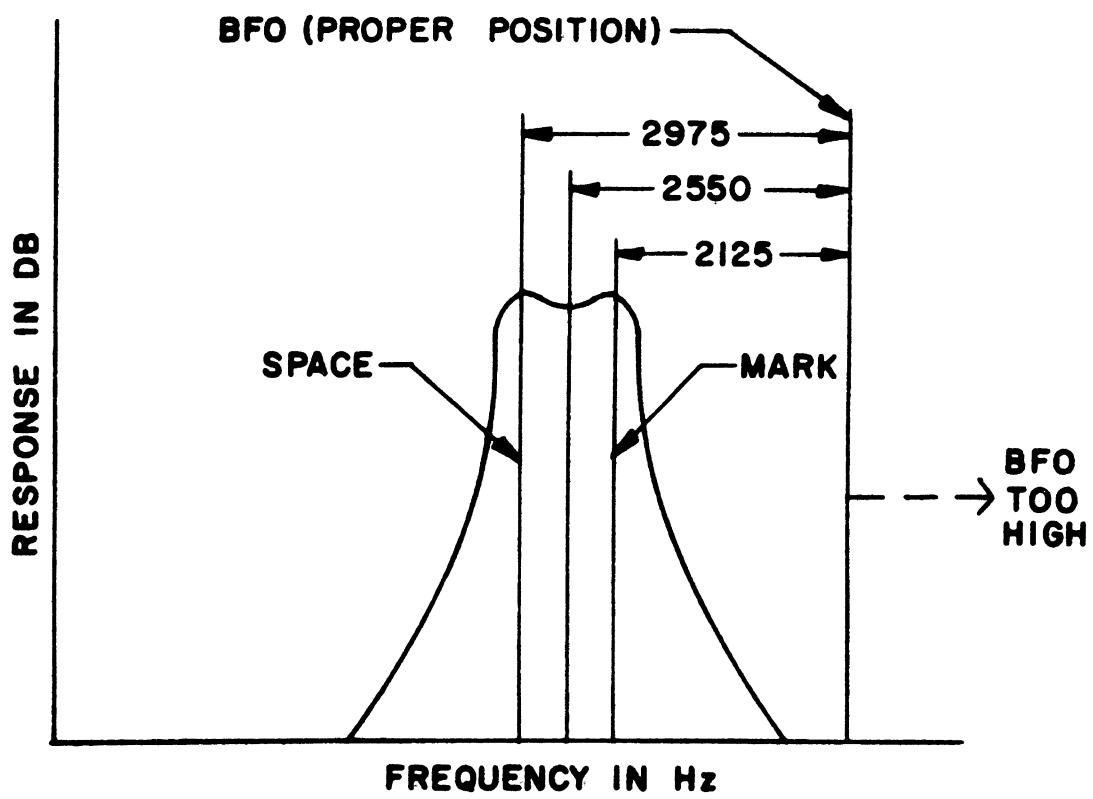


Figure 3-1. BFO Frequency Higher Than Signal Frequency

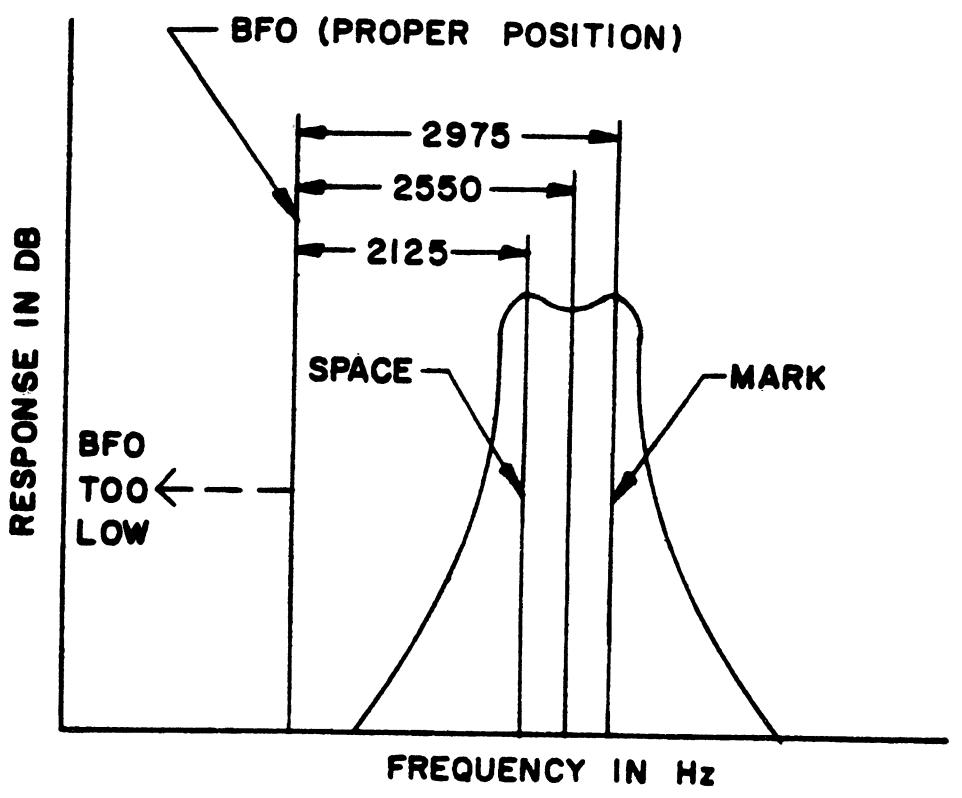


Figure 3-2. BFO Frequency Lower Than Signal Frequency

passband. This is particularly useful with interfering signals, since the passband can often be tuned to eliminate the unwanted signal. If the receiver has a passband tuning control, this control is substituted for the BFO control. The tuning procedure is the same.

3.3.2. DEMODULATOR

3.3.2.1 MODE SWITCHES. The MARK or SPACE switches select the channel transferred to the external TTY equipment. These operating modes are used only under special conditions. Normal operation transfers both channels and is usually selected. The Auto Mark-Hold (AMH1) mode of operation holds the outputs of the Demodulator in a steady mark condition during the absence of incoming signals to deactivate the external TTY equipment.

3.3.2.1.1 Limiter Mode. The limit function permits the operator to insert an additional 30 db (minimum) of gain (LIMIT depressed). Use of this mode is dependent upon the characteristics of the receiver. Normally the unit should be operated in the linear mode (LIMIT switch in out position). If reception is unsatisfactory, depress the LIMIT pushbutton switch to obtain the additional gain.

3.3.2.2 DEMOD/KEYER METER SWITCHES. There are six meter switches, four are associated with the Demodulator circuits of the Model 1273.

The ++ switch is used in tuning the receiver to an FSK signal. If only a carrier is present (no keying) the receiver is tuned for maximum needle deflection with the MARK indicator on. If keying is present, the receiver is tuned for maximum deflection and minimum oscillation of the meter needle. Both the MARK and SPACE indicators will flicker during keying.

The +- switch is used to obtain equal amplitude response (noise balance) from the mark and space channels. This response is obtained by first tuning the receiver to noise only and then by adjusting either the BFO or passband control until the needle rests at 0 (center scale). When the receiver is tuned to an FSK signal, deflection of the needle to the right indicates reception on the mark channel, and deflection to the left indicates reception on the space channel.

The LEVEL switch is used to adjust and monitor the amplitude of the audio input to the Demodulator. The input level is properly set when adjustment of the receiver audio gain control positions the meter needle at 0 DBM.

The LOOP switch is used to adjust and monitor output loop current from the Demodulator high level keyers.

3.3.2.3 STBY SWITCH. This switch controls the output circuit. When the STBY switch is pressed, the Demodulator output is held in steady mark. This is used during tuning.

3.3.2.4 DEMOD SENSE SWITCH. This switch is used to reverse the mark and space signals at the output of the detector, thereby permitting the output to function with the proper mark-space relationship. There is no set position for the DEMOD SENSE switch since mark-space polarities may change with receiver tuning and other conditions external to the Demodulator.

SECTION IV

THEORY OF OPERATION

4.1 FUNCTIONAL DESCRIPTION

A functional block diagram of the Model 1273 Keyer/Demodulator is illustrated in Figure 4-1. An external communications receiver supplies FSK tone inputs to the Demodulator circuits. The Demodulator converts the FSK signals to Mark/Space teleprinter signals and provides a neutral/polar loop output, MIL-STD-188C, or EIA RS-232-C output signaling.

The keyer circuits of the Model 1273 accept neutral/polar loop or EIA mark/space input data bits. Different frequency shifts can be selected by changing the keyer mark/space oscillator crystals.

4.1.1 DEMODULATOR

The FSK input tone is applied across an input isolation transformer to the input circuits.

The input circuit is comprised of a buffer amplifier, bandpass filter, and limiter. Limiter operation is controlled by the LIMIT MODE pushbutton switch. The circuit provides at least 30 db of additional gain in limiter operation over linear operation.

The Mark and Space Bandpass Filters are comprised of two identical 5-pole active networks which separate the audio tone input into its mark and space tones. Each channel filter has a narrow bandpass designed for aiding the detectors in achieving optimum signal detection. The filter outputs are detected individually, amplified, and applied to a postdetection Dual Active Low Pass Filter. After low pass filtering the mark-space channels are applied to the DTC (Decision Threshold Computer) circuits.

If mark and space diversity inputs are used they are inserted in their respective channels prior to the postdetection filters. These inputs are utilized in a diversity reception system and are normally supplied by a slave Demodulator unit.

The DTC circuits increase the reception capabilities of the unit during fading conditions in either the mark or space channel. Each channel DTC circuit sets a decision threshold which varies with the input signal amplitude. When sufficient signal strength is available, the mark and space signals are detected and undesired noise levels are rejected since they exist below the threshold level. In the presence of fading in either channel, the DTC circuits select the optimum channel to carry the received information.

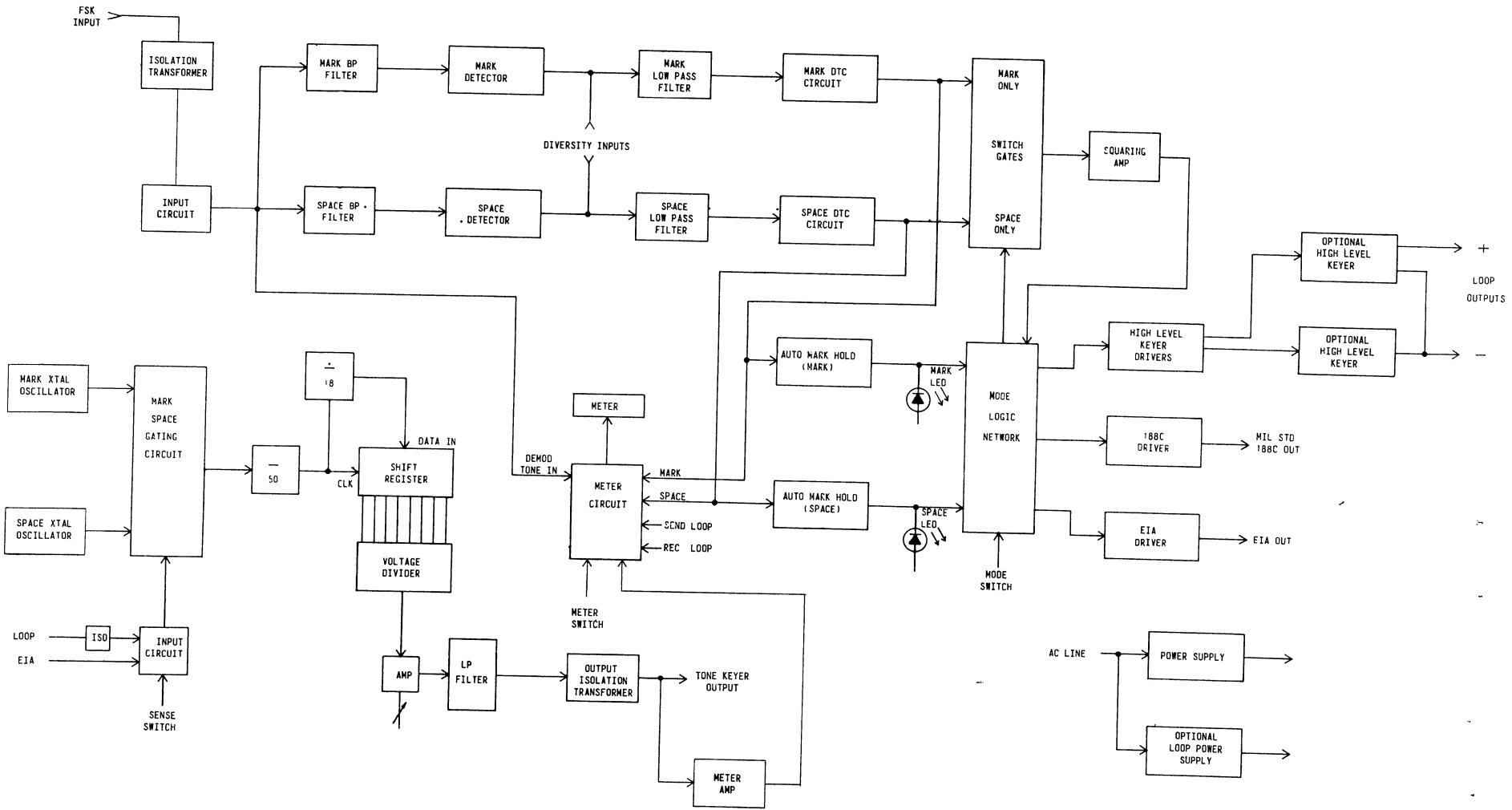


Figure 4-1. Model 1273 Block Diagram
D3359A

The Auto Mark-Hold circuit samples the mark and space channels and automatically returns the output of the Demodulator to the mark state in the absence of signaling or when the received signal drops below a preset signal level. The Auto Mark-Hold circuit is controlled by the front panel AMH1 MODE switch. In the AMH1 mode, the absence of signals in either the mark or space channel, or both channels will activate the Mark-Hold circuit.

The Mark Only and Space Only switch gates are controlled by the front panel MARK and SPACE MODE switches and permit selection of the optimum channel or both channels.

The selected output of the DTC circuit is applied to a squaring circuit prior to application to a Mode Logic Network. The Mode Logic transfers the mark-space data and is controlled by the STBY MODE and DEMOD SENSE controls or the Auto Mark-Hold circuit. When in STBY or when Mark-Hold is initiated, the control gating circuit locks the Demodulator output in the mark condition. The DEMOD SENSE control reverses the polarity of the detected mark-space signals to provide the proper mark-space relationship at the Demodulator's output.

The Demodulator output circuits provide high level neutral or polar loop, EIA RS-232-C, or MIL-STD-188C outputs through the respective Keyer/Driver circuits.

A meter circuit permits four Demodulator functions to be monitored and adjusted. These four functions are associated with the LEVEL, LOOP, ++, +- of the front panel switches. In the LOOP position, the meter monitors the current in the high level teleprinter circuit. In the LEVEL position, the meter reads the audio input level from the receiver. The ++ position is used when tuning the associated receiver to a FSK signal. In the +- position the meter is used to obtain an equal amplitude response (noise balance) from the mark and space channels.

4.1.2 TONE KEYER

The Tone Keyer is designed to accept isolated Neutral/Polar, 20/60 ma, high level mark-space data or EIA RS-232-C logic level data. Jumpers on the Tone Keyer board select the type of signaling. After high level isolation, and conversion to logic levels, inputs are applied to the Mark-Space Gating circuit.

The Mark-Space Gating Circuit transfers either the mark or space oscillator outputs to the divider input. A KEYER SENSE switch controls which oscillator output is selected for a given mark/space input signal polarity. Both the mark and space oscillators are controlled by plug-in crystals and operate at 900 times the output mark and space tone frequencies. An optional wire jumper selects a smaller portion of the Divider circuits to give operation at 180 times crystal oscillator output.

The Divider circuits supply a divide-by-50 clock and a divide-by-900 data pulse train to the Digital to Sine Wave Converter circuit. The converter is basically an eight-stage serial to parallel register with each parallel output being developed across a precision voltage divider network. Each of the outputs are summed developing a composite voltage level which varies in amplitude with the number of register stages which are loaded. Since the register clock and data inputs vary directly with the mark and space oscillator frequencies, a near sine wave AFSK signal is generated at the output of the circuit. This circuit configuration prevents instantaneous changes or jitter in the AFSK signal at the converter output as the data input signal shifts between the mark-space, space-mark states.

The converter output is amplified and applied to an Active Low Pass Filter circuit. The filter removes undesired high frequency components from the tone output. The output isolation transformer provides a 600 ohm output impedance from the Tone Keyer.

4.2 DETAILED CIRCUIT DESCRIPTION

4.2.1 DEMODULATOR

The Demodulator detailed circuit description is divided into the following major functions:

1. Input Circuit
2. Mark/Space Bandpass Filter Circuits
3. Detector Circuits
4. Dual Low Pass Filter Circuits
5. DTC Circuits
6. Mark-Hold Circuits
7. Squaring Amplifier Circuits
8. Keyer Circuits, EIA, and MIL-STD-188C Output Circuits
9. High Level Keyer Circuit
10. Meter Circuits
11. DC Regulator Circuits

4.2.1.1 INPUT CIRCUIT. The input circuit (Figure 6-1 Sheet 1) consists of isolation transformer T1, buffer amplifier Z2, active bandpass filter sections Z4, Z5, and Z6, and limiter circuit Q2, Q1 and Z7.

The AFSK tone input from the associated receiver is applied to pins 1 and 3 of the Demodulator board from the DEMOD input on the rear panel barrier strip. Transformer T1 sets the input impedance at 10K ohms or 600 ohms when the eyelet designated "1" is jumpered (shunting the primary winding). The transformer also provides overload protection.

In addition, the tone-input is sampled by meter amplifier Z16 when one of the front panel meter pushbutton switches is depressed (refer to Paragraph 4.2.1.10).

Active bandpass filter Z4, Z5, and Z6 passes the signals within the operating frequency band, attenuating all other frequencies. Resistors Z3-A, -B, -D, -G, -H, and Z1-A, -D, -E, -H are factory selected for appropriate bandwidth per operating frequency desired by the customer. Operation of the limiter circuit Q2, Q1, and Z7 is controlled by a voltage level input to J12-18 from the front panel LIMIT MODE switch.

The input from the LIMIT MODE switch is jumpered to J13-5 and applied to control the operation of the limiter circuit on diversity board NO1490 (1200A unit only). With LIMIT MODE switch depressed, an LL0 applied to J12-18 turns Q2 and Q1 OFF. Limiter Z7 is ON providing at least 30 db of gain. With LIMIT MODE switch in the OUT position, Q2 and Q1 are ON effectively bypassing Z7; with Z7 OFF operation is linear.

4.2.1.1.1 Optional High Impedance Input. (Refer to Figure 6-2.) The Optional High Impedance Input consists of operational amplifier Z1 on additional board NO964 (FEC assembly C2362). The new board provides a high impedance input and still provides an appropriate audio level to the standard input low pass filter. The new circuit is connected in series between rear panel connector TB1 and input connector J13 on Demodulator board assembly D3739.

The board is installed by plugging the mating connector from J13 into an identical set of male pins on C2362. A mating plug identical to J13 is wired to the output connections on C2362. This plug is inserted in place of J13 on D3739.

4.2.1.2 MARK-SPACE BANDPASS FILTER CIRCUITS. The Mark and Space Bandpass Filters consist of two printed circuit card assemblies D2818. Each bandpass filter is a 5-pole Butterworth network comprised of operational amplifiers Z1 through Z6 and other discrete circuit components (refer to Figure 6-3, Sheet 1). Components will vary with frequency shift and spacing.

Input signals from the input circuit are applied to the input port of the filter. Active filter amplifiers Z2 and Z3 form the first two poles of the filter. Amplifier Z1 provides negative feedback flattening the overall peak response. The eyelet jumper marked "1" removes the positive feedback signal when adjusting the filter tuning potentiometers.

Cascaded active filter amplifiers Z4, Z5, and Z6 provide improved overall response. Stages Z2 and Z3 usually have more gain than stages Z4-Z6 to improve dynamic range. Negative feedback is provided through resistor R34. The jumper across eyelet "2" is also removed during filter adjustment. The mark and space filter outputs are applied to the Demodulator detector circuits.

4.2.1.3 DETECTOR CIRCUITS. The detector circuits (Figure 6-1, Sheet 1) are comprised of operational amplifiers Z12, Z13, Z14, and Z15, and other discrete circuit elements. Since the mark

channel (Z12 and Z13) and the space channel (Z4 and Z5) are identical with the exception of diode and signal polarity reversal, only the mark channel detector is discussed in the following paragraphs.

The mark tone output from the mark bandpass filter is applied to the inverting input of operational amplifier Z12, through C10, R18, and R29 (mark signal level control). The Mark Detector output is also available through MOLEX connector J12 pin 7 for optional diversity connections. This signal is also suitable for connection to an external tuning and display monitor.

Detector Z12 has two half-wave rectified outputs, one the positive excursions of the output signal, and the other the negative excursions. Diode CR8 is forward biased during the negative voltage swing and diode CR9 is forward biased during the positive output voltage swing. Circuit gain is set to unity by feedback resistors R31 and R32. The stage is compensated by capacitor C11.

The half-wave rectified outputs of Z12 are summed in Z13. Z13 inverts the positive output of Z12, but not the negative output, thus providing a full-wave rectified output. Negative mark outputs forward bias diode CR10, transferring the mark envelope to the low pass filter circuit on board assembly D2913. Potentiometer R36 is an offset adjustment to compensate for dc voltage offset in Z13 for low level signals.

Diode CR10 in conjunction with a similar diode in a diversity unit form an OR circuit which selects the stronger signal for diversity reception.

4.2.1.4 DUAL LOW PASS FILTER CIRCUIT. The Dual Low Pass Filter circuit (Figure 6-4) is comprised of active filter stages Z1 and Z2 and other discrete circuit elements. The Dual Low Pass Filter circuits are contained on circuit board assembly D2813 which is plugged into the Demodulator board.

Resistive and capacitive component values vary with the operating baud rate. Filters are available on special order for any given baud rate within the operating range of the Model 1273.

The postdetection Dual Low Pass Filter is a three-pole device which provides rejection of the high-frequency components present in the mark and space channels. The mark channel is filtered through the negative section comprised of active filter Z2. The space channel is filtered through the positive section of the filter comprised of Z1.

4.2.1.5 DECISION THRESHOLD COMPUTER CIRCUITS. The Decision Threshold Computer (DTC) circuits (Figure 6-1, Sheet 2) consist of mark and space peak detectors Z11 and Z10, mark and space summing amplifiers Z19 and Z18, continuous-level input detectors

(JFET transistors) Q4 and Q3, and other discrete circuit components. The DTC circuits prevent loss of mark or space bit recognition during fading conditions, and false recognition of bits during fast-fade conditions with the input at steady mark or steady space.

Detected and filtered mark signals appear as a negative-going signal at the negative output of the low pass filter. Mark signals are applied to Z11 and Z19. Space signals appear as a positive-going signal at the positive output of the low pass filter and are applied to Z10 and Z18. Since the mark and space DTC circuits are functionally identical, only the mark DTC circuit will be described.

The mark DTC circuit is basically a dc amplifier made to act as an ac coupled amplifier. It varies the threshold level at which the output is gated. This offsets the signal so that it swings an equal distance on either side of ground at the Schmitt trigger input. Offset levels are established separately for the mark and space signals. The basic scheme used is to peak detect the incoming signal, divide the result by a negative one-half, then add this to the original signal. After the signals are offset separately, the mark and space signals are added together. This scheme reduces distortion caused by fading and thus increases the dynamic range. The gain of Z11 is set at $\frac{1}{2}$ by the ratio of resistors R21 and R22. The negative mark input signal is inverted through Z11 charging C9 to a positive potential equal to $\frac{1}{2}$ the peak mark signal amplitude.

The negative polarity mark signal (through R84) and the positive charge on C9 are summed by Z19. Since these signals are opposite in polarity, the negative mark input signal will be shifted so that its average value is zero. The gain of inverting amplifier Z19 is set at three by the ratio of feedback resistor R69 to R67 or R84. The output of Z19 will be a positive mark signal.

Figure 4-2 shows typical DTC waveforms. Waveform A, Figure 4-2 illustrates the varying threshold level with respect to an input mark signal of varying characteristics. The small amplitude mark pulses would normally go undetected as mark bits. However, the varying threshold level assures sampling of bits at approximate midamplitude. The dropout of the steady mark (A, Figure 4-2) is a result of a fast-fade condition. This would normally result in false recognition of a space bit. However, the threshold level prevents circuit response to the dropout condition. An example of DTC circuit operation is given in the following paragraphs.

4.2.1.5.1 Operation During Signal Conditions. Assume that the mark input signal begins to fade, decreasing the DTC threshold charge on C9. C9 has a time constant of approximately 300 ms

allowing it to follow typical fading rates (B, Figure 4-2). Note that the positive DTC capacitor charge will be such that the signal will be detected at one-half of the excursion of the negative mark input signal level, permitting accurate detection of the input signal. The threshold level is maintained at 6 db below peak amplitude. The DTC circuits improve the noise rejection capabilities of the Demodulator since the signal is shifted to midpoint for sampling.

4.2.1.5.2 Operation During Steady Mark Condition. Capacitor C16 has a relatively slow charge to rapid discharge ratio. During normal signal conditions, C16 barely charges (C, Figure 4-2). However, when a steady mark condition is present on the input, C16 charges through R68 to a positive potential determined by the series divider network consisting of R68, R52, and Q4; capacitor C9 discharges. This produces a potential at Z19-6 equal to 2 times the peak-to-peak signal amplitude (D, Figure 4-2). Zener diode CR6 prevents C16 from discharging. When normal signal is again present, C16 discharges rapidly through CR21.

In mark only operation, Q4 is turned OFF, opening the R68-R52-Q4 path, preventing C16 from charging. With Q4 OFF, operation of the mark DTC circuit is as described in Paragraph 4.2.1.5.1; the threshold level is fixed at approximately $\frac{1}{2}$ the peak signal level.

4.2.1.6 AUTO MARK-HOLD CIRCUITS. The auto mark-hold circuits (Figure 6-1, Sheet 2) consist of mark threshold detector Z29; space threshold detector Z30; switch transistors Q11 through Q14; NOR gates Z17-A, Z22-B, and Z27-D; NAND gates Z22-C and Z27-C; and inverter Z26-F.

The auto mark-hold circuits operate under control of front panel mode pushbutton switch AMH1. With the AMH1 pushbutton depressed, a LL0 is applied to pin 19 enabling one input of gates Z27-C and Z22-C. The other input is enabled when either the mark or space output of the DTC circuit goes to the below threshold condition, switching Z29 or Z30 to the mark-hold output condition and gating Z27-D to the LL0 output state. If both the mark and space outputs of the DTC circuit go to the below threshold condition, both mark-hold threshold detectors Z29 and Z30 and their associated switching transistors are activated enabling the two remaining inputs to gate Z22-C. Gate Z22-B is enabled by the auto mark-hold condition, setting the Demodulator output to the mark condition. The mark-hold threshold detectors operate as described below.

The non-inverting input to mark threshold detector Z29 is referenced slightly above ground by voltage divider resistors R90 and R91. The inverting input of space threshold detector Z30 is referenced slightly below ground by resistors R94 and R95. During a no-signal condition in the mark channel, characterized by

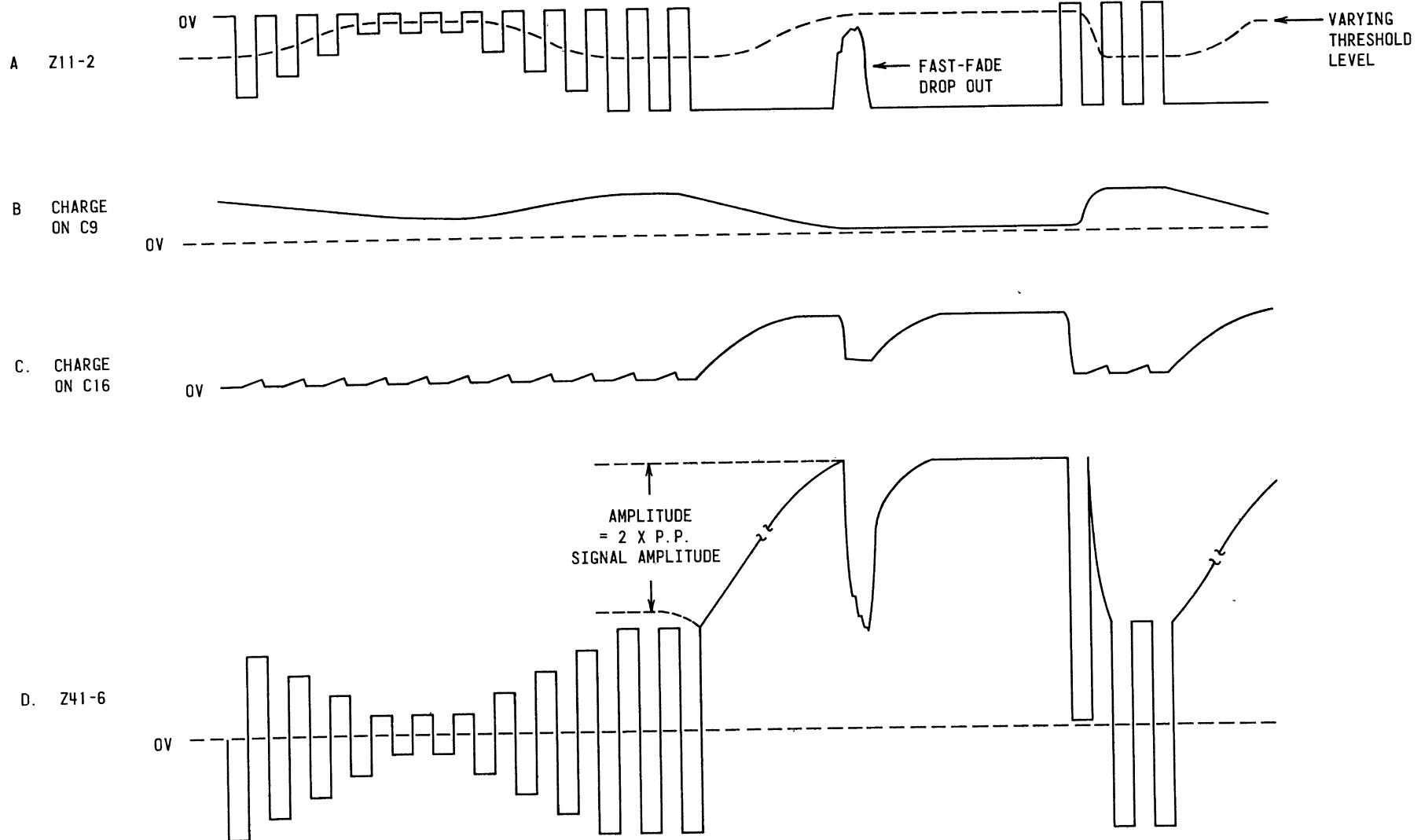


Figure 4-2. DTC Waveforms
C3402

a zero voltage at the output of the DTC circuit, threshold detector Z29 switches to the positive output state. This reverse-biases CR28, allowing C24 to discharge through R112. After a short delay period, Q12 is biased on. The conduction of Q12 switches transistor Q4 on, providing a positive enable input to gates Z22-C and Z27-D to initiate a mark-hold condition at the Demodulator output.

The operation of the space mark-hold circuit is identical with the exception that Z30 is connected to detect a negative signal condition at the output of the space DTC circuit.

4.2.1.7 SQUARING AMPLIFIER CIRCUITS. The Squaring Amplifier circuits (Figure 6-1, Sheet 2) consist of isolation amplifier Z24; operational amplifier Z23; JFET switch transistors Q8 and Q6; switch transistors Q7 and Q5; and gates Z17-C, Z17-D, Z22-A and Z27-A.

JFET switch transistors Q8 (mark channel) and Q6 (space channel) are controlled by the SPACE MODE switch input at pin J12-21 and the MARK MODE switch input at pin J12-20, respectively. The MARK input is associated with the MARK pushbutton switch on the front panel. When the MARK pushbutton switch is depressed, a LL0 is applied to the base of switch Q5, turning JFET Q6 and Q4 off. This prevents application of space signals to the operational amplifier and inhibits operation of the continuous-level input detection portion of the mark DTC circuit as described in Paragraph 4.2.1.5.2. Likewise, depressing the space pushbutton turns off JFET Q8 and Q3 interrupting the mark signal and affecting space DTC operation.

The amplifiers accept the combined analog mark-space signals from the DTC circuits and output a digital signal suitable for driving gates Z17-C and Z27-A. The output of Z23 can go above LL1. Resistor R75 is used to limit the current into the gates. These gates are also controlled by the DEMOD SENSE pushbutton switch on the front panel through pin J12-16. In one position, the supply voltage through R72 enables Z17-C when Z23 outputs a LL1 level. In the other position, a LL0 is applied through pin J12-16, enabling Z27-A only when Z23 outputs a LL0 level. The DEMOD SENSE pushbutton switch permits selection of the proper mark-space relationship at the Demodulator output. When the mark-space polarities are normal the output of Z23 will be in the LL1 state. For mark, gate Z22-A is enabled by the LL0 output of Z17-C in normal operation, and the LL0 output of Z17-D when the DEMOD SENSE pushbutton switch is depressed. Gate Z27-B is gated by mark polarity signals from Z22-A, or by the STBY or AMH1 pushbutton switch producing a LL1 state at Z22-B.

4.2.1.8 ±KEYER, EIA RS-232-C, AND MIL-STD-188C DRIVER CIRCUITS. The output driver circuits (Figure 6-1, Sheet 2) consist of inverter Z26-A; mark and space delay circuits comprised of Z26-B,

Z26-C, Z26-D, Z26-E, Z21-A, Z21-B, Z21-C, and Z21-D; MIL-STD-188C driver Z20; and EIA driver Z25.

The LL0 mark output from Z27-B is applied to MIL-STD-188C driver Z20. Zener diodes CR24 and CR25 limit the output to a +6.2V mark, and a -6.2V space output.

Mark outputs from Z27-B are inverted in Z26-A to LL1 mark signals to drive EIA driver Z25. The EIA driver supplies a positive space and a negative mark EIA RS-232-C output.

In the space output condition of Z27-B, a LL1 level is applied to the space delay circuit comprised of Z26-B, Z26-C, Z21-A and Z21-B, and a LL0 level is applied to the mark delay circuit comprised of Z26-D, Z26-E, Z21-C and Z21-D. The mark delay circuit prevents activation of the mark keyer for 80 μ sec to allow the space keyer to deactivate. Likewise, the space delay circuit delays activation of the space keyer. The delay circuits are required in the polar keying application to prevent simultaneous turn-on of the mark and space keyers. The remainder of the high level keyer circuit is contained on the Power supply board and is described in the following section.

4.2.1.9 HIGH LEVEL KEYER CIRCUIT. The high level keyer circuit is comprised of switch transistors Q1 and Q2 (Figure 6-5), two identical \pm high level keyer circuits contained on board assemblies C3240 and additional discrete circuit elements. The LL1 level from the mark delay circuit just described provides a positive turn-on voltage to the base of Q2, turning on the mark keyer. In a similar manner, the LL1 level from the space delay circuit is applied to the base of Q1, turning on the space keyer.

Only one of the high level keyer modules is required for neutral loop signaling. The keyer module is installed in the MARK KEYER position for neutral loops. The second keyer is installed in the SPACE KEYER position for polar loops. The mounting holes and mating pins are patterned to prevent incorrect mounting of the keyers. Zener diode CR5 on the Power Supply board prevents the breakdown of Q1 and Q2.

4.2.1.10 METER CIRCUITS. The Demodulator meter circuits (Figure 6-1, Sheet 1) consist of operational amplifiers Z8, Z9, and Z16 and pushbutton switches S8 through S11.

The meter circuits provide four switch selectable functions labeled: LOOP, LEVEL, $++$, and $+-$. When the LOOP pushbutton switch is depressed, the meter is connected across the output loop circuit through resistors R2 and R3. This permits monitoring of the Tone Keyer output loop current.

When the LEVEL pushbutton switch is depressed, the negative terminal of the meter is grounded and the positive terminal is connected to the output of meter amplifier Z16. The audio input

tone is rectified by Z16, CR14 and CR15. Meter deflection is dependent on the amplitude of the input tone and the setting of potentiometer R47. The potentiometer is provided to calibrate the meter for a 0 dbm level.

When the ++ pushbutton switch is depressed, the negative terminal of the meter is grounded and the positive terminal is connected to meter amplifier Z8 which inverts the output of the mark detector Z12 and sums it with the output of space detector Z14. The amplifier output provides a dc voltage which varies in amplitude with input signal strength. Depressing this switch gives a relative signal strength indication on the meter to aid in receiver tuning. Meter deflection is to the right of the center scale position.

When the +- pushbutton switch is depressed, the negative terminal of the meter is grounded and the positive terminal is connected to the output of meter amplifier Z9 which sums the primary channel mark and space detectors Z12 and Z14, respectively. This provides a center scale meter reading to show proper noise balance in the mark and space channels. The meter deflects on either side of the center scale position for mark and space inputs.

4.2.1.11 PSEUDO GROUND REGULATOR CIRCUIT. The Regulator circuit (Figure 6-1, Sheet 1) consists of transistors Q9 and Q10, and operational amplifier Z28.

The +24V output of the Power Supply board connects to J12 pin 10. A voltage, equal to one-half the input voltage is present at the junction to the non-inverting input of Z28. Z28 and transistors Q9 and Q10 are connected as a voltage follower with the transistors increasing the current output capability. This establishes a floating ground level for the demodulator circuits at J14 pin 10, which is half of the regulated power supply voltage.

4.2.2 TONE KEYER

The Tone Keyer circuits are divided into the following circuit groups: Refer to Figure 6-6.

1. Input Circuits
2. Mark/Space Oscillator Gating Circuits
3. Divider Circuits
4. Digital To Sine Wave Converter Circuits
5. Output Circuits

4.2.2.1 INPUT CIRCUITS. The input isolation circuits consist of transistor switch Q1, photo-isolator Z1, and threshold detector Z2.

The input isolation circuit accepts standard 20/60 ma, 130 vdc neutral or polar loop connections through board pins J20-2 and J20-3. In neutral keying operations, a jumper inserts resistor R1 or R2 in the base circuit of Q1 to provide selection of either 10 ma or 30 ma switching threshold for neutral loop inputs. In polar or EIA operation, the jumpers are removed from the input circuit. R3 is a series resistor used in monitoring the keyer loop current through R4.

Input mark current switches Q1 on applying a forward bias across the isolator diode Z1. This generates a positive level at the photo-isolator output which will switch threshold detector Z2 to a LL0 mark output condition. During space inputs, the photo-isolator output is negative, switching Z2 to a LL1 mark output condition.

In EIA operation, the high level input circuits may be used (Q1-Z1) or data may be applied to board pin J23-1. Negative polarity EIA mark inputs switch Z2 to a LL1 mark output condition.

The two jumpers marked MIL JUMPER and HALF DUPLEX JUMPER are included for half duplex operation. Feedback can occur if the Tone Keyer input and the Demodulator output devices share the same loop. The Tone Keyer must remain in mark while the Demodulator is receiving data or the received data will be retransmitted.

This is caused by the Demodulator loop also keying the Tone Keyer loop input. The HALF DUPLEX jumper must be installed when operating in this mode. This forces the Keyer loop to be locked in a mark state as the Demodulator loop changes state.

The MIL jumper is included to control the sense of the data input so that mark is a logic level zero at Z4-A pin 1. Thus, this jumper is used when a detected loop current corresponds to the mark state.

4.2.2.2 MARK-SPACE OSCILLATOR/GATING CIRCUITS. The Mark-Space Oscillator/Gating circuits consist of two identical oscillator circuits comprised of Y1-Q2-Q3, Y2-Q4-Q5; EXCLUSIVE OR gates Z3-A, Z3-C, Z3-D; NAND gates Z4-B, Z4-C; and other associated components.

Assume the mark oscillator will operate at a frequency of 1.9125 MHz which will develop a 2125 Hz mark tone frequency at the keyer output.

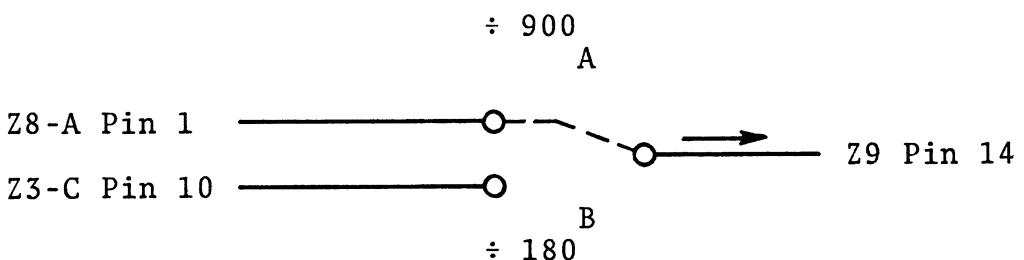
The Space oscillator comprised of crystal Y2, and transistors Q4-Q5 will operate at a frequency of 2.6775 MHz which will develop a 2975 Hz space tone at the keyer output.

KEYER SENSE switch S7 on the front panel provides either a LL0 or LL1 level to control EXCLUSIVE OR gate Z3-D. Depending on the position of S7, Z3-D will provide either inversion or a straight transfer of the threshold detector (Z2) output. Mark inputs gate Z3-D to a LL0 output state gating Z3-A high and enabling mark NAND gate Z4-C. This permits transfer of the mark oscillator signal through EXCLUSIVE OR gate Z3-C. Space inputs gate Z3-C to the LL1 output condition gating the space oscillator frequency through space NAND gate Z4-B and Z3-C.

4.2.2.3 DIVIDER CIRCUITS. The Divider circuit is comprised of flip-flops Z7-A, Z8-A, Z8-B, Z16; counters Z9, Z10; and gates Z15-A, Z15-C.

Flip-flops, Z7-A, Z8-A and Z8-B divide the gated mark or space oscillator frequency by a factor of five. Counter Z9 is driven by the divide-by-five output to provide a divide-by-50 clock to register Z13 and the divide-by-18 circuit comprised of Z10 and flip-flop Z16. This provides a final divide-by-900 data input to register Z13. The data input pulse rate for the example is 2125 Hz for mark ($1.9125 \text{ MHz} \div 900 = 2125 \text{ Hz}$) and 2975 Hz for space ($2.6775 \text{ MHz} \div 900 = 2975 \text{ Hz}$).

A special jumper is utilized to lower the division factor during operations above 3500 Hz. This jumper designated B lowers the division factor from $\div 900$ to $\div 180$ as shown below.



Crystal frequency should be Division Factor X Tone Frequency.

4.2.2.4 DIGITAL TO SINE WAVE CONVERTER CIRCUITS. The converter is comprised of serial-to-parallel register Z13, control gates Z12 and Z14, and precision voltage divider resistors R42 through R50.

The timing diagram illustrated in Figure 4-3 shows the conversion of the digital input to a near sinusoidal output waveform. It should be noted that each voltage step is not equal as shown in the illustration but varies depending on the point where it occurs in the sine wave. For example, the voltage change at the positive and negative transition points must change at a more rapid rate than changes in voltage at the positive and negative peaks of the waveform. Voltage divider resistors R43 through R50 are selected and form the output sine wave as described in the following paragraph.

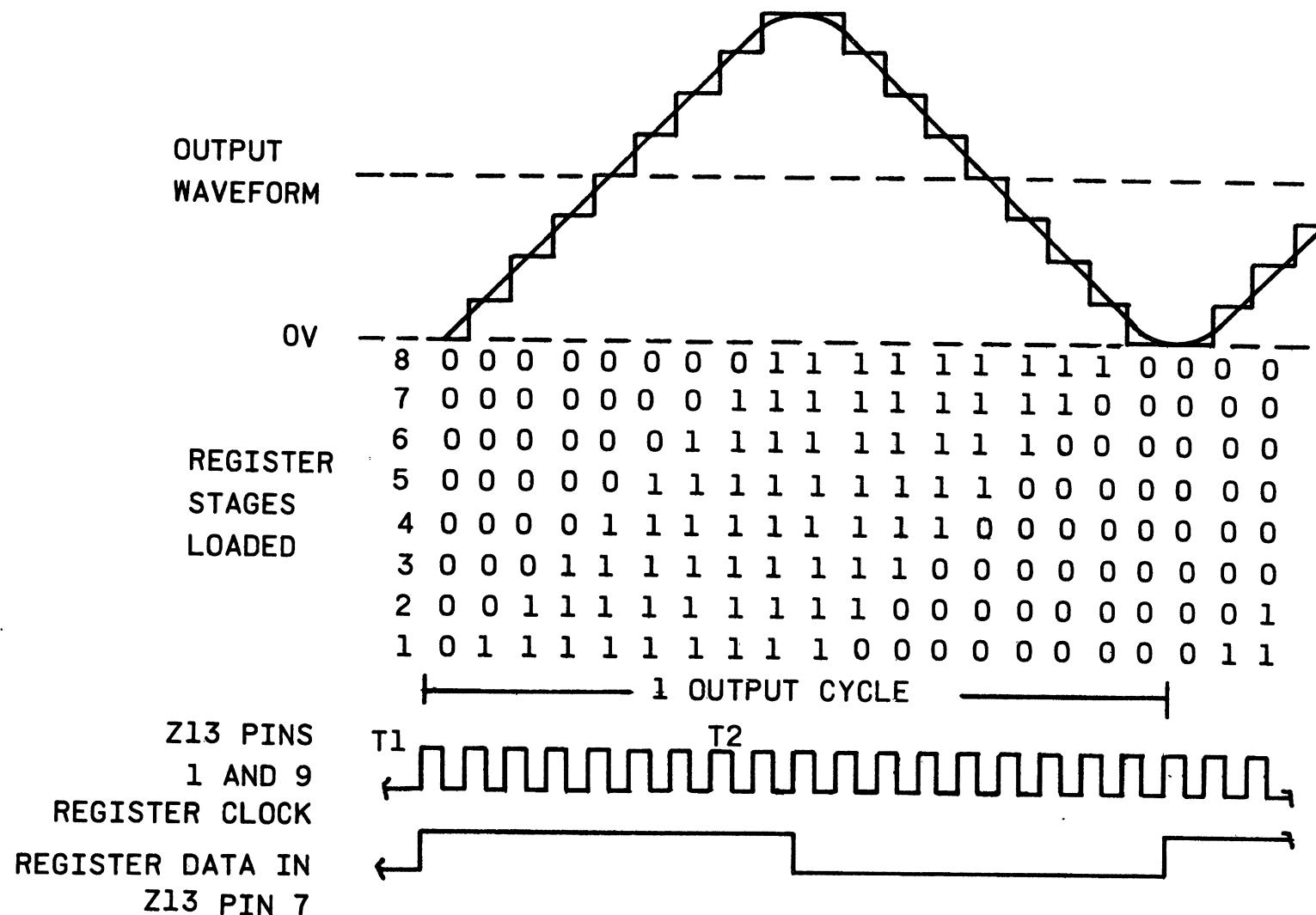


Figure 4-3. Digital To Sine Wave Converter Waveform Drawing
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Each positive transition of the register clock loads the serial input of the register depending on the logical state of the input. In the timing diagram shown in Figure 4-3, at time T1 all of the register stages are empty and the control gates at the parallel outputs of the register are open. This time is represented by the negative peak of the output waveform taken at the junction of R42 and R48. The next nine positive transitions of the clock input will load the LL1 level at the data input, loading the register. At this time (T2) the control gates at the register outputs are gated on placing output resistors R43 through R50 in parallel. In this condition, the majority of the supply voltage is developed across R42 and the positive peak of the output sine wave is generated. On the tenth positive clock transition the low portion of the divide-by-900 divider output will begin to empty the register forming the second half of the output cycle.

4.2.2.5 OUTPUT CIRCUIT. The output circuit is comprised of amplifier Z11, keyer gain potentiometer R1 on the rear apron, active output 3-pole low pass filter Z5, and isolation transformer T1.

Outputs from the digital to sine wave converter are applied to the inverting input of Z11. Amplifier gain is variable as set by Keyer Gain potentiometer R1 on the rear apron. The potentiometer varies the feedback loop resistance and is in parallel with C12.

Active low pass filter Z5 provides rejection of the remaining high frequency components existing above the mark and space tone frequencies. The network comprised of resistors R19 through R24 capacitors C1, C2, C3; and the jumper eyelet positions designated 1, 2, and 3 set filter characteristics.

The tone output of the low pass filter is applied to the primary of T1 and amplifier Z6 for the front panel meter. The secondary of T1 provides a balanced 600Ω output. These outputs connect to the keyer output at TB1 pins 9 and 10.

4.2.3 POWER SUPPLIES

4.2.3.1 AC POWER SUPPLY. The AC power supply circuits consist of power transformer T1, full-wave rectifier CR1 through CR4, preregulator Q3, series regulators Q5 and Q6, precision voltage regulator Z1, and voltage follower Z2, Q4. These circuits are contained on PC board assembly D2962 and are schematically illustrated in Figure 6-5. The circuitry in Figure 6-5 pertaining to the high level keyer is explained in Paragraph 4.2.1.9.

The power supply will operate from either a 115 vac or 230 vac power source. AC input switch S1, located on the power supply

board must be placed in the appropriate position. S1 also controls the ac input voltage to the loop power supply thru connector J3.

The ac output of transformer T1 is rectified by CR1 thru CR4 and filtered thru RC filter R10, C1, and C2. The supply voltage to Z1 is preregulated to approximately 36 vdc by zener diode CR6 and transistor Q3. Precision voltage regulator Z1 is a temperature compensated device and is controlled by feedback from potentiometer R1. A regulated +24 vdc ± 1 vdc is provided at board J5 pin 1 thru series regulators Q5 and Q6, and current limiting resistor R11. The voltage at J5 pin 1 can be adjusted by potentiometer R1. A regulated +14.5 vdc (+.5, -1 vdc) set by voltage divider R6 and R7, is provided thru voltage follower Z2 and Q4 to board pin J5-2.

The +24 vdc and +14.5 vdc are referenced to -V. Using this method the potentials +24 and -V float an equal amount from ground (i.e., +24 V is +12V from ground and -V is -12V from ground). Since +14.5V (VDD) is also referenced to -V, it will rest at approximately +2.5 volts from ground. The voltages ± 12 V from ground are used for all operational amplifier IC's and the voltages -12 and +2.5V from ground supply a total of 14.5 vdc to the CMOS digital logic.

4.2.3.2 OPTIONAL LOOP POWER SUPPLY. Additional space is provided for an optional loop power supply board. The polar loop supply can be ordered in any one of the following configurations:

100 ma/ ± 48 vdc
100 ma/ ± 64 vdc
40 ma/ ± 80 vdc

CAUTION

Currents are maximum values and must be limited by an external resistor.

The loop supply is schematically illustrated in Figure 6-7. Physical location is shown on the Model 1273 assembly drawing, Figure 7-1.

The polar loop power supply consists of T1, full-wave bridge rectifier CR1 thru CR4, negative voltage filter section C1-R1, and positive voltage filter section C2-R2. Each section furnishes the nominal voltages and current listed. T1 will operate from either a 115 or 230 vac power source, controlled by AC input switch S1, located on power supply board assembly D2962.

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SECTION V

MAINTENANCE

PART I. GENERAL MAINTENANCE AND PERFORMANCE CHECKS

5.1 GENERAL

The Model 1273 FSK Keyer Demodulator is a solid-state device designed to operate over extended periods of time with little or no routine maintenance. Should trouble occur, the information contained in this section will be helpful to a qualified maintenance technician. The technician should be thoroughly familiar with analog and digital integrated circuits and have a good understanding of the circuit theory and operating procedures before attempting any troubleshooting.

A discussion of the circuit theory is contained in Section IV. Schematic diagrams are contained in Section VI, and part location drawings in Section VII.

WARNING

The AC input circuit of this unit contains voltages which are hazardous to life. Exercise caution when working in the unit with protective covers removed.

5.2 PREVENTIVE MAINTENANCE

Since the Model 1273 is a solid-state low-power device, preventive maintenance is not recommended except during corrective maintenance. However, in locations with extreme environmental conditions, such as sand, dust, and/or large variations in humidity the unit may require periodic cleaning. Use a soft cloth or a medium bristle brush to clean the interior of the unit.

CAUTION

Do not use harsh cleaning solvents on painted surfaces.

5.3 CORRECTIVE MAINTENANCE

It is recommended that a complete visual inspection of the unit be made for indications of mechanical or electrical defects if

the unit is inoperative. Components showing signs of deterioration should be checked, and a thorough investigation of associated circuitry should be made to verify correct operation. Damage to parts due to heat is often the result of less obvious troubles in the circuit. It is essential that the cause of overheating be determined before replacing the damaged component. Mechanical parts such as switches and plug-in connectors should be checked for excessive wear, looseness, misalignment, corrosion, and other signs of deterioration.

If the technician thoroughly understands the operation of the Model 1273, malfunctions in its operation should be readily apparent by monitoring the input versus output signals and by observing the meter indications. For specific troubleshooting procedures reference Part II of this section.

5.3.1 REQUIRED TEST EQUIPMENT

The test equipment or its equivalent required to test and troubleshoot the Model 1273 is listed in Table 5-1.

Table 5-1. Required Test Equipment

EQUIPMENT	MANUFACTURER
Oscilloscope	Tektronix Model 422
Audio Generator	Hewlett-Packard Model 204C
Pulse Pattern Generator	Frederick Electronics Model 201
Decade Attenuator	Hewlett-Packard Model 350D
AC Vacuum Tube Voltmeter	Hewlett-Packard Model 400E
VOM	Triplett Model 630
Electronic Counter	Hewlett-Packard Model 5302A
FSK Signal Generator	FEC Model 1215A Tone Keyer
Digital Distortion Analyzer	Digitech Model 2683-01
Message Generator	Frederick Electronics Model 1306A

5.3.2 TROUBLESHOOTING

Troubleshooting procedures outlined in this paragraph may be utilized by a qualified technician to isolate a trouble to a specific circuit. When a trouble has been isolated to a specific circuit, a defective integrated circuit or component can normally be located using the detailed circuit description in Section IV.

After the top cover has been removed and a visual inspection has been made, measure the power supply voltages with reference to

NO1318, J5 pin 5. With a nominal input voltage of 115 vac or 230 vac, the dc voltages should be as follows:

POINT	VOLTAGE
NO1318, J5 pin 1	+24V ±1V
NO1318, J5 pin 2	+14.5V + .5V, -1V

CAUTION

Do not connect pins of J5 to the chassis or any other ground.

If the power supply is functioning properly and the visual inspection reveals no obvious trouble, then the logic or control circuits of the unit should be suspected.

After a trouble has been isolated to a defective component, circuits associated with that component should be checked to ensure that they did not cause the problem, or have not been damaged by the malfunction.

5.4 PERFORMANCE CHECKS

The following performance checks and adjustments may be required when the Model 1273 is initially installed. No subsequent adjustments should be required unless deemed necessary during troubleshooting procedures.

5.4.1 MARK/SPACE BANDPASS FILTER BANDWIDTH CHECK

The operating baud rate, center frequency, and bandwidth of the bandpass filters are determined by the dash number designated NO1158-() stencilled on the filter printed circuit card. Refer to the chart accompanying the schematic diagram.

Proceed as follows:

1. Set up the equipment as shown in Figure 5-1, with the signal generator connected to pins 12 and 13 of TB1 and the VTVM connected as shown by the dotted line.
2. Tune the signal generator to the mark tone center frequency at a 0 dbm output level.
3. Reconnect the VTVM between pins 2 and 10 of connector J17 and note the reading.

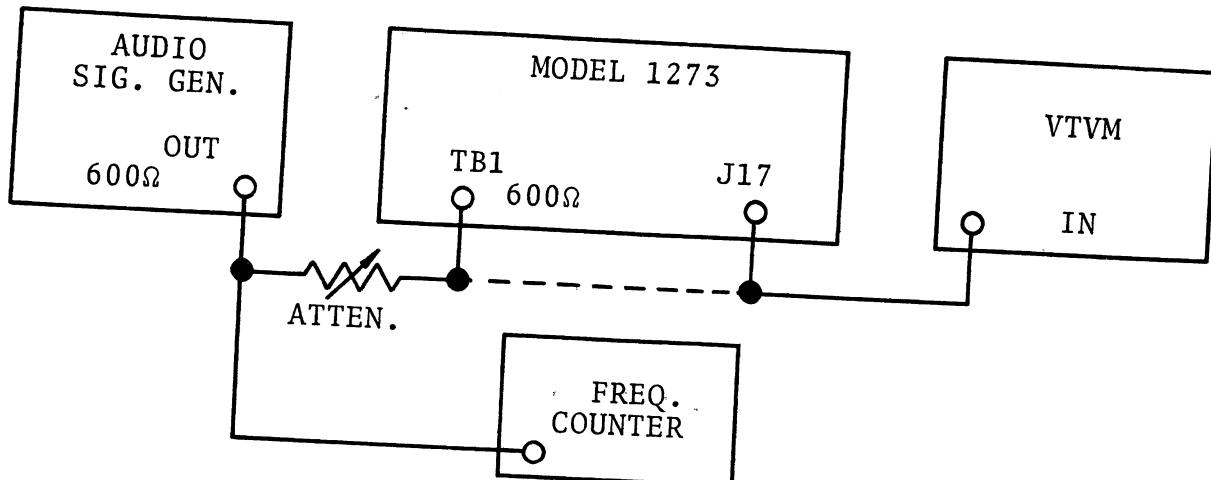


Figure 5-1. Test Setup, Mark/Space Bandpass Filter Operational Check

4. Increase the signal generator frequency to obtain a 3 db drop in the VTVM reading noted in Step 3. Check the frequency reading on the counter.
5. Decrease the signal generator frequency below the tone center frequency to obtain a 3 db drop in the reading noted in Step 3. Check the frequency reading on the counter.

NOTE

The filters bandwidth is correct when the two 3 db points are symmetrical with respect to the center frequency, within $\pm 10\%$ of the bandwidth. If the filter does not meet the above requirements, perform the alignment steps outlined in Paragraph 5.5.7.

6. Repeat Steps 1 thru 5 for the space bandpass filter, reconnecting the VTVM to pins 5 and 10 of J17.

5.4.2 TONE KEYER OUTPUT FREQUENCY CHECK

Proceed as follows:

1. Connect the frequency counter to TB1 pins 9 and 10.
2. Note the reading on the frequency counter. The reading should be the desired mark or space tone frequency.
3. Reverse the KEYER SENSE switch position.
4. Note the reading on the frequency counter. The reading should be the opposite tone frequency.

5.5 ALIGNMENT AND ADJUSTMENT PROCEDURES

5.5.1 POWER SUPPLY ADJUSTMENT

Proceed as follows:

1. Connect the positive voltmeter probe to J5 pin 1 on N01318. Connect the negative probe to J5 pin 5.
2. Adjust potentiometer R1 on the power supply for a +24 vdc ± 1 vdc reading on the voltmeter.
3. Connect the positive voltmeter probe to J5 pin 2. Check that this voltage is +14.5 vdc $\pm .5$, -1 vdc.

5.5.2 METER AMPLIFIER ADJUSTMENT

Proceed as follows:

1. Set up the equipment as shown in Figure 5-1, with the signal generator connected to pins 12 and 13 of TB1 and the VTVM connected as shown by the dotted line.
2. Depress DEMOD LEVEL pushbutton switch.
3. Tune the signal generator for the in-use mark tone center frequency at a 0 db output level. Check that the eyelet position designated "1" on the Demodulator board has a jumper installed to set the input impedance to 600 ohms.
4. Adjust potentiometer R47 on the Demodulator board for a 0 dbm reading on the front panel meter.

5.5.3 FSK KEYER OUTPUT LEVEL ADJUSTMENT

1. Connect the AC VTVM to TB1 pins 9 and 10. Actuate the Keyer LEVEL front panel switch.
2. Adjust KEYER TONE LEVEL potentiometer R1 on the rear apron for a 0 dbm reading on the AC VTVM. Adjust R14 on the Tone Keyer board until the front panel meter indicates 0 dbm.

5.5.4 MARK CHANNEL GAIN ADJUSTMENT

Check that filters are properly tuned before proceeding further.

Proceed as follows:

1. Set up the equipment as shown in Figure 5-1, with the signal generator connected to pins 12 and 13 of TB1 and the VTVM connected as shown by the dotted line (the LIMIT MODE pushbutton should be in the out position).

2. Apply a space tone at a level of -10 dbm.
3. Reconnect the VTVM between pins 4 and 10 of J17; measure and note the space filter output level.
4. Reconnect the VTVM as indicated by the dotted line in Figure 5-1 and set the signal generator to produce a mark tone at a level of -10 dbm.
5. Reconnect the VTVM between pins 1 and 10 of J17 and measure the mark filter output level.
6. If necessary, adjust the Level potentiometer R29 on the Demodulator board for the same level as noted in Step 3.

5.5.5 MARK AND SPACE RECTIFIER OFFSET

Proceed as follows:

1. Disconnect connector J13 from the Demodulator board.
2. Connect oscilloscope probe to pin 1 of J17 (select its most sensitive input) and oscilloscope ground to pin 10 of J17.
3. Adjust mark RECT OFFSET potentiometer R36 for zero-volt dc.
4. Reconnect oscilloscope probe to pin 4 of J17.
5. Adjust space RECT OFFSET potentiometer R45 for zero-volt dc.
6. Reconnect J13.

5.5.6 MARK AND SPACE DTC OFFSET

Proceed as follows:

1. Connect the output of the message generator to the data input of the tone keyer.
2. Connect the FSK output of the tone keyer as illustrated in Figure 5-2, with the FSK signal connected to pins 12 and 13 of TB1.
3. Make certain that the message generator and tone keyer are set at the proper baud rate and mark and space frequencies.
4. Connect distortion analyzer between pin 7 and pin 10 (ground) of J17.
5. Set message generator for steady mark output.

6. Set the attenuator to zero and ensure that the input to the 1273 is 0 dbm; adjust the output level of the tone keyer, if necessary, to obtain 0 dbm.
7. Set the message generator to produce a reversals output.
8. Adjust attenuator to obtain a -30 dbm input to the 1273 unit.
9. Set distortion analyzer for polar input, bias distortion, filter control -- OUT, and for operation at appropriate baud rate (all equipment should be operating at the same baud rate).
10. Depress the front panel SPACE MODE pushbutton.
11. Adjust SPACE DTC OFFSET potentiometer R83 for the lowest distortion indication on the distortion analyzer.
12. Release SPACE MODE pushbutton and depress MARK MODE pushbutton.
13. Adjust MARK DTC OFFSET potentiometer R86 for the lowest distortion indication on the distortion analyzer.

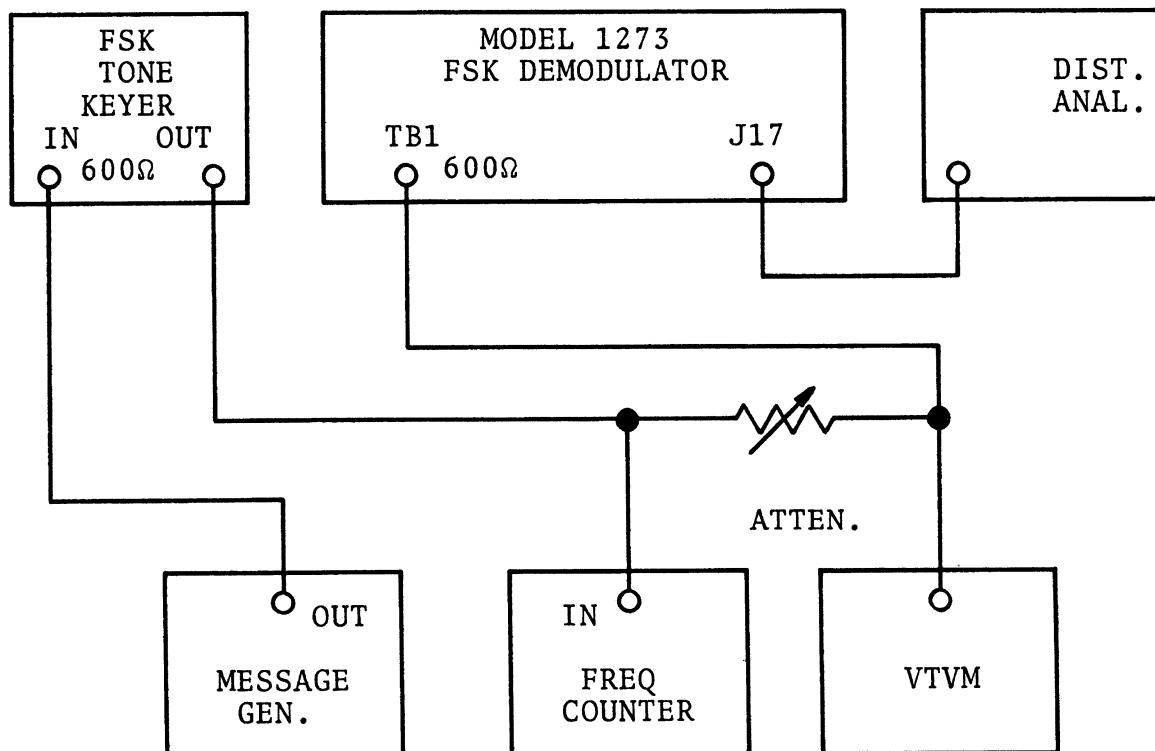


Figure 5-2. Test Setup, Mark/Space DTC Offset Adjustment

5.5.7 MARK AND SPACE BANDPASS FILTER ALIGNMENT

The mark and space bandpass filters are tuned at the factory for optimum operation. Prior to following alignment steps, insure that the filters are defective or misaligned by performing the checks outlined in Paragraph 5.4.1.

The alignment steps listed below apply to the Mark and Space bandpass filters located on the Demodulator board. Refer to Table 5-2 for the applicable test equipment input/output connections.

Table 5-2. Input/Output Connections For Bandpass Filter Alignment

FILTER UNDER TEST	SIGNAL GENERATOR CONNECTION	VTVM CONNECTION
Mark BP Filter	TB1 Pins 12 & 13	J17 Pin 2
Space BP Filter	TB1 Pins 12 & 13	J17 Pin 5

Proceed as follows:

1. Set up the equipment as shown in Figure 5-1.
2. Locate the eyelets marked "1" and "2" on the bandpass filter board. If jumpers are installed, unsolder one end of each eyelet jumper and remove from eyelet hole.
3. Tune the signal generator to the in-use mark or space tone center frequency at a -20 dbm output level.
4. Adjust potentiometers R4, R10, R19, R25, and R31 for a maximum indication on the VTVM.
5. Resolder jumper wires across eyelets "1" and "2", if originally installed.
6. Repeat the bandpass filter performance checks as outlined in Paragraph 5.4.1.

NOTE

If any filter fails the performance checks after alignment has been performed, return the defective filter to FEC.

PART II. TROUBLESHOOTING PROCEDURES

5.6 GENERAL

This section contains instructions for fault isolation to the active component in an inoperational Model 1273 FSK Keyer/Demodulator.

Paragraph 5.7 determines initial tests to determine the nature of a malfunction. Paragraph 5.8 lists steps in isolating the functional circuit in which the failure has occurred. Troubleshooting procedures are provided in Paragraphs 5.9 through 5.17 for the demodulator board, Paragraph 5.18 for the power supply and Paragraphs 5.19 through 5.23 for the tone keyer. Also included with these procedures are portions of the schematic diagrams contained in Section VI.

To gain access to the Model 1273, circuit boards, remove the screws securing the top panel.

5.7 DETERMINING NATURE OF MALFUNCTION

The Model 1273 consists of 3 main circuit boards. In Paragraph 5.8, step 1 refers to the power supply board, step 2 to the tone keyer and step 3 to the demodulator board. If the nature of the malfunction is not known proceed to the next paragraph.

With the unit plugged in, power on, and no input signal, monitor the tone output with an oscilloscope and depress the keyer sense switch. A tone frequency signal should be viewed which changes frequency as the sense switch is changed. If not refer to Paragraph 5.8, step 1 to be sure the keyer has power. Then proceed to Paragraph 5.8, step 2 to check the tone keyer.

Connect the tone output to the demodulator input on the rear panel. Monitor the demodulator output. Change the sense switch on the front panel. If the demodulator output does not change, refer to Paragraph 5.8, step 3 for demodulator repair. If the output changes but the unit is not functional refer to Section 5.5 for adjustment and alignment.

5.8 ISOLATING THE AREA OF A MALFUNCTION

1. Power Supply

Measure the DC voltage across pins 1 (+) and 5 (-) of J5. If approximately 24V is not obtained refer to Paragraph 5.18. If the voltage is present and correct, proceed to steps 2 and 3.

2. Tone Keyer

If there is no output from the tone keyer, first check the power supply.

If power is properly supplied to the board, monitor pin 10 of Z3. (Connect the oscilloscope between pin 10 and ground.) Oscillations should appear at one of the crystal frequencies. Changing the sense switch should change frequency. If this does not occur refer to Paragraph 5.9.

Monitor pin 1 of Z16 with the oscilloscope. If logic level changes are not present refer to Paragraph 5.10.

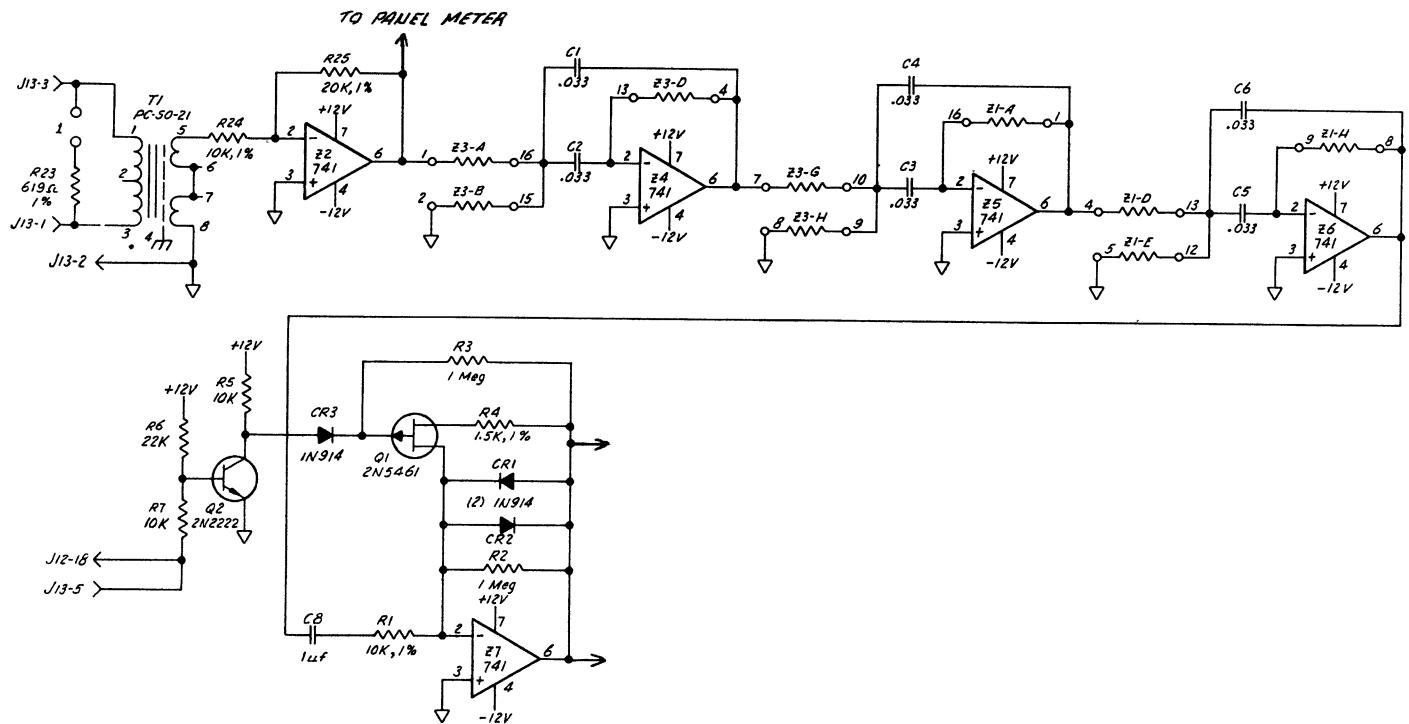
Monitor TP2. If a single similar to Figure 4-3 is not present refer to Paragraphs 5.11 and 5.12.

Monitor TP1. If a sine wave is not present refer to Paragraph 5.12. If no malfunction can be detected refer to step 3.

3. Demodulator

- a. Connect a tone keyed signal to the demodulator input on the rear panel. This may come from the tone output if it has been checked or an FEC Model 1215A or equivalent tone keyer. Monitor pin 6 of Z7. If tone signals are not present refer to Paragraph 5.17 to be sure power is available, then continue with Paragraph 5.9.
- b. Monitor J14 pins 1 and 4. A signal should be present at pin 1 when there is a mark input and at pin 4 for a space input. If not refer to Paragraph 5.10 and 5.11.
- c. Monitor TP2 and TP1. If mark signal is not detected at TP2 and space at TP1 when they are input refer to Paragraphs 5.12 and 5.13.
- d. Monitor TP3; if mark and space inputs are not distinct DC levels refer to Paragraph 5.14.
- e. If all checks to this point pass but there is no output refer to Paragraph 5.15.

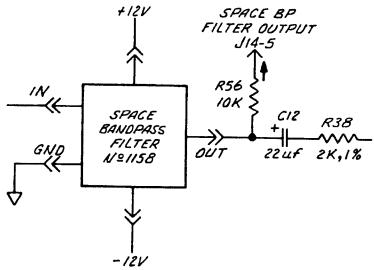
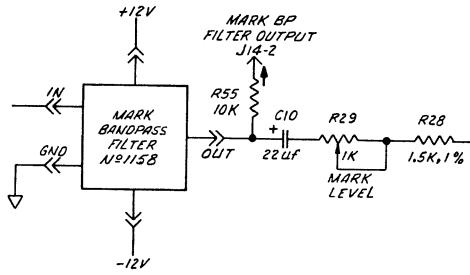
5.9 INPUT CIRCUIT (DEMODULATOR)



1. Ensure that jumper 1 is installed or removed for correct input impedance.
2. Connect a tone keyer output to the DEMOD input on the rear panel. The tone keyer output from the Model 1273 can be used. Check that tone frequency input appears across points 1 and 3 of T1. Monitor point 5 of T1. (Connect the oscilloscope between point 5 and ground.) If no signal appears replace T1.

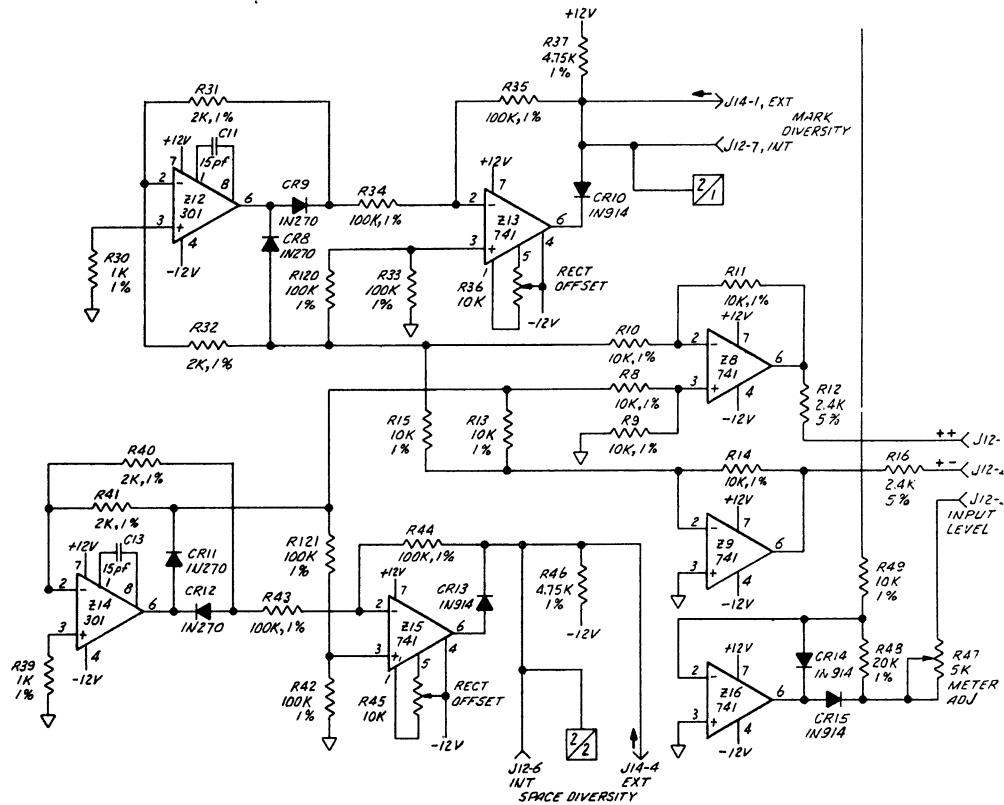
3. Monitor pin 6 of Z2. If an amplified signal does not appear replace Z2.
4. Monitor pin 6 of Z6 and change the input from mark to space tone frequencies. If either one but not the other frequency is transmitted to pin 6, check capacitors C1 to C6 and the values of resistor networks Z1 and Z3. The proper resistor values are given in Figures 7-10 and 7-11. If no signal appears at pin 6 of Z6 ensure that Z1 and Z3 are properly inserted and check or replace Z4, Z5, and Z6.
5. Monitor pin 6 of Z7. If no signal appears with the limit switch on the front panel in the off position, check or replace Q1 and Q2. If the signal is not amplified when the limit switch is depressed, replace Z7.

5.10 MARK AND SPACE BANDPASS FILTERS



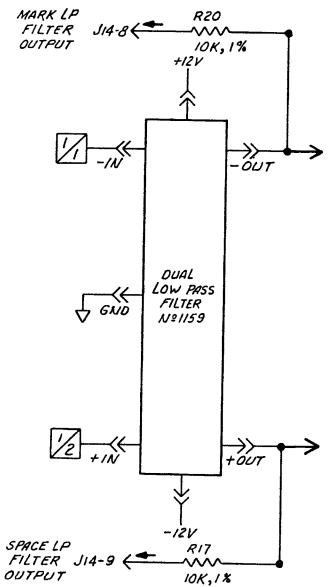
1. Monitor either side of C10. Set the input to mark tone frequency. Change the input to space and monitor either side of C12. If no signals or greatly attenuated signals appear, proceed to the mark/space filter bandwidth check in Paragraph 5.4.1.

5.11 MARK DETECTOR, SPACE DETECTOR, METER CIRCUITS



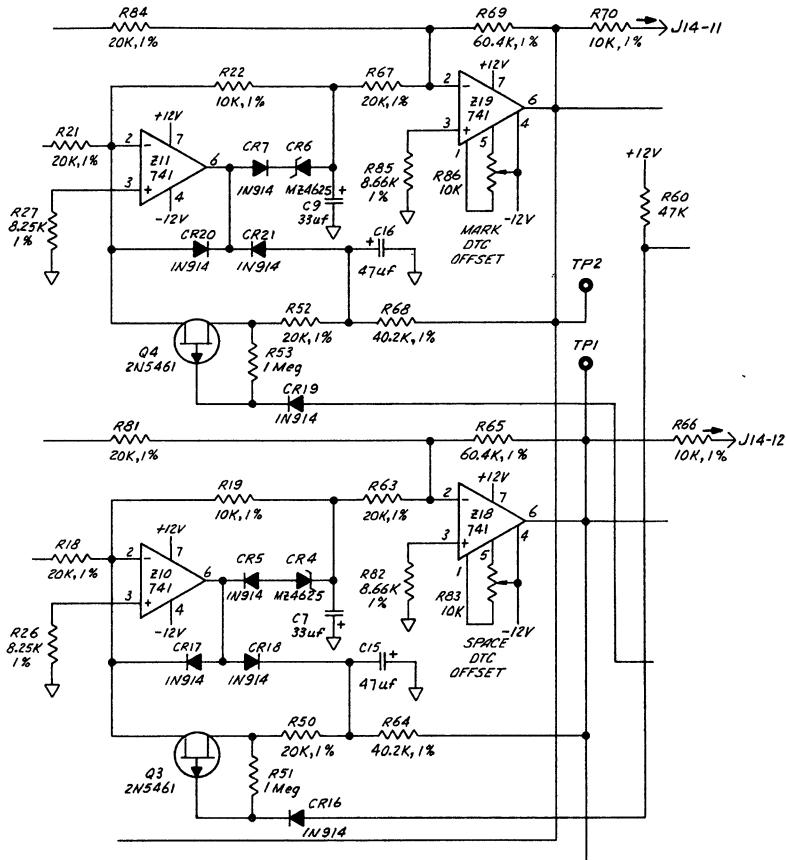
1. Monitor pin 6 of Z13. If no signal appears when the input is in mark, proceed to Paragraph 5.5.5 to check mark rectifier offset before checking or replacing Z12 and Z13. Monitor pin 6 of Z15 and repeat the same procedure with a space input, checking Z14 and Z15.
2. If the panel meter does not function check meter. If it is functional replace Z16.

5.12 DUAL LOW PASS FILTERS



1. Refer to Figure 6-4, Dual Low Pass Filter Schematic Diagram. Monitor either side of R20. If no signal appears when there is a mark input, replace Z1 on the Dual Low Pass filterboard.
2. Monitor either side of R17. If no signal appears when there is a space input replace Z2 of the Dual Low Pass filterboard.

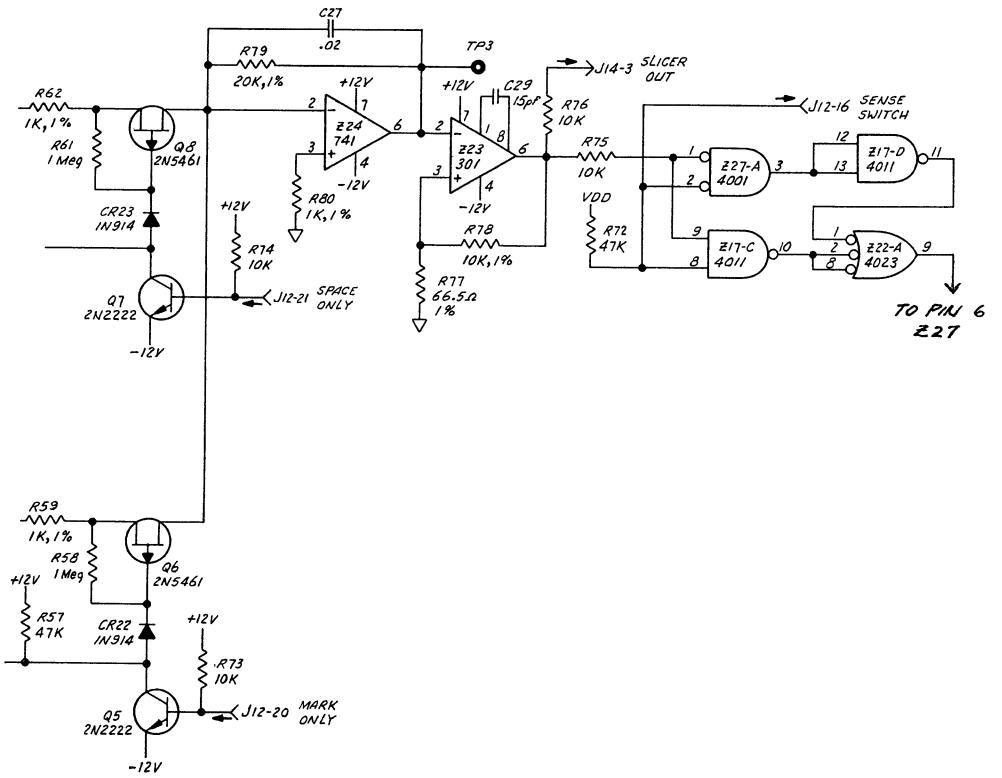
5.13 DECISION THRESHOLD COMPUTER CIRCUITS



1. If mark and space signalling are not detected at TP2 or TP1 respectively, check or replace Z11, Z19, and Q4 for mark failure and Z10, Z18, and Q3 for space failure.

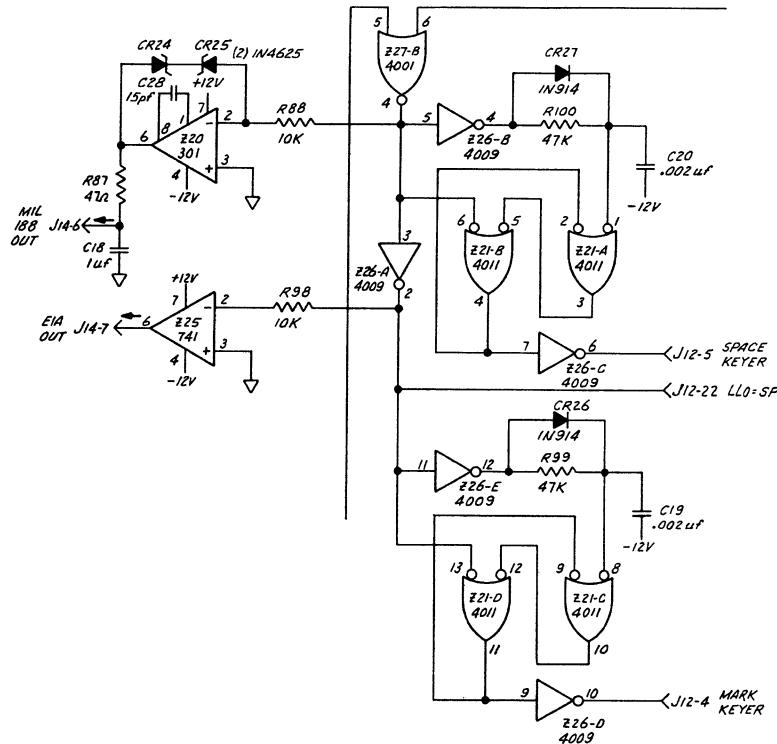
Refer to Paragraph 5.5.6 to correctly adjust Mark and Space DTC offset.

5.14 SQUARING AMPLIFIER CIRCUITS



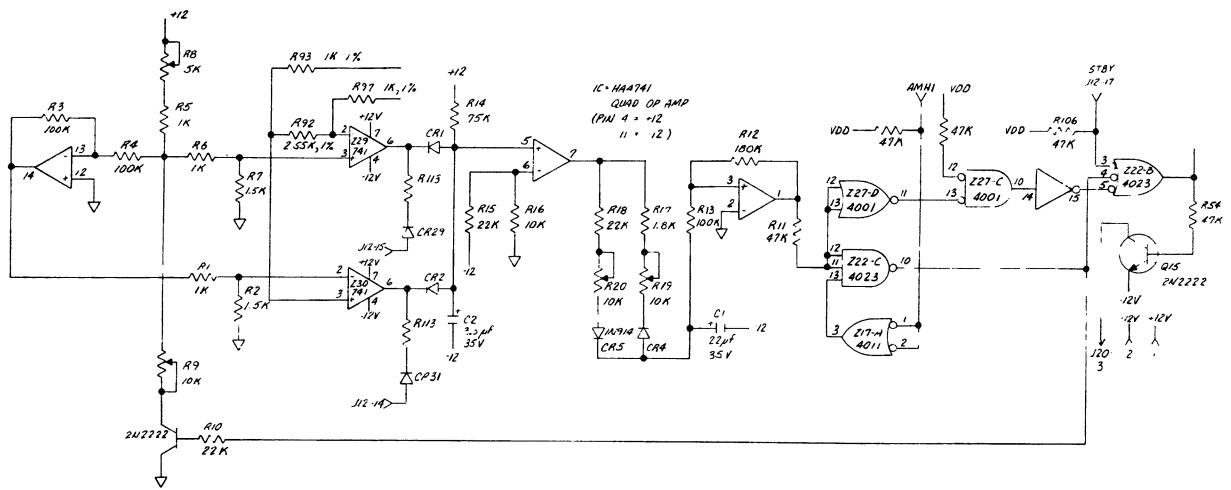
1. Monitor TP3. If mark and space inputs are not distinct DC levels, check or replace Z24, Q8, and Q7.
2. Monitor pin 1 of Z27. If mark and space inputs are not represented by distinct TTL levels replace Z23.
3. Monitor pin 6 of Z27. Changes in state should occur as the input to the unit changes states and also as the DEMOD switch is pressed or released. If not, check or replace Z17, Z27, and Z22.

5.15 KEYER OUTPUTS



1. Ensure that pin 5 of Z27 has a LL0. If not, refer to Paragraph 5.16. Monitor pin 3 or 5 of Z26. If there is no change as the input is changed from mark to space, or when the DEMOD switch is changed, replace Z27.
2. Monitor pins 6 and 10 of Z26. If they do not change state as the input changes from mark to space check or replace Z21 and Z26.
3. Monitor pin 6 of Z20 for MIL 188 output or pin 6 of Z25 for EIA output. If either does not change as the input changes from mark to space, replace Z20 or Z25 respectively.

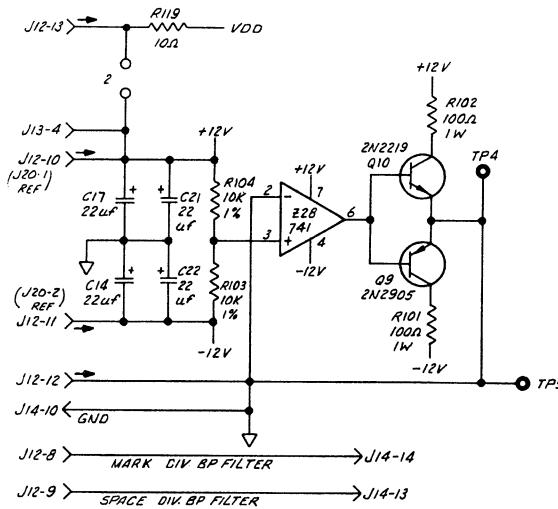
5.16 AUTO MARK-HOLD CIRCUITS



1. Disconnect the tone input to the unit. Monitor pin 12 of Z27. If it is not hi, check or replace Z29 and the quad operational amplifier.

Note: hi = board ground, lo = -12V.
 2. If Auto Mark-Hold (AMH1) does not function, check or replace Z27, Z17, or Z22.
 3. Monitor pin 6 of Z22. Depress STBY switch, if pin 6 does not go hi replace Z22.

5.17 POWER INPUTS AND REGULATOR CIRCUIT

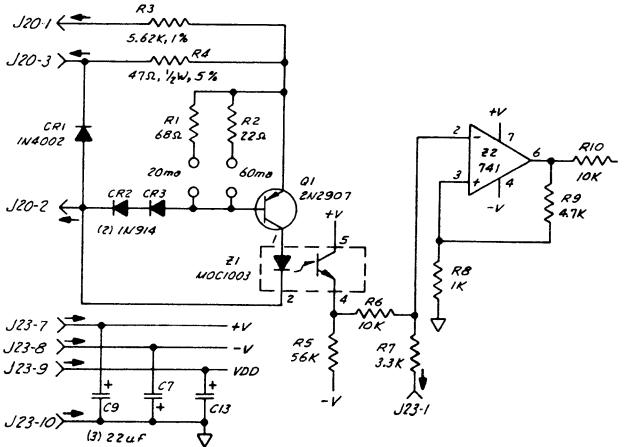


TP4 is at a floating ground potential for the board. There should be +12V between the + side of C21 and TP4 and also -12V between the - side of C22 and TP4. If not, check or replace Z28, Q9, and Q10.

5.18 POWER SUPPLY BOARD

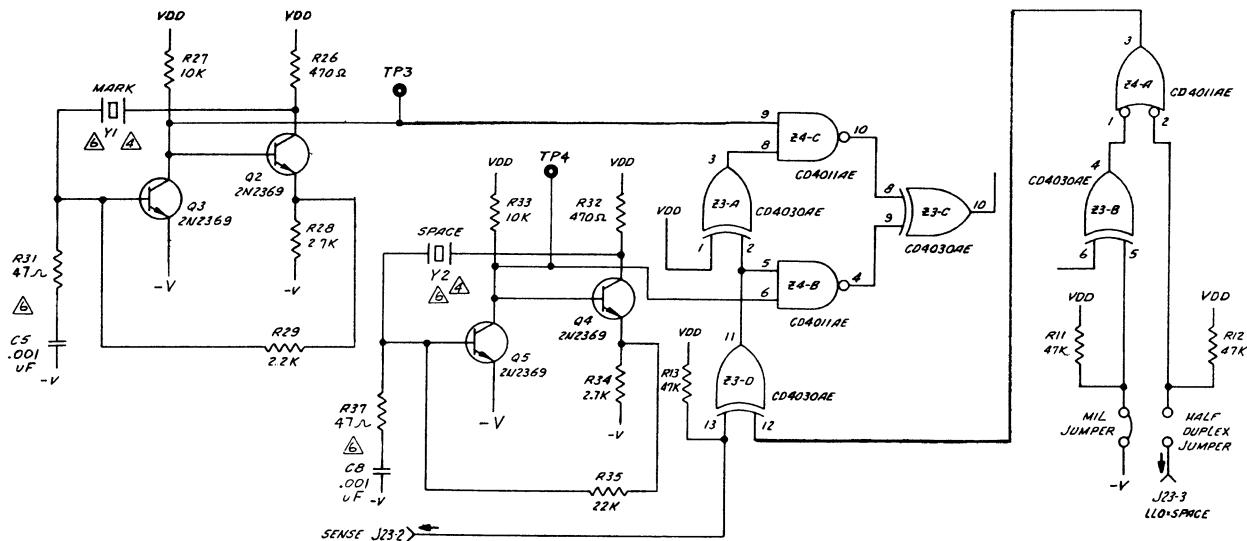
1. Refer to the schematic in Figure 6-5. Ensure that S1 is set properly to either 115 or 230V. The voltage across the two green leads from T1 should be 38 vac RMS. If not, check T1 for opens and replace if defective.
2. Measure the DC voltage across C1. Approximately 45V should be present. If not, check or replace diodes CR1 to CR4.
3. Check for 24V across C3. If no voltage is present, check or replace Q6. If the voltage is less or varies with the load, check or replace Z1, Q3, and Q5.
4. Check V_{DD} voltage. If 14.5V is not present check or replace Q4 and Z2.

5.19 INPUT CIRCUIT (TONE KEYER)



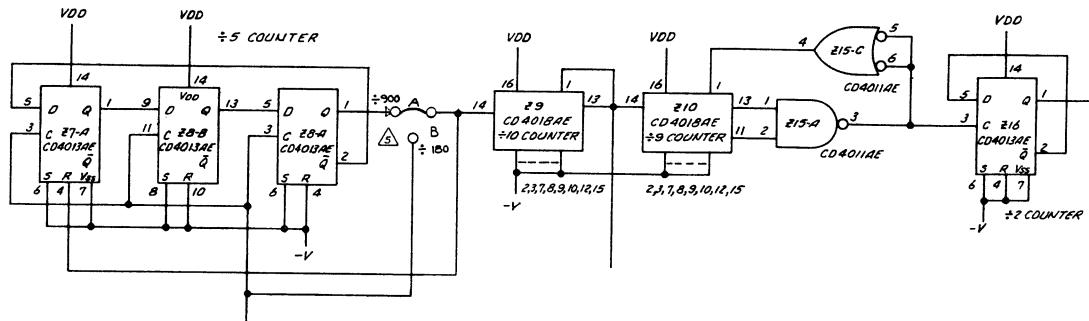
1. If logic level keying is being used proceed to step 2. If high level keying is used check that the unit is properly strapped for 20 mA or 60 mA operation. Connect the oscilloscope leads across pins 1 and 2 of Z1 and apply input keying to the + - loop inputs on the back panel. If the level changes are not apparent on the oscilloscope check Q1, CR2, CR3, and Z1. If level changes occur, reconnect the oscilloscope between pin 4 of Z1 and ground. If no level changes occur replace Z1.
 2. Connect a logic level keyer or any changing logic level output to the logic + - screws on the back panel. Connect the oscilloscope between pin 6 of Z2 and ground. If no change occurs replace Z12.

5.20 MARK/SPACE GATING CIRCUIT



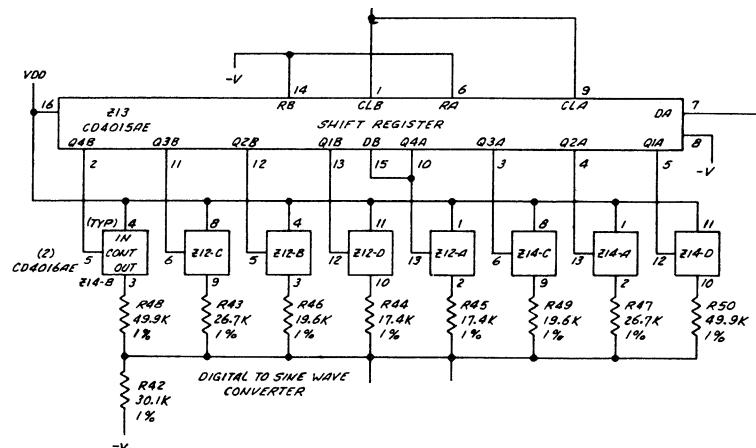
1. Monitor TP3. (Connect an oscilloscope between TP3 and ground.) Oscillations should be seen at the Y1 crystal frequency. If not, check or replace Q3 and Q2. Move the oscilloscope lead to TP4; note oscillations at the Y2 frequency. If there is no signal, check or replace Q5 and Q4.
2. If there is no input to the back panel, monitor pin 11 of Z3. Reverse the sense switch. If no change occurs at pin 11 replace Z3. Monitor pin 3 of Z3 and again reverse the sense switch. If no change occurs at pin 3, replace Z3.
3. Monitor pin 10 of Z4. Reverse the sense switch. Oscillations should be seen in only one position of the sense switch, repeat this procedure for pin 4 of Z4. If either fails replace Z4.
4. Monitor pin 10 of Z3. Reversing the sense switch should change the output from Y1 to Y2 frequency oscillations. If not, replace Z3.

5.21 DIVIDER CIRCUITS



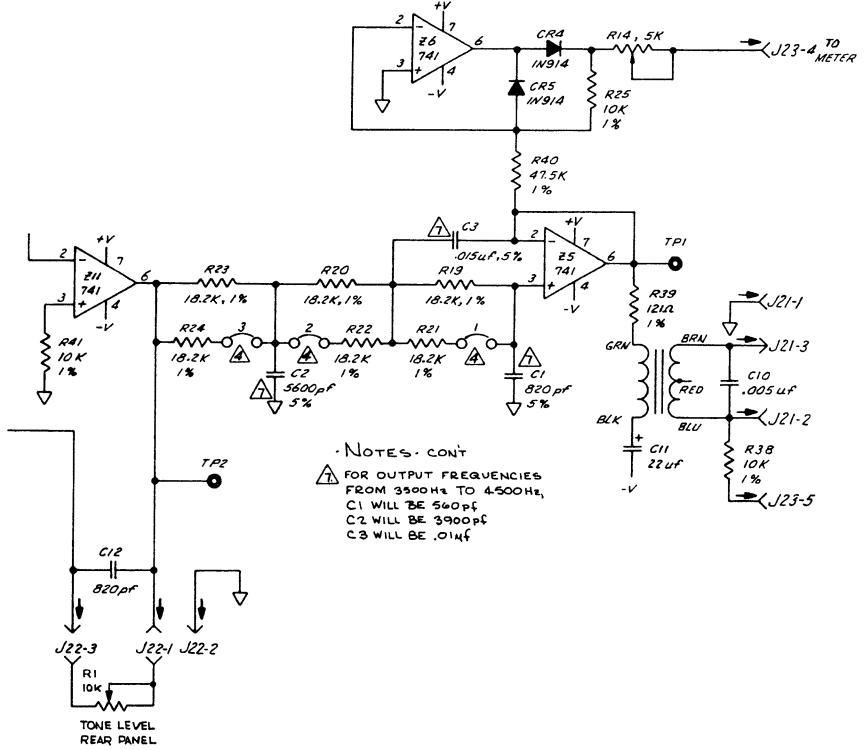
1. Monitor pin 3 of Z8. If there is no high frequency change return to Paragraph 5.20.
2. Monitor pin 1 of Z8. If high frequency logic level changes occur proceed to step 3, if not monitor pin 5 of Z8. If changes occur at pin 5 but not pin 1 replace Z8. If no changes occur at pin 5, monitor pin 2. If there are changes at pin 2 replace Z7, if not replace Z8.
3. Unless an external oscillator is used, be sure the jumper is in the A position. Monitor pin 14 of Z10. If there is no changing signal replace Z9. Monitor pin 3 of Z16. If there is no changing signal, check and replace Z10 or Z15.
4. Monitor pin 1 of Z16. If there is no output replace Z16.

5.22 DIGITAL TO SINE WAVE CONVERTER CIRCUIT



1. Ensure that changing inputs occur at pins 1 and 7 of Z13. If not, return to Paragraph 5.21.
2. With the oscilloscope set at approximately .1 ms/cm monitor pins 2, 3, 4, 5, 10, 11, 12, and 13 of Z13, one at a time. If each does not show a changing output replace Z13.
3. A similar output should appear at pins 2, 3, 9, and 10 of Z12 and pins 2, 3, 9, and 10 of Z14. If not, replace Z12 or Z14.

5.23 OUTPUT CIRCUIT



1. Monitor pin 6 of Z11. A signal approximating the one shown in Figure 4-3 should appear. If not, adjust R12 by rotating the amplitude screw on the back panel with a small screwdriver. If there is no response replace Z11.
2. Monitor TP1. A sine wave should be present. If not, replace Z5. If there is a signal present but no output at the rear panel check T1 and cabling. If replacing Z11 or Z5 does not correct the problem, check associated resistors and capacitors for opens or shorts.

SECTION VI
SCHEMATIC DIAGRAMS

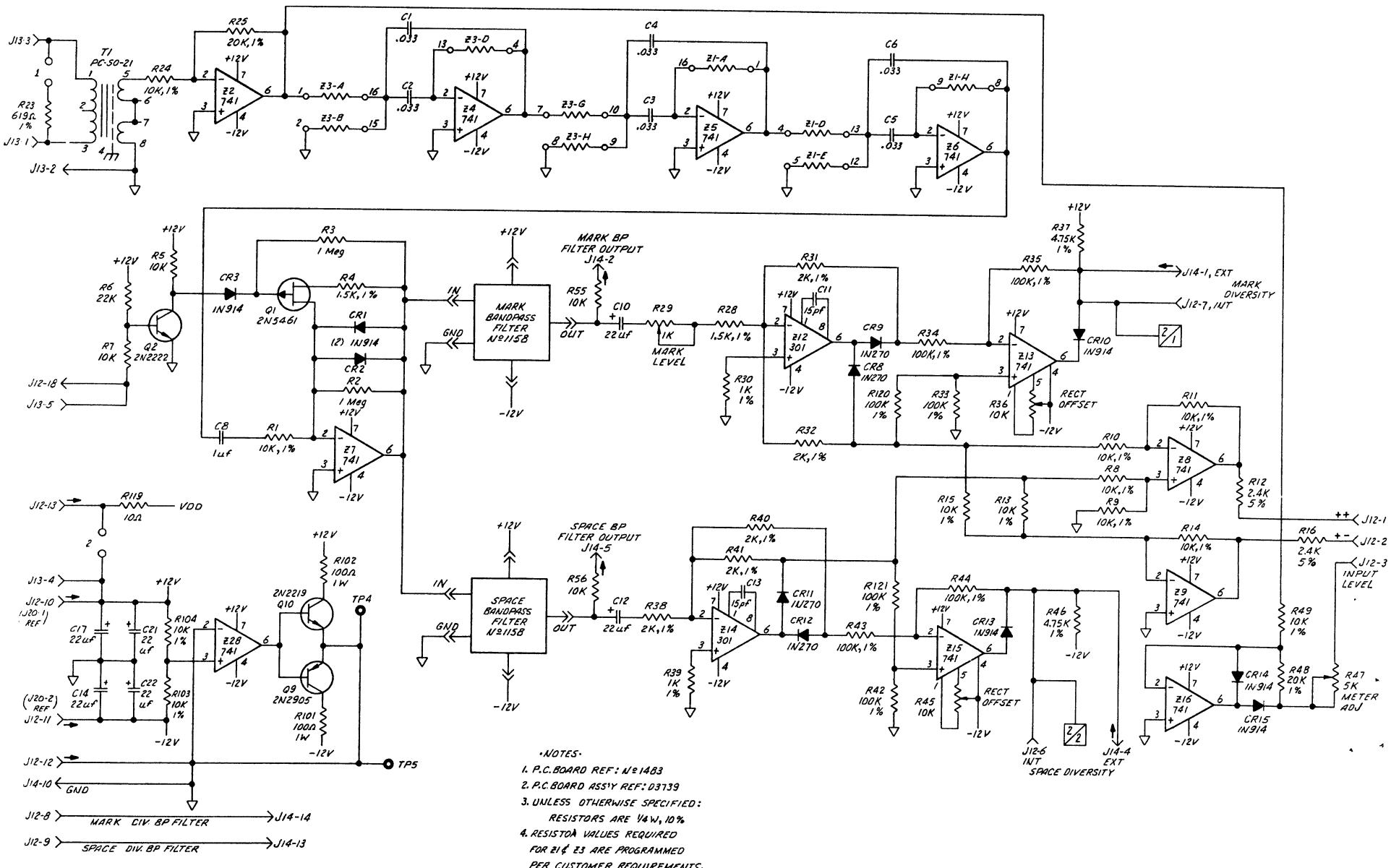


Figure 6-1. Primary Channel Demodulator Schematic Diagram
D3738A, Sheet 1

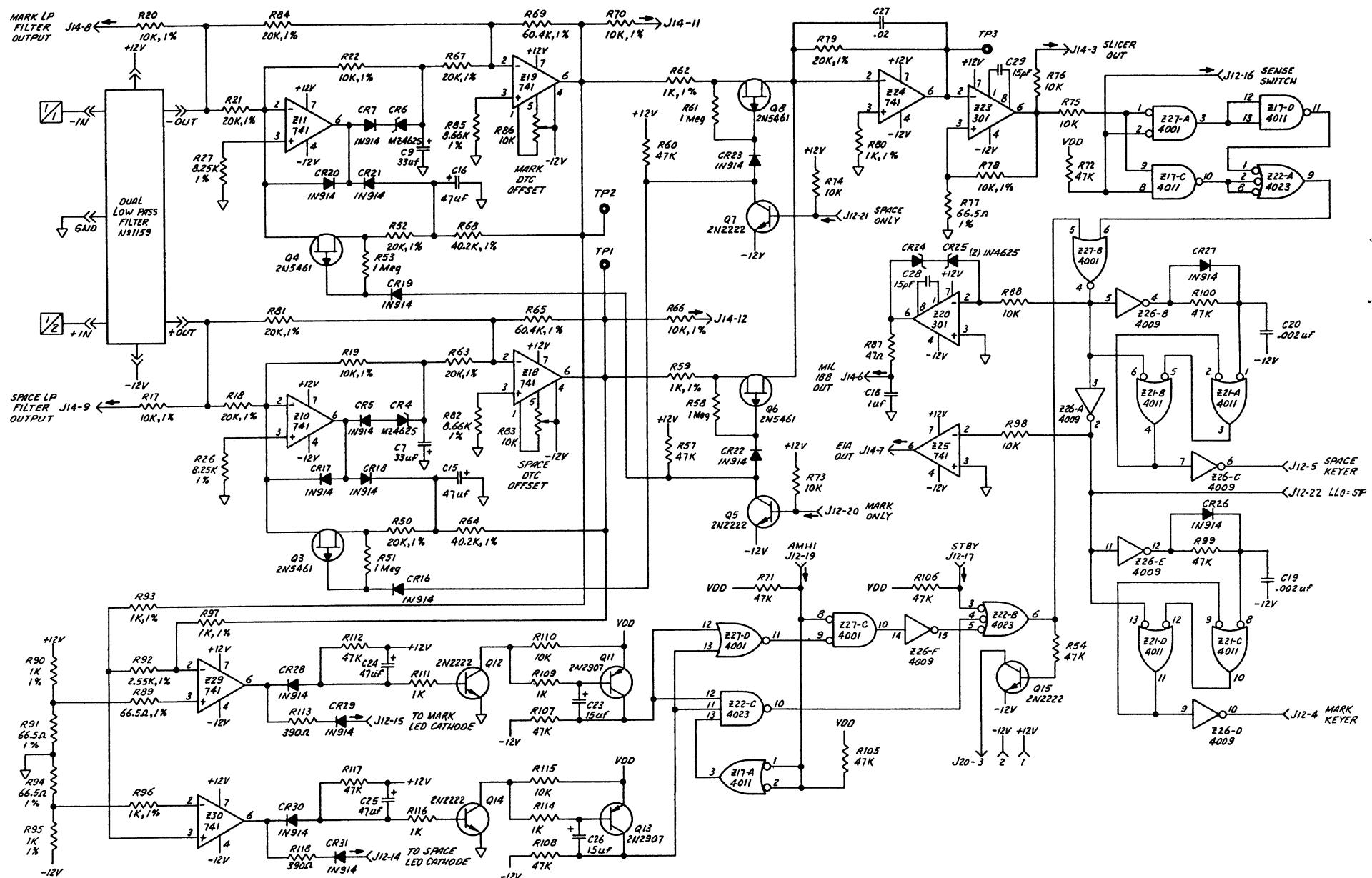
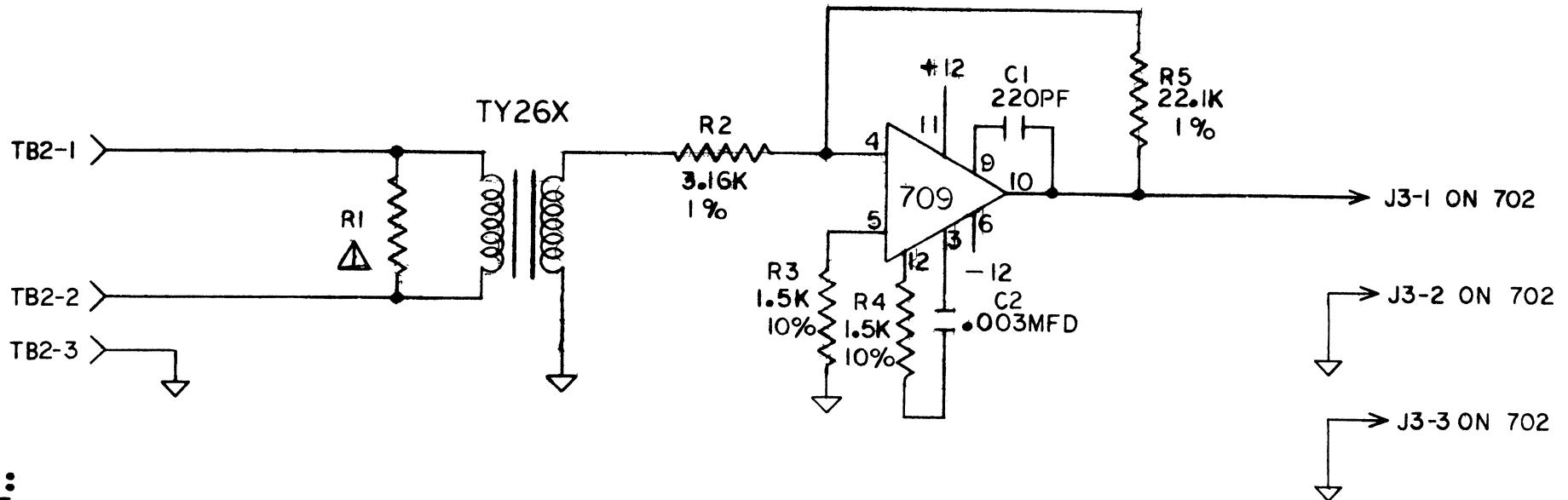


Figure 6-1. Primary Channel Demodulator Schematic Diagram
D3738A, Sheet 2



NOTES:

FOR JOB 4762 R1 24.9K FOR $Z \approx 20K$

FOR 100K INPUT IMPEDANCE OMIT R1

P.C.BOARD 964

P.C.BOARD ASSY. C2362

⚠ UPON CUSTOMER REQUIREMENT

Figure 6-2. High Impedance Input Schematic Diagram
C2361

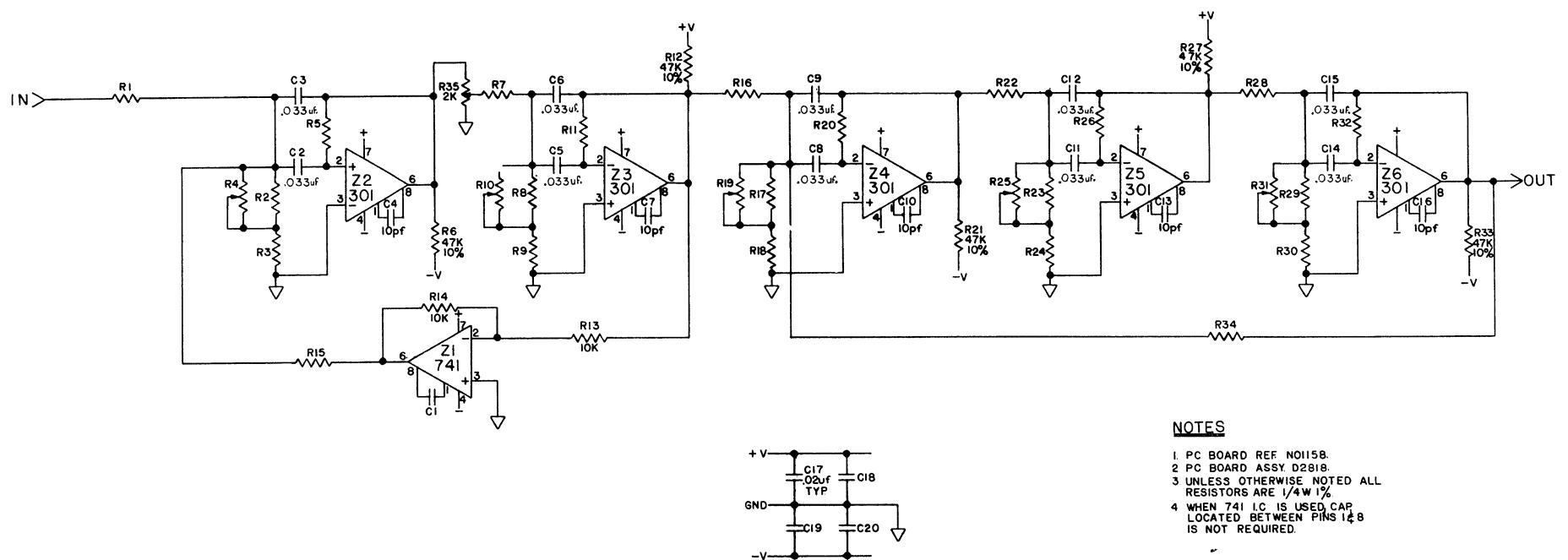
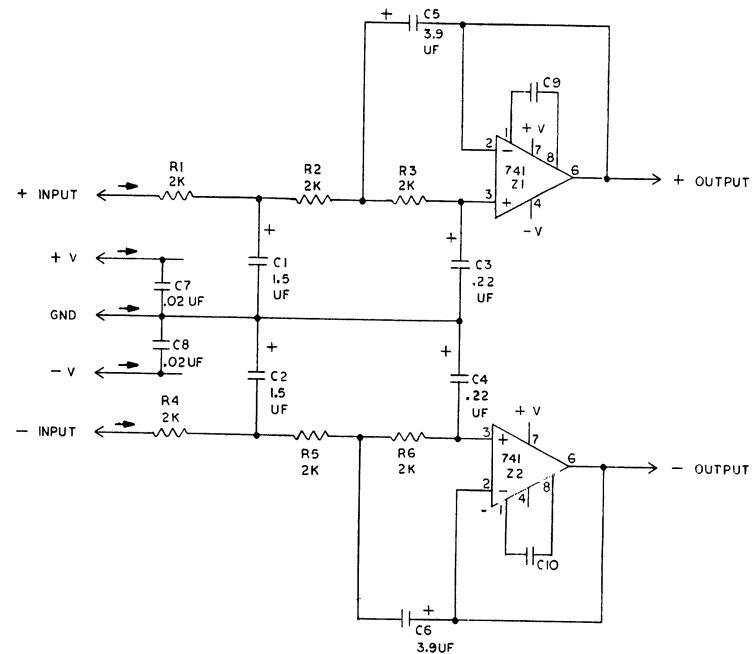


Figure 6-3. Mark-Space Bandpass Filter Schematic Diagram
D2817A

	-1	-2	-3	-4	-5	-6	-7
FREQ. (BAUD)	60/75	45/50	130	150	200	300	600
Z1, Z2	741	741	741	741	741	741	741
R1, 2, 3, 4, 5, R6	2K	3.01K	1K	2K	7810	.6490	3.5K11
C3, C4	.22MFD	.22MFD	.22uf	.15uf	.22uf	.22uf	.22uf
C5, C6	3.9MFD	3.9MFD	3.9uf	2.7uf	3.9uf	3.9uf	.39uf
C1, C2	1.5MFD	1.5MFD	1.5uf	1.0uf	1.5uf	1.5uf	.15uf
C7, C8	.02MFD	.02MFD	.02uf	.02uf	.02uf	.02uf	.02uf



NOTES

- 1 P.C BOARD REF NO1159
- 2 P.C BOARD ASSY REF D2813
- 3 ALL RESISTORS ARE 1/4 W 1%
- 4 WHEN Z1 & Z2 IS A 741 I.C, C9 & C10 IS NOT REQUIRED

Figure 6-4. Dual Low-Pass Filter Schematic Diagram
D2814G

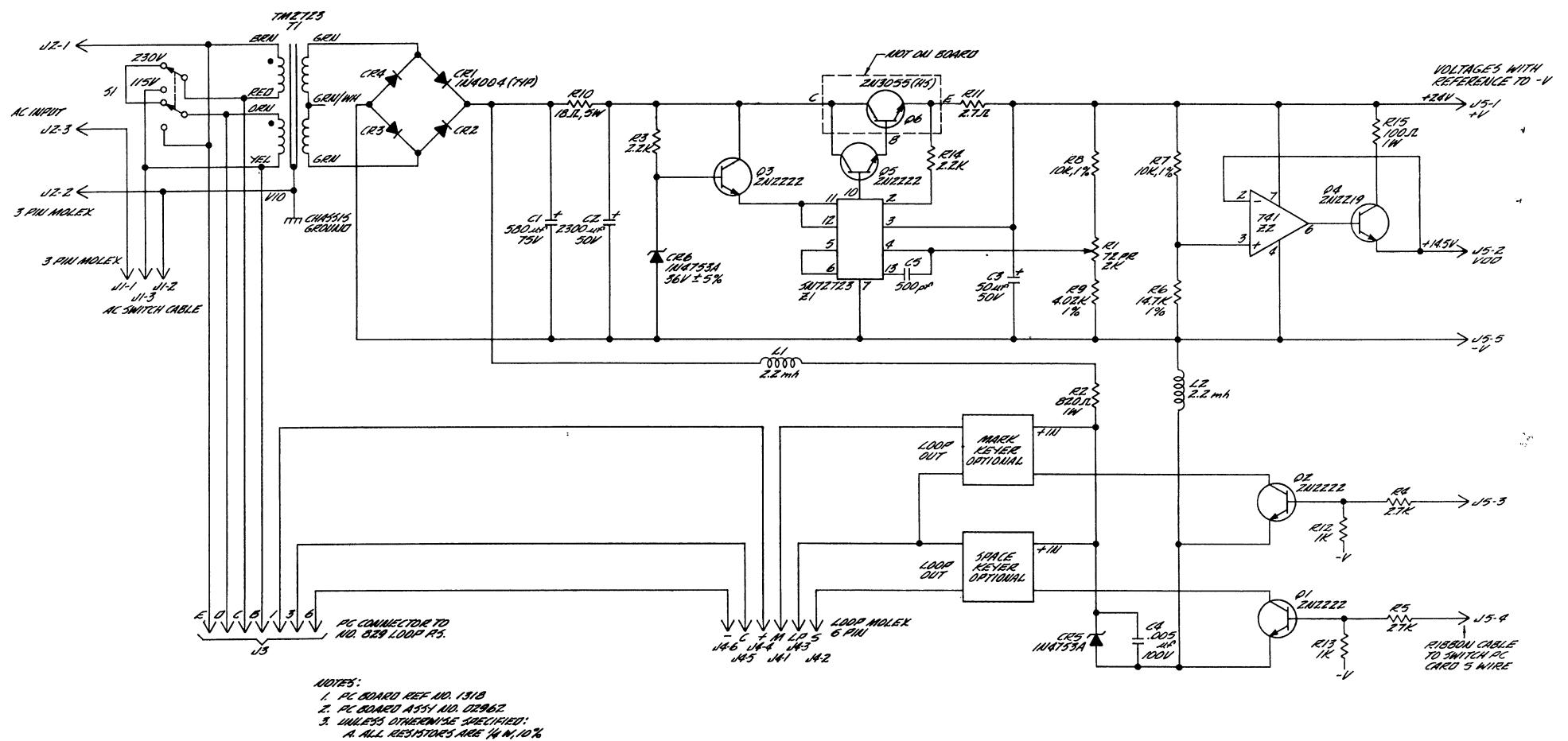


Figure 6-5. Power Supply Schematic Diagram
D2961C

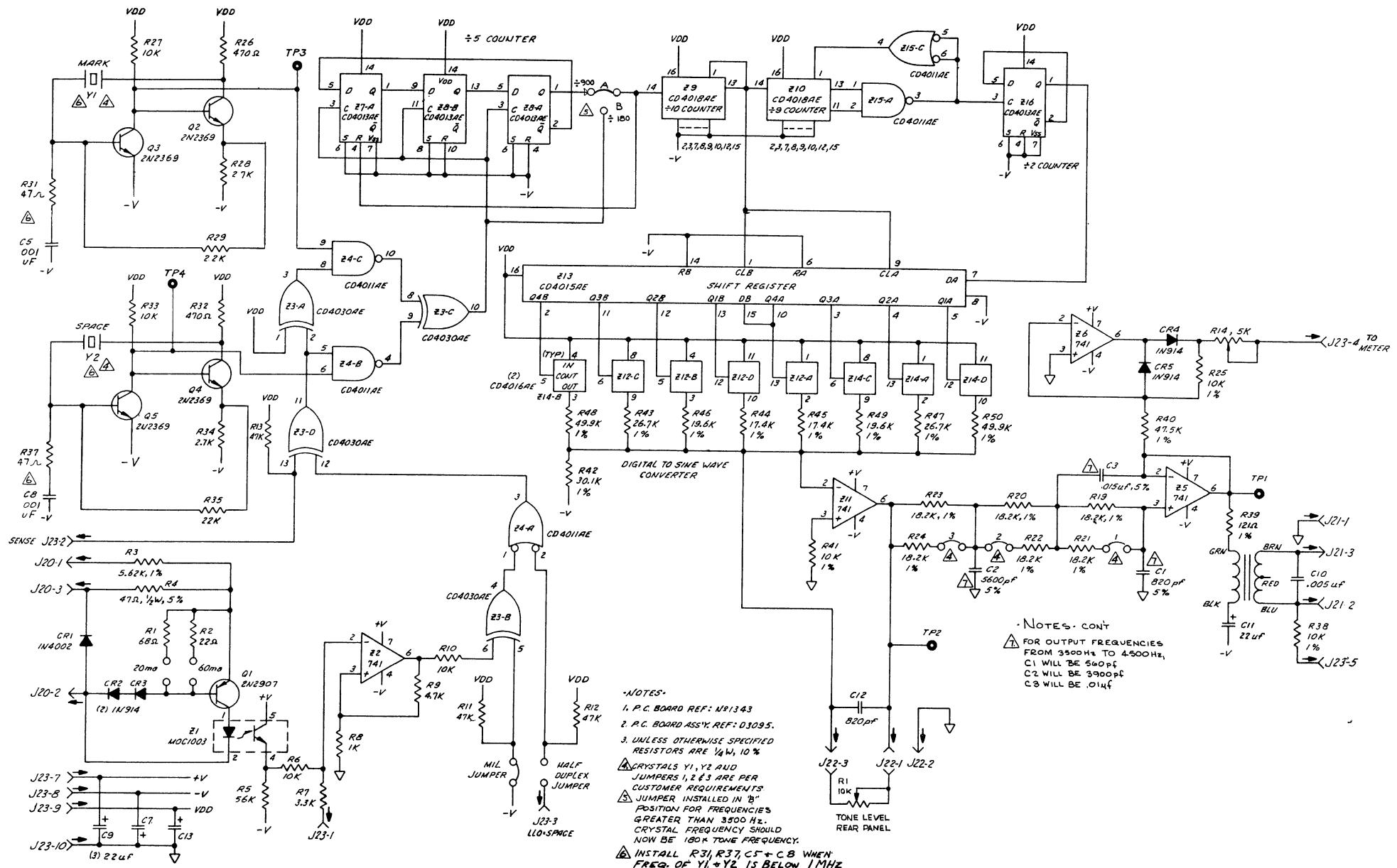
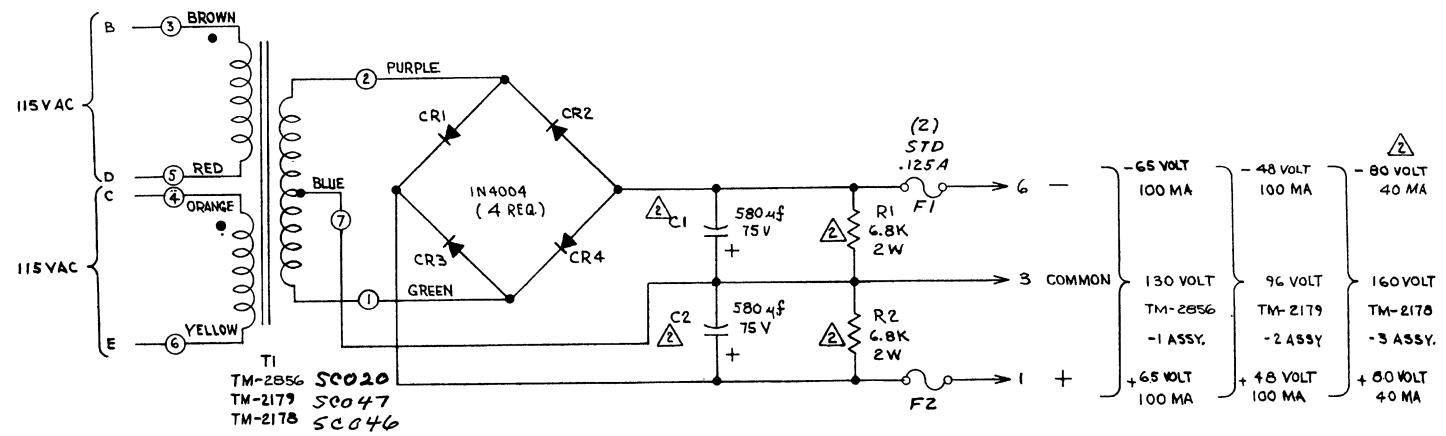


Figure 6-6. Tone Keyer Schematic Diagram
D3094C



NOTES:

1. REF. ASSY. C2324
2. ON - 3 ASSY. R1, R2 ARE 10K, 2W & C1, C2 ARE 300 MFD. 100 VOLT.
3. P.G. BOARD NO829

Figure 6-7. Optional Loop Power Supply Schematic Diagram
C2367C

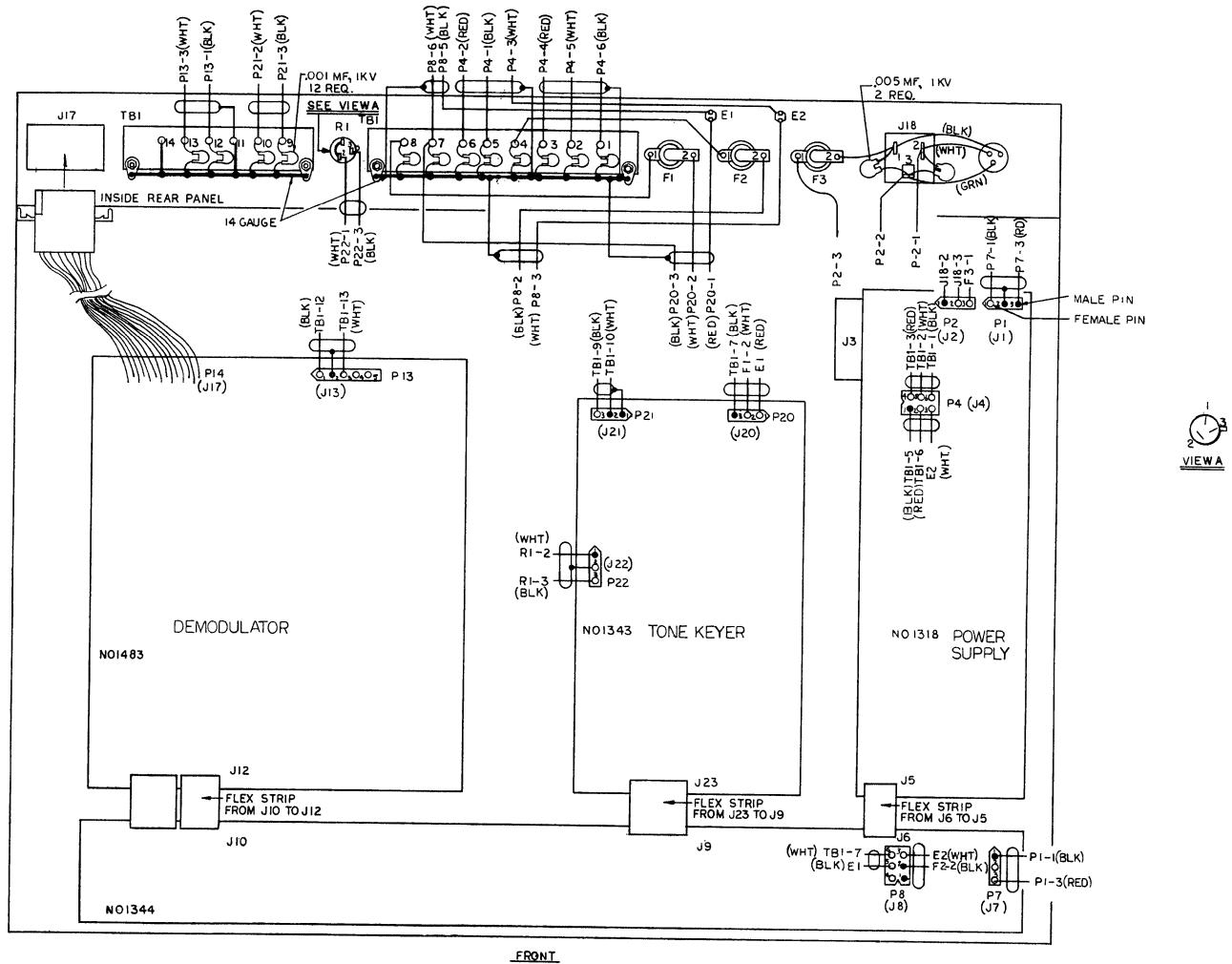


Figure 6-8. Model 1273 Wiring Diagram
D3150D

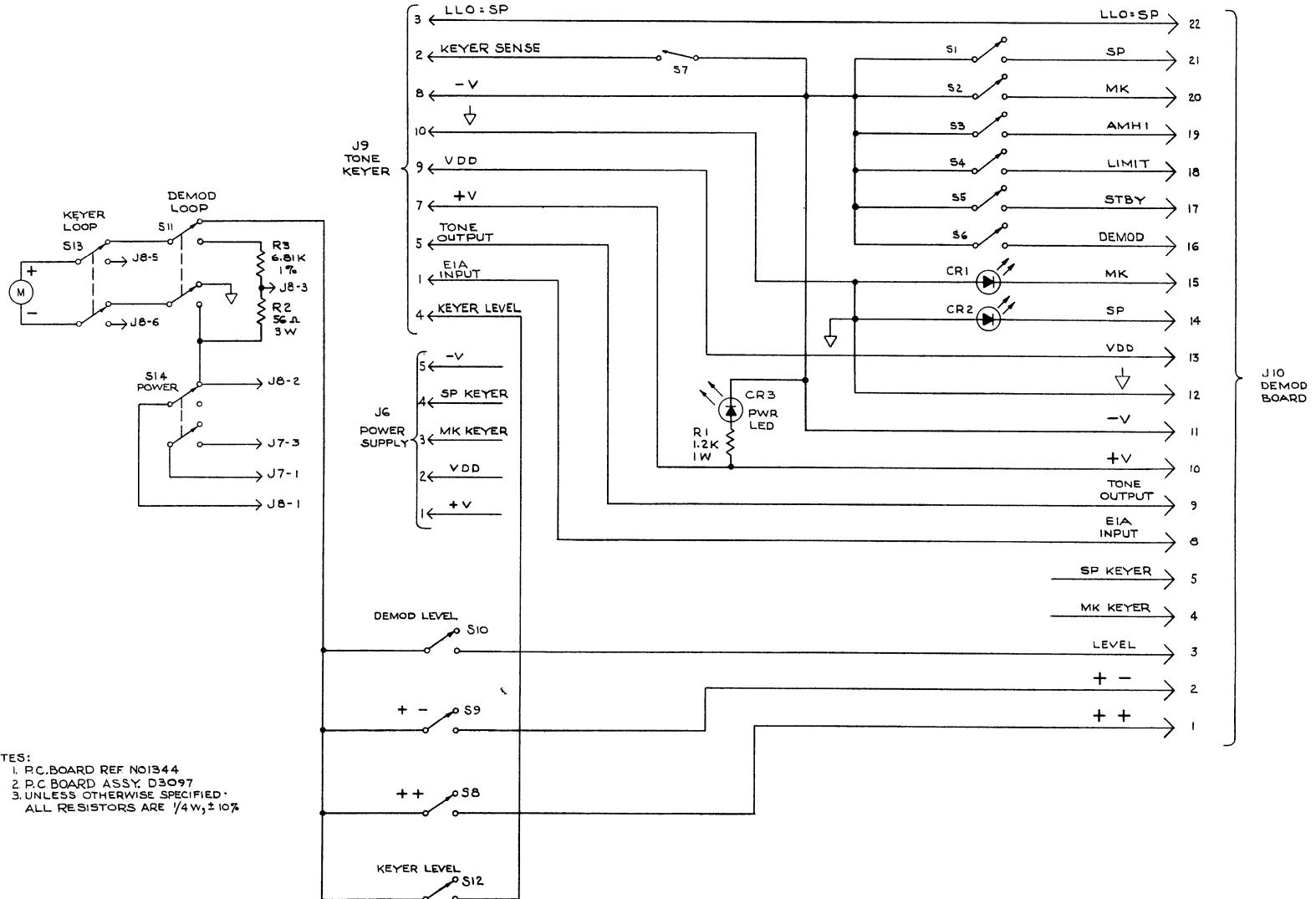
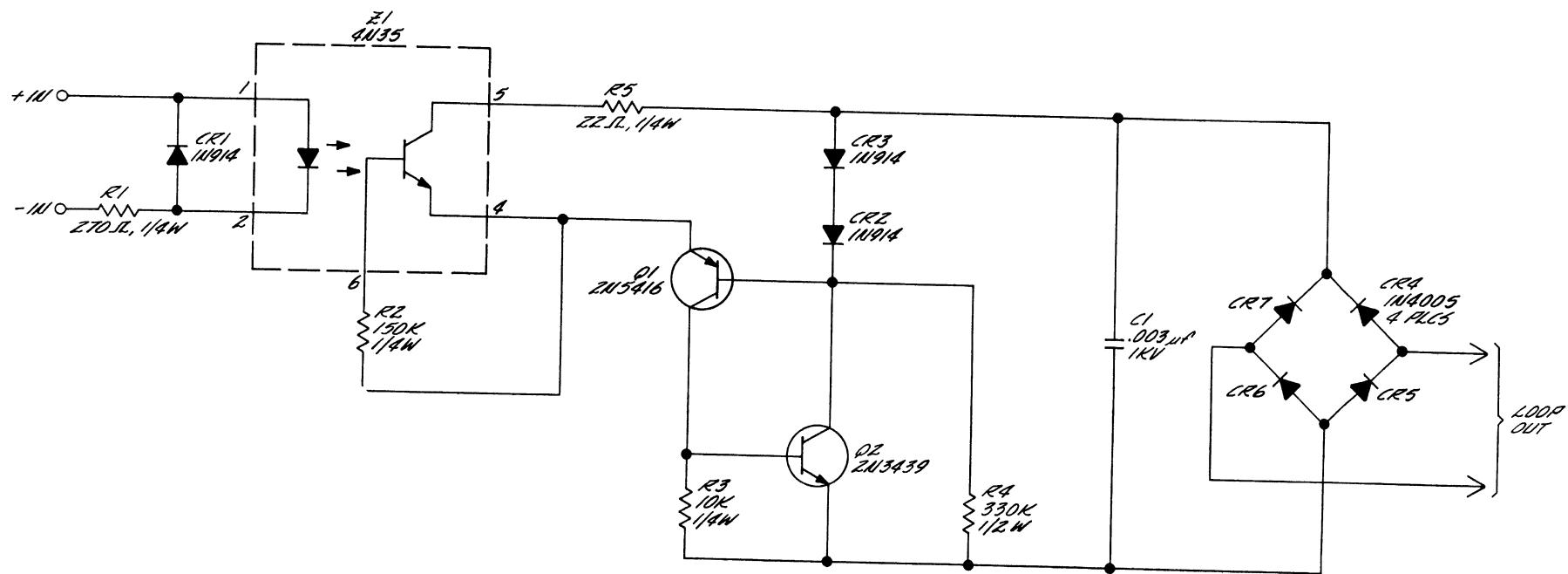


Figure 6-9. Front Panel Switch Schematic Diagram
D3096A



NOTES:

1. PC BOARD REF 101452
2. PC BOARD ASSY C3240

Figure 6-10 Optically Isolated High Level Neutral Keyer Schematic Diagram

C3308

SECTION VII
PART REPLACEMENT DRAWINGS

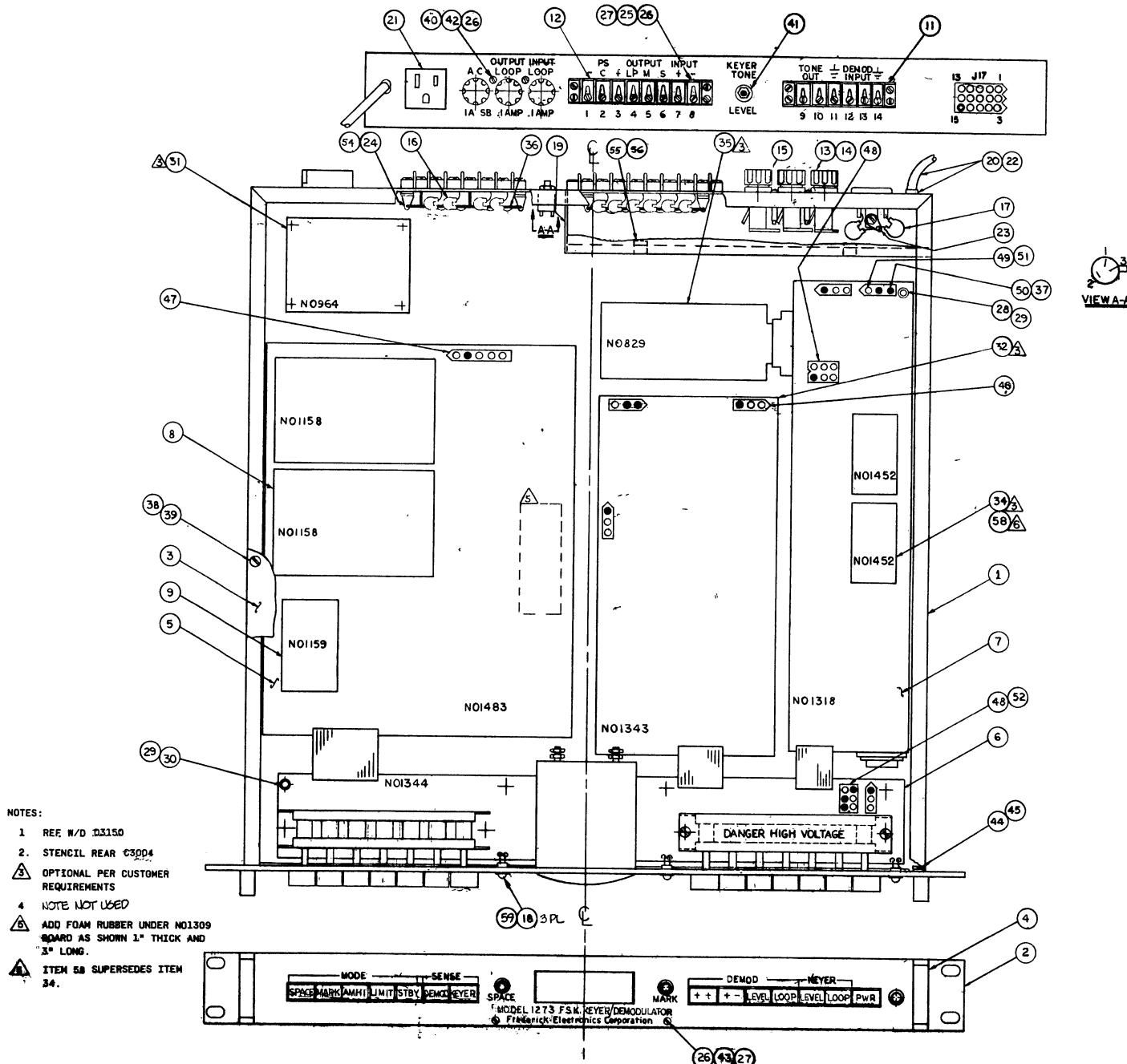


Figure 7-1. Model 1273 Assembly
D3162N

ITEM REQ'D	PART NO.	DESCRIPTION	MATL OR MFR	MATL SPEC OR CAT PART NO.	FINISH	FINISH SPEC	CRT SYM
59	3 040977	DIODE HOLDER	DIALCO	555-000Z			
58	2 C3240	ASSY HI-LEVEL KEYER	FEC	N01452			
57	1 C1470	CHASSIS SLIDE	FEC				
56	2	SCREW, 4-40x5/16 LG BD HD SST	SST	404203			
55	2 C15263-4Z-2	SPEED NUT	TINNERMAN	403170			
54	2 B1558	INSULATOR	FEC				
53	A/R	WIRE, 24 GA	ALPHA				
52	A/R	SHIELDED 3 COND. 24 GA	DELCO				
51	A/R	SHIELDED 2 COND. 24 GA	DELCO				
50	13 1560-TL8	PIN MALE	MOLEX	744400			
49	22 1561-TL8	PIN FEMALE		744410			
48	2 1625-6R1	CONNECTOR 6 PIN		246304			
47	1 1625-5R1	CONNECTOR 5 PIN		246301			
46	6 1625-3R1	CONNECTOR 3 PIN	MOLEX	246275			
45	4	WASHER NO 6 SPLIT LOCK	SS	404895			
44	4	SCREW, 6-32x3/8 FILLISTER HD SST	404375				
43	2	SCREW, 4-40x3/8 OVAL HD SST	SST	404213			
42	2	SCREW, 4-40x5/16 BD HD SST	SST	404203			
41	1 MAZL0405105UC	POTENTIOMETER	AB	627406			
40	2 750	STANDOFF, INSULATED	WINCHESTER	683014			
39	7	SCREW NO 6-32x5/16 FL HD UNDERCUT SST	404368				
38	7 C8020-632-6	SPEED NUT NO 6	TIMMERM	403180			
37	A/R SST1	CABLE TIES	PAN DUIT				
36	A/R	14 GAUGE COPPER WIRE	ALPHA				
35	1 C2324B	ASSY, LOOP POWER SUPPLY	FEC	N0829A			
34	2 C2434	ASSY, HI-LEVEL KEYER		N0982			
33	1 C310G	ASSY, DIVERSITY CABLE					
32	1 D3095	ASSY, TONE KEYER		N01343			
31	1 C2362	ASSY, HI-IMPEDANCE INPUT	FEC	N0964			
30	8	SCREW, 6-32x1/4 LG BD HD SS	404361				
29	31	WASHER NO 6 INT. TOOTH	SS	404893			
28	21	SCREW NO 6-32x5/16 LG BD HD SST	404369				
27	10	NUT HEX NO 4-40x1/4 AF SST	403030				
26	8	WASHER NO 4 INT. TOOTH		404878			
25	8	SCREW NO 4-40x1/2 LG BD HD SST	404220				
24	4 1416-4	SOLDER LUG NO 4	SMITH	242754			
23	1 1416-6	SOLDER LUG NO 6	SMITH	242756			
22	1 5P-4	STRAIN RELIEF	HEYCO	688025			
21	1 M1536GS	RECEPTACLE	CIRCLE F	247025			
20	1 17237	LNE CORD	BELDEN	366050			
19	1 C2989-2	REAR COVER	FEC				
18	3 FLV-112	LED	FAIRCHILD	040027			
17	2 DD502	CAPACITOR 005MF 1KV	CRL	021510			
16	12 801X5F102K	CAPACITOR 001MF 1KV	ERIE	021300			
15	2 312-100	FUSE 1/10 AMP	LITTLEFUSE	368050			
14	1 313-001	FUSE 1 AMP	LITTLEFUSE	368250			
13	3 342004	FUSEHOLDER	LITTLEFUSE	368425			
12	1 8-140-Y	BARRIER STRIP	C-J	100350			
11	1 6-140-Y	BARRIER STRIP	C-J	100300			
10	2 C3916	ASSY, BAND PASS FILTER	FEC				
9	1 D2813	ASSY, LOW PASS FILTER		N01159			
8	2 D2818	ASSY, BAND PASS FILTER		N01158			
7	1 D2962	ASSY, POWER SUPPLY		N01316			
6	1 D3097	ASSY, SWITCH		N01344			
5	1 D3759	ASSY, DEMODULATOR		N01483			
4	2 B1132	HANDLES		409030			
3	1 C3001	COVER					
2	1 D3090	ENGRAVING, FRONT PANEL					
1	1 D3092	CHASSIS	FEC				

Figure 7-1. Parts List

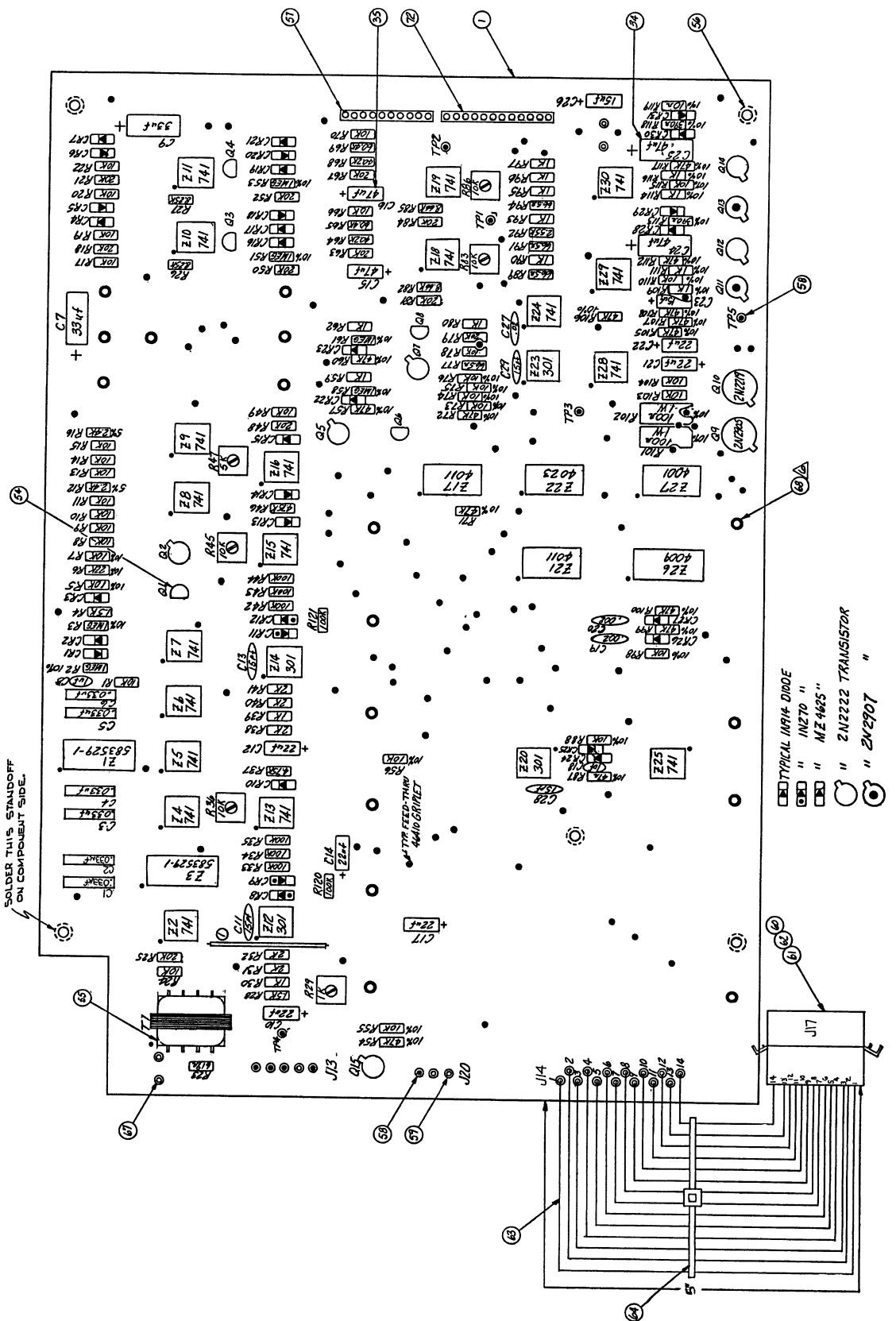


Figure 7-2. Demodulator Board Subassembly
D3739N

DEMODULATOR WIRE LIST (-1 ASSEMBLY ONLY)			
FROM	PIN TYPE	TO	PIN TYPE LENGTH(24 GA. WHT)
J14-1(N01483)	SOLDER PAD	J17-1	744300 5"
J14-2(N01483)	SOLDER PAD	J17-2	744300 5"
J14-3(N01483)	SOLDER PAD	J17-3	744300 5"
J14-4(N01483)	SOLDER PAD	J17-4	744300 5"
J14-5(N01483)	SOLDER PAD	J17-5	744300 5"
J14-6(N01483)	SOLDER PAD	J17-6	744300 5"
J14-7(N01483)	SOLDER PAD	P15-4	744300 5"
J14-8(N01483)	SOLDER PAD	J17-8	744300 5"
J14-9(N01483)	SOLDER PAD	J17-9	744300 5"
J14-10(N01483)	SOLDER PAD	P15-2	744300 5"
J14-11(N01483)	SOLDER PAD	J17-11	744300 5"
J14-12(N01483)	SOLDER PAD	J17-12	744300 5"
J14-13(N01483)	SOLDER PAD	J17-13	744300 5"
J14-14(N01483)	SOLDER PAD	J17-14	744300 5"
J17-7		P15-3	744300 8 1/4"
J17-10		P15-1	744300 8 1/4"
J17-15		P15-5	744300 8 1/4"
PAD A(N01483)	SOLDER PAD	J16-1	744400 9"
PAD B(N01483)	SOLDER PAD	J16-2	744400 6"
PAD C(N01483)	SOLDEK PAD	J16-3	744400 3"

NOTES:

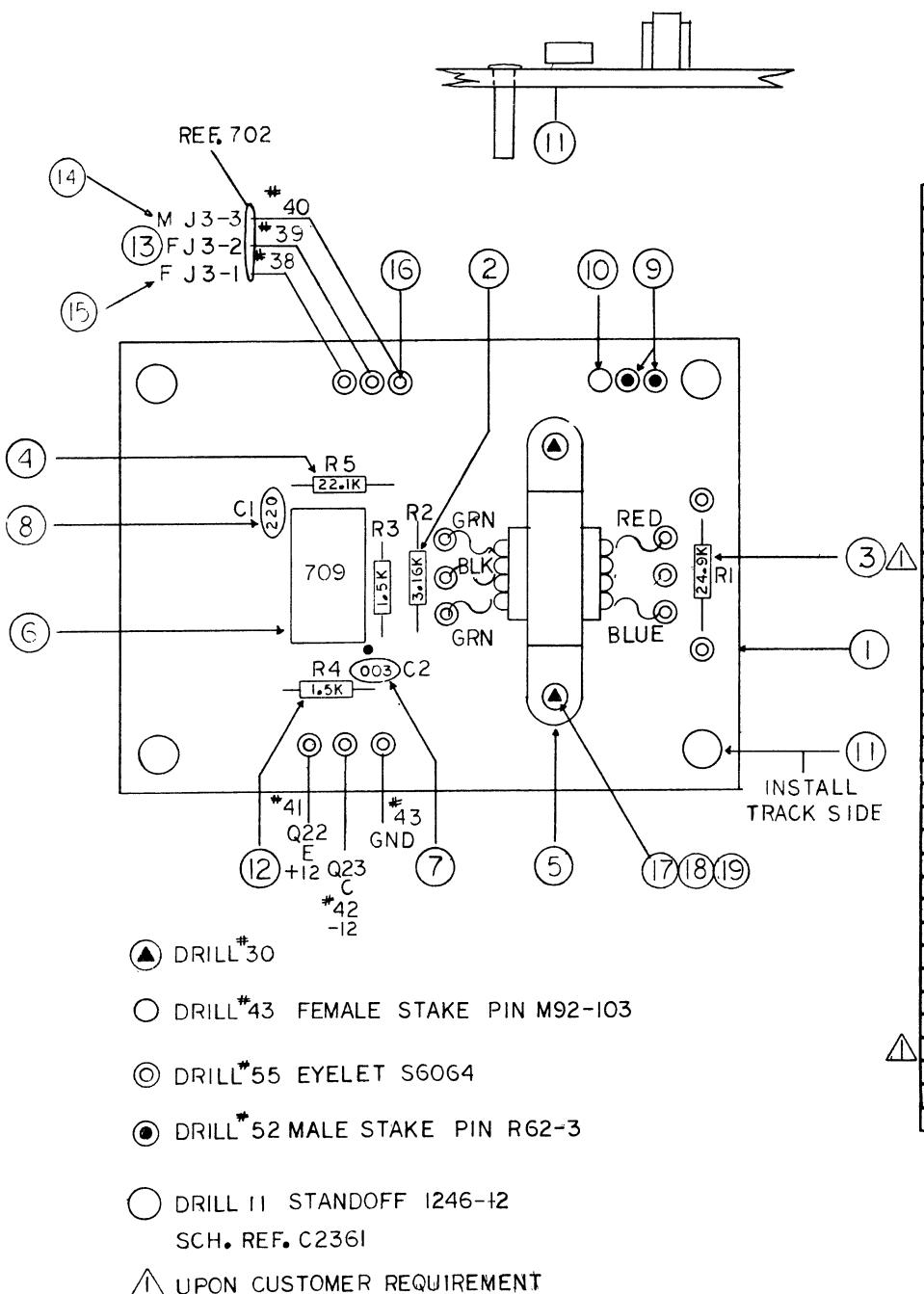
- 1 SCHEMATIC REFERENCE D3738
- 2 UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4W 1%
- 3 WIRE MOLEX RECEPTACLE PIN FOR PIN WITH PC BOARD USING 1380TL PINS PIN 15 WILL BE 1381TL AND REMAIN UNUSED
- △ RESISTOR VALUES REQUIRED FOR DWG. NO. ARE PROGRAMMED & WILL DEPEND ON CUSTOMER REQUIREMENTS.
- △ ITEMS 69 & 71 USED IN ACCORDANCE WITH CUSTOMER REQUIREMENTS AND/OR SPECIFICATIONS.
- △ AFTER INSTALLATION OF ITEM NO. 68, SOLDER EYELET IN PLACE.

I	-	76	5HKS10	CAPACITOR .01MF 1KV	SPRAGUE	021570		
I	-	75	1261P-1	RECEPTACLE 6 PIN	MOLEX	246012		
3	-	74	02062103	PIN, MALE	MOLEX	744400		
I	-	73	1625-3R1	RECEPTACLE 3 PIN	MOLEX	246275		
I	-	72	583773-4	12 POSITION DIP. RECEPTACLE	AMP	248732		
I	-	71	D2813	LOW PASS FILTER	FEC			
A	-	70	D4029	PROGRAMMABLE RES. CHIP	FEC			
A	-	2	69	D2818	BAND PASS FILTER	FEC		
A	-	17	68	A919	EYELET	US		
A/R	A/R	66	56064	EYELET	US			
A/R	A/R	66	46410	GRIPPLET	BERG			
I	-	65	J1.375X0.250T22	JUMPER 1.375	SQ. EL.	3666557		
I	-	64	5571	TIE WIRE	PANDUIT	184750		
A/R	A/R	63		WIRE 24 GA. WHITE	ALPHA			
I	-	62	1380TL	TERMINAL (FEMALE)	MOLEX	744325		
I	-	14	61	1380TL	TERMINAL (MALE)	MOLEX	744300	
-I	-	ITEM	PART NO.	DESCRIPTION	MFR	CAT. NO.		

I	I	60	1375R	RECEPTACLE	MOLEX	246125		
3	3	59	M93-102ET	STAKE-PIN (FEMALE)	B. CHAIN	744555		
10	10	58	R62-3ET	STAKE-PIN (MALE)	B. CHAIN	744550		
I	I	57	1-583773-3	10 POSITION DIP RECEPTACLE	AMP	248731		
5	5	56	1246-12	STANDOFF	CTC	683182		
I	I	55	PC-SO-21	TRANSFORMER	UTC	765033		
5	5	54	2N5461	TRANSISTOR	MOT	080835		
I	I	53	2N2905		MOT	080520		
I	I	52	2N2219		MOT	080469		
2	2	51	2N2907		MOT	080522		
6	6	50	2N2222	TRANSISTOR	NAT	080467		
2	2	49	583529-1	SOCKET	AM	248106		
I	I	48	CD4023A	INTEGRATED CIRCUIT	RCA	061220		
2	2	47	CD4011A		RCA	061180		
I	I	46	CD4009A		RCA	061170		
I	I	45	CD4001A		RCA	061175		
I	I	44	LH741CN		NAT	060140		
4	4	43	LM301CN	INTEGRATED CIRCUIT	NAT	060080		
4	4	42	HZ4625	DIODE	MOT	040661		
23	23	41	IN914	DIODE	GE	040238		
4	4	40	IN270	DIODE	TI	040044		
I	I	39	RH6001080E	RESISTOR 100 1/4W 1%	CORNING	624005		
2	2	38	150D156X9020B2	CAPACITOR 15MF 20V	SPRAGUE	026572		
I	I	37	5835YSU203Z	.02MF 25V	ERIE	021550		
I	I	36	C3301C105MSU1CA	1MF 50V	KEMET	029940		
2	2	35	150D476X9006B2	47MF 6V	SPRAGUE	028704		
2	2	34	150D476X9020B2	47MF 20V	SPRAGUE	028726		
2	2	33	150D338X9020B2	.33MF 20V	SPRAGUE	028660		
6	6	32	150D226X9015B2	.22MF 15V	SPRAGUE	028594		
6	6	31	BP28533J	.033MF 100V	IMB	029045		
		30						
4	4	29	DD150		15pf 1KV	CRL	021020	
2	2	26	DD022	CAPACITOR .002MF 1KV	CRL	021360		
I	I	27	T2PR1K	POTENTIOMETER 1K	BECKMAN	627134		
4	4	26	T2PR10K	POTENTIOMETER 10K	BECKMAN	627415		
I	I	25	T2PR5K	POTENTIOMETER 5K	BECKMAN	627325		
8	8	24	RN55D1003F	RESISTOR 100K 1/8W 1%	CORNING	625811		
4	4	23	RN60D66GRSF	.66.50 1/4W 1%		624043		
2	2	22	RN55D6042F	.60.4K 1/8W 1%		625750		
2	2	21	4022F	40.2K		625673		
11	11	20	2002F	20K		625505		
19	19	19	1002F	10K		625270		
2	2	18	8661F	8.66K		625233		
2	2	17	8251F	8.25K		625209		
2	2	16	4751F	4.75K		624879		
5	5	15	2001F	2K		624481		
2	2	14	1501F	1.5K		624399		
10	10	13	1001F	1K		624299		
I	I	12	RN55D190F	61.90 1/8W 1%	CORNING	624181		
2	2	11	RC32GF101K	1000 1W 10%	AB	606175		
2	2	10	RC07GF242J	2.4K 1/4W 5%	AB	601336		
I	I	9	RN60D2551F	2.55K 1/4W 1%	CORNING	624580		
2	2	8	RC07GF391K	3900 1/4W 10%	AB	602312		
6	6	7	105K	1 MEG		602792		
13	13	6	473K	47K		602635		
I	I	5	223K	22K		602588		
12	12	4	103K	10K		602540		
4	4	3	102K	1K		602372		
I	I	2	RC07GF470K	RESISTOR 470 1/4W 10%	AB	602180		
I	I	1	NO1483A	PC BOARD	FEC			
-I	-I	ITEM	PART NO.	DESCRIPTION	MFR	MATERIALS OR CAT PART NO.	FINISH	FINISH SPEC
						CAT SYM		

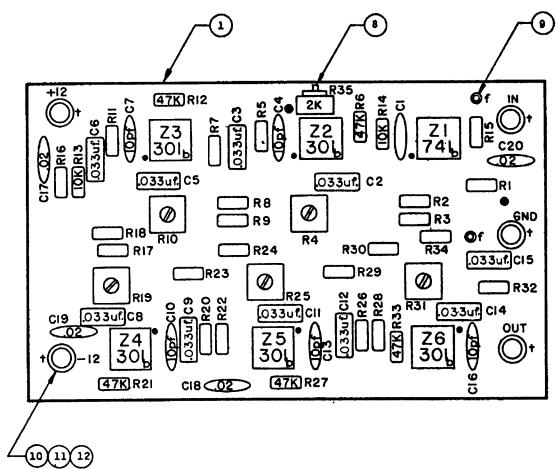
LIST OF MATERIAL

Figure 7-2. Parts List



ITEM	REQ'D	PART NO.	DESCRIPTION	MATL OR MFR	MATL SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
19	2	4-40x1/4AF	NUT		SS			
18	2	*4	WASHER		SS			
17	2	4-40x1/4	SCREW		SS			
16	14	S6064	EYELET	STIMPSON				
15	2	1561	FEMALE PIN					
14	1	1560	MALE PIN					
13	1	1625-3R1	3 PIN MOLEX PLUG	MOLEX				
12	2	1.5K 1/4W 10% RESISTOR	R1	A B				
11	4	I246-12	STANOFF	CTS				
10	1	M92-103	FEMALE STAKE PIN	BEAD CHAIN				
9	2	RG2-3	MALE STAKE PIN	BEND CHAIN				
8	1	JF220Z5F	220PF 1KV DISC.	PMC				
7	1	DD302	.003MFD 1KV DISC.	CRL				
6	1	SN72709N	INTEGRATED CIRCUIT	T I				
5	1	TY26X	TRANSFORMER	TRIAD				
4	1		22.1K 1% 1/4W RESISTOR	CORNING				
3	1		24.9K					
2	1		3.16K					
1	1	N0964	P.C. BOARD	FEC				

Figure 7-3. High Impedance Input Board Subassembly
C2362

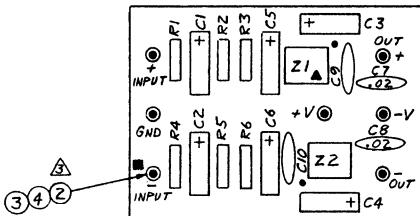


NOTES:

1. SCHEMATIC REFERENCE D2817
 2. INSTALL STANDOFFS ON COMPONENT SIDE OF BOARD AND SOLDER ON TRACK SIDE ONLY
 3. SG301AM AND LM748CN ARE INTERCHANGEABLE
 4. DRILL & SHEARING INFORMATION CALLED OUT ON SR# SHEET OF NO1158
 5. ALL STANDOFFS MUST BE SOLDERED SHUT ON TRACK SIDE OF BOARD.

ITEM	REF ID	QTY	DESCRIPTION	MANUF.	TYPE	CAT. PART NO.	PIN#	PIN# SPEC	CAT. EXP.
13	10	029045	CAP 033uF 100V 5%	I.M.B.	BP2B33S1				
12	5	246321	BANANA PLUG	SMITH		192			
11	5	.404861	WASHER NO.2 SPLIT LOCK	TAC					
10	6	685842	STANDOFF	CTC		2168-14			
9	2	247065	MINX INSERT	AMP		2332172-1			
8	1	627220	POTENTIOMETER 2K	BECKMAN		T2KNR2K			
7	2	625270	RESISTOR 10K 1/4W 1%	CORNING		NR5501002F			
6	6	602636	RESISTOR 47K 1/4W 10%	AB		RC076F47K3K			
5	1	060140	INTEGRATED CIRCUIT	TI		LTM471CN			
4	5	060080	INTEGRATED CIRCUIT	SIG		S6302AN			
3	4	021580	CAPACITOR 02uf 25V	ERIE		6835Y02W[20Z]			
2	6	021010	CAPACITOR 10pf 1KV	CRL		DO-100			
1	1	NO11568	PC BOARD	FEC					
ITEM	REF ID	QTY	DESCRIPTION	MANUF.	TYPE	CAT. PART NO.	PIN#	PIN# SPEC	CAT. EXP.

Figure 7-4. Mark-Space Bandpass Filter Board Subassembly
D2818D



NOTES :

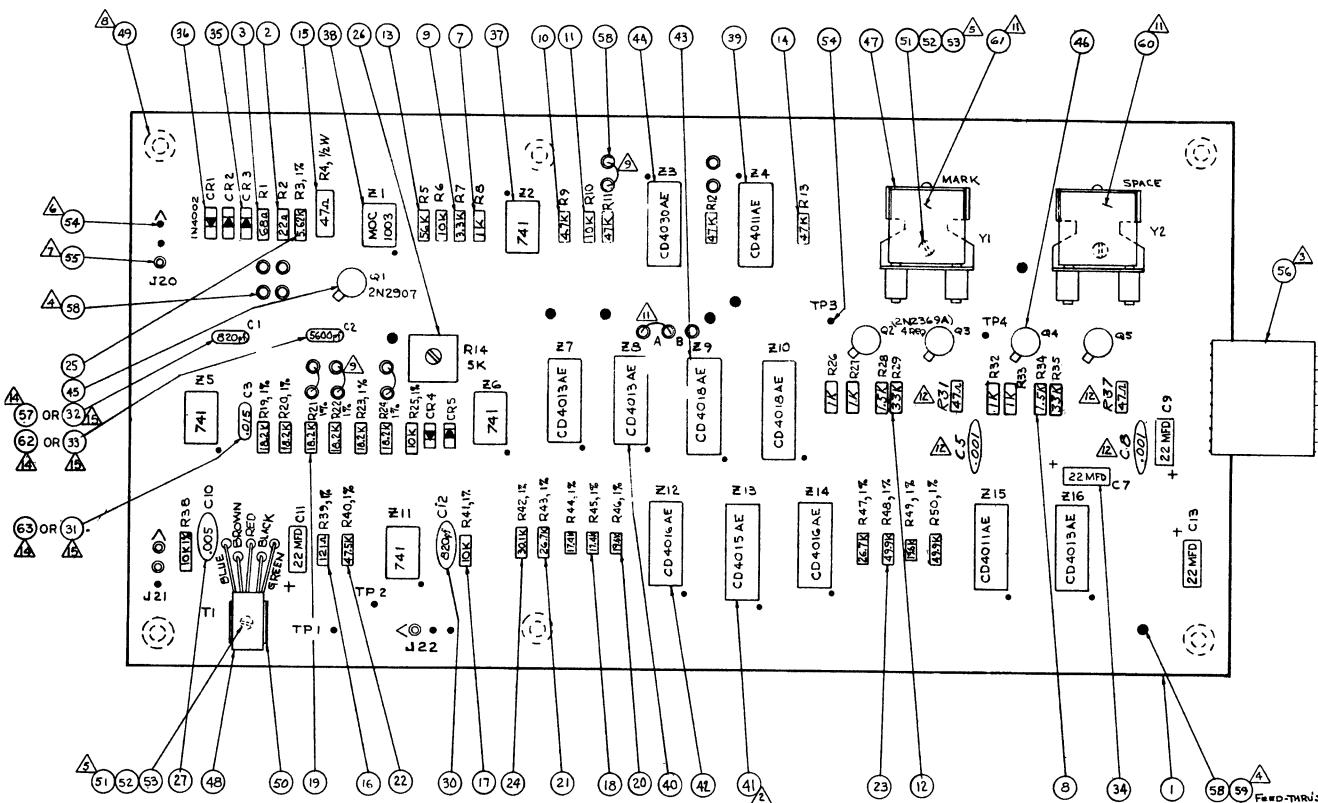
- 1 SCHEMATIC REF D2814
 - 2 UNLESS OTHERWISE NOTED DRILL MOUNTING HOLES
NO 55 (.052) DIA & INSTALL 46410 GRIPPLETS
 - ▲ NO 68 (.031) DR - AS REQUIRED FOR ITEM 11
 - NO 30 (.128) DR - 7 PLACES FOR ITEM 2
 - 3  INSTALL ITEM 2 ON COMPONENT SIDE OF BOARD &
MOUNT ITEMS 3 & 4 AS REQUIRED ALSO SOLDER
ITEM 2 TO BOARD
 - 4 DO NOT CRIMP CARK ON PC BOARD.

OUTPUT

Figure 7-5. Dual Low-Pass Filter Board Subassembly
D2813G, Sheet 1

300 BAUD										
R123456	6			40	RC076F332J	RESISTOR 3.3KΩ 1/4W 5%	ALLEN-BRADLEY	601384		
C1.2	2			39	154-K0MEP5001-1	CAPACITOR .15uF DOV 5%	PAKTRON	028010		
C3.4	2			38	150012290025A2	CAPACITOR 22uF 35V 10%	SPRAGUE	028013		
C5.6	2			37	MPC-033	CAPACITOR 39uF DOV 5%	PAKTRON	028950		
R1.2,3,4,5,6.				6	RN52061390F	RESISTOR 619Ω 1/4W 1%	CORNING	624181		
				35	RN52071870F	RESISTOR 787Ω 1/4W 1%	CORNING	624332		
				34	15001054091B2	CAPACITOR 1uF 15V	SPRAGUE	028176		
				33	1500275X903B2	CAPACITOR 2.7uF 35V	SPRAGUE	028374		
				32	1500154X093B2	CAPACITOR 15uF 35V	SPRAGUE	028044		
				31	RN5601001F	RESISTOR 1K 1/4W 1%	CORNING	624299		
				30	RN5603011F	RESISTOR 3.0K 1/4W 1%	CORNING	624613		
ZL2	2	Z1.2		2	29	LH741CN	INTEGRATED CIRCUIT	NAT.	060140	
				28	RN5602001F	RESISTOR 2K 1/4W 1%	CORNING	624481		
				27	1500224X901B2	CAPACITOR 22uF 15V	SPRAGUE	028066		
				26	1500395X902B2	CAPACITOR 3.9uF 20V	SPRAGUE	028400		
				25	1500155X903B2	CAPACITOR 1.5uF 35V	SPRAGUE	028264		
C7.8	2	C7.8		2	24	5835Y5U203Z	CAPACITOR .02uF 25V	ERIE	021580	
A/R				A/R	23	46410	GRIPLET	BERG		
				7	22		WASHER NO.2 SPLIT LOCK	SST	404861	
				7	21	192	BANANA PLUG	SMITH	246321	
				7	20	2188-14	STANDOFF	CTC	683842	
600 BAUD				1	300 BAUD	1	N01159	P.C. BOARD	FEC	
ITEM REOD PAR. NO. DESCRIPTION MATEL OR MFR MATEL SPEC OR CAT PART NO FINISH FINISH SPEC CKT BY										
-12	-11	-10	-9	-8	-7	-6				

Figure 7-5. Dual Low-Pass Filter Board Subassembly
D2813G, Sheet 2



NOTES:

1. REF SCHEMATIC D3094
2. DRILL INTEGRATED CIRCUITS NO 68 (.031) DR
3. DRILL NO 68 (.031) OR INSTALL ANSLEY RIBBON CABLE
4. DRILL NO 55 (.052) DR FOR GRIPPLETS
5. DRILL NO 38 (101) DR CRYSTAL HOLDER & TRANSFORMER CLAMP
6. DRILL NO 52 (.063) DR MALE STAKE PIN & TP'S
7. DRILL NO 43 (.089) DR FEMALE STAKE PIN
8. DRILL NO 11 (.191) DR STANDOFFS
9. JUMPERS SHOWN ARE FOR STANDARD BOARD
10. CRYSTALS AND JUMPERS ARE PER CUSTOMER SPECIFICATIONS
(CRYSTAL FREQUENCY IS 900 TIMES OUTPUT TONE FREQUENCY)

JUMPER TO BE INSTALLED IN "B" POSITION FOR FREQUENCIES GREATER THAN 3500HZ
CRYSTAL FREQUENCY SHOULD NOW BE 180X TONE FREQUENCY

Y1 - MARK CRYSTAL IS 900 TIMES MARK TONE FREQUENCY FOR
TONES LESS THAN 3500 Hz, 180 TIMES FOR MARK TONES
GREATER THAN 3500 Hz

Y2 - SPACE CRYSTAL IS 900 TIMES SPACE TONE FREQUENCY FOR
TONES LESS THAN 3500 Hz, 180 TIMES FOR SPACE TONES
GREATER THAN 3500 Hz

IF MARK AND SPACE TONES FALL ON BOTH SIDES OF 3500 Hz, SEE
ENGINEERING FOR ORDERING INFORMATION

BELLOW 1MHz ORDER "SL" CUT CRYSTAL, HC-6/U CASE, RESONANCE
SERIES 2 01X TOL AND INSTALL R31, R37, C5, AND C8

CD4000 SERIES INTEGRATED CIRCUITS REQUIRE SPECIAL HANDLING
DO NOT REMOVE FROM SHIPPING CONTAINERS UNTIL INSTALLED IN BOARDS

FOR OUTPUT FREQUENCIES FROM 3500 Hz TO 4500 Hz, USE ITEMS 57, 62 & 63

ITEMS 31, 32 & 33 ARE STANDARD AND SHOULD BE INSTALLED UNLESS
OTHERWISE SPECIFIED BY THE WORK AUTHORIZATION.

Figure 7-6. Tone Keyer Board Subassembly
D3095D

ITEM	REQ'D	PART NO.	DESCRIPTION	MATEL OR SPEC	MATEL SPEC OR CAT. PART NO.	FINISH	FINISH SPEC
63	1	12FR103-1C	CAPACITOR 0.1uf	MIDNEC	029042		
62	1	12FR3592-1C	CAPACITOR 0.039uf	MIDNEC	029875		
61	1	D2400	1 FREQ TOLERANCE * 005% 2 CASE - HC-6/U	3 CUT - AT 4. RESONANCE - SERIES	5. MAX Z - 5000		
60	1	D2400	1 FREQ TOLERANCE * 005% 2 CASE - HC-6/U	3 CUT - AT 4. RESONANCE - SERIES	5. MAX Z - 5000		
59	A/R		WIRE JUMPER	ALPHA			
58	24	S6084	EYELETS	U.S.			
57	1	DM18561J	CAPACITOR 560nf	ELMENCO	026715		
56	1	100F401S2A	10 RIBBON CABLE	ANSLEY	356008		
55	4	M93-103SET	STAKE PTN, FEMALE	BEADCHAIN	744555		
54	9	R62-3ET	STAKE PTN, MALE	BEADCHAIN	744550		
53	3		NUT, HEX 2-56x3/16 AF	SS	403010		
52	3		WASHER, NO 2 SPLIT LOCK	SS	404861		
51	3		SCREW, 2-56x3/16 BD HD	SS	404010		
50	1	6010-16	CLAMP	AUGAT	184450		
49	6	1246-12	STANDOFF	CTC	683182		
48	1	I-DO-T122	TRANSFORMER	UTC	765009		
47	2	8000-AG3	SOCKET	AUGAT	305520		
46	4	2N2369A	TRANSISTOR	NAT	080470		
45	1	2N2907	TRANSISTOR	HOT	080522		
44	1	CD4030AE	INTEGRATED CIRCUIT	RCA	061240		
43	2	CD4018AE			061210		
42	2	CD4016AE			061195		
41	1	CD4015AE			061190		
40	3	CD4013AE			061185		
39	2	CD4011AE			061180		
38	1	MOC1003		HOT	060445		
37	4	LM741CN	INTEGRATED CIRCUIT	NATIONAL	060140		
36	1	IM4002	DIODE	HOT	040550		
35	4	1N914	DIODE	GE	040238		
34	4	150D226X9015B2	CAPACITOR 22MF 15V	SPRAGUE	028594		
33	1	DM-19-562J	CAPACITOR 5600nf 500V	ELMENCO	026885		
32	1	DM-19-821J	820nf 500V	ELMENCO	026735		
31	1	1MD-1-153J	015MF 100V	ELMENCO	024506		
30	1	JF82025F	820pf 1KV DISC	AMC	021270		
29	2	8Q1X5F102K	CAPACITOR .001uf JKV	ERIE	021300		
28	2	RC076FA70K	RESISTOR 470 1/4W ±10%	AB	602636		
27	1	835X5V502Z	CAPACITOR 005WFD 100V DTC	ERIE	021480		
26	1	T72PR5K	POTENTIOMETER 5K	BOURNS	627325		
25	1	RN60D5621F	RESISTOR 5.62K 1/4W ±1%	CORNING	625036		
24	1	3012F	30 1K		625620		
23	2	4992F	49 9K		625720		
22	1	4752F	47 5K		625702		
21	2	2672F	26 7K		625595		
20	2	1962F	19.6K		625487		
19	6	1822F	18 2K		625468		
18	2	1742F	17 4K		625450		
17	3	1002F	10K		625288		
16	1	RN60D1210F	RESISTOR 1210 1/4W ±1%	CORNING	624086		
15	1	RC20GF470K	RESISTOR 470 1/2W ±10%	AB	604175		
14	3	RC07GF473K	47K 1/4W ±10%		602836		
13	1	563K	56K		602648		
12	2	333K	33K		602612		
11	2	103K	10K		602540		
10	1	472K	4.7K		602492		
9	1	332K	3.3K		602468		
8	2	152K	1.5K		602396		
7	5	102K	1K		602372		
6							
5							
4							
3	1	680K	680		602204		
2	1	RC07GF220K	RESISTOR 220 1/4W ±10%	AB	602132		
1	1	NO1343B	PC BOARD	FEC	602132		

LIST OF MATERIAL

Figure 7-6. Parts List

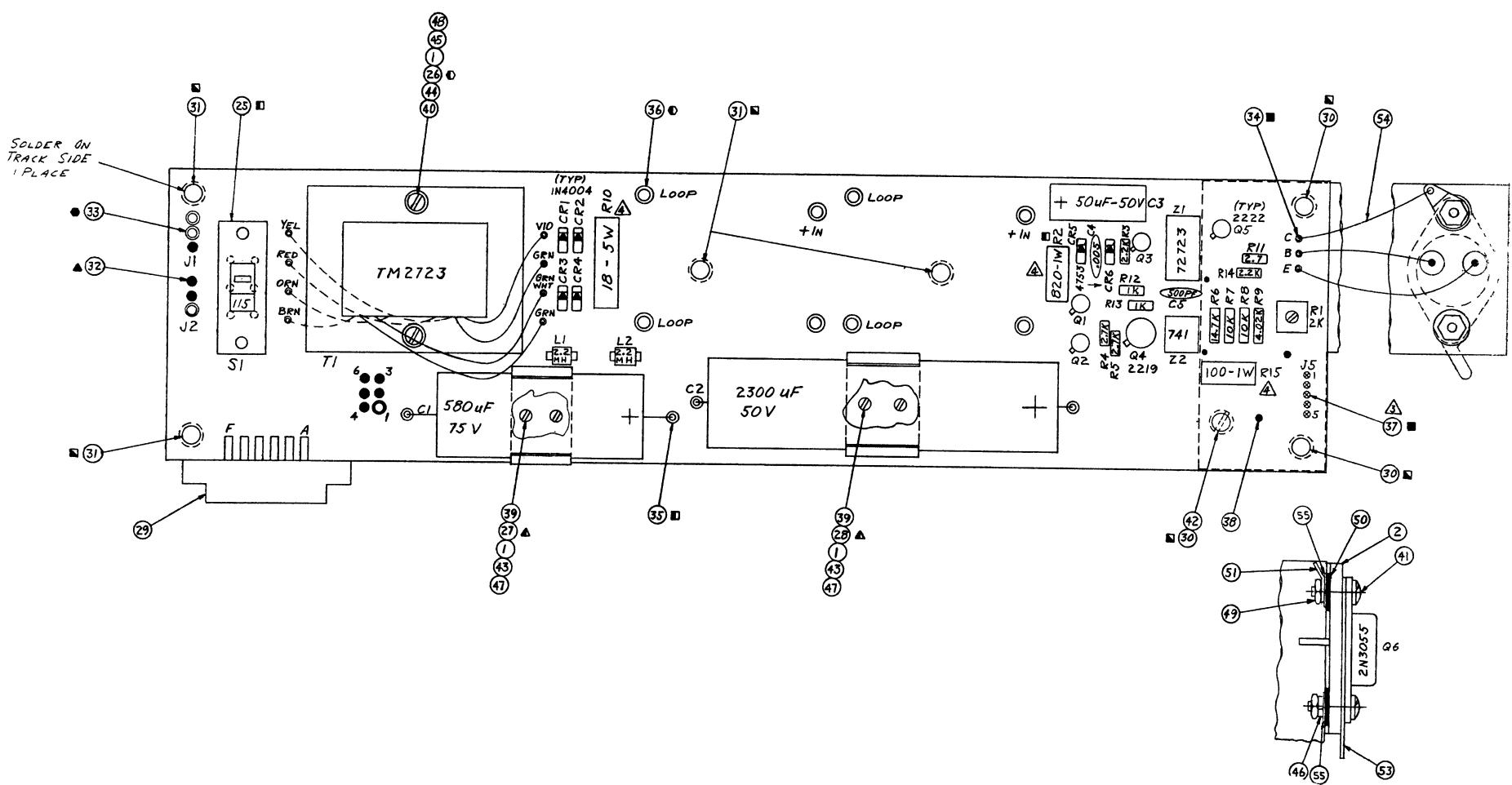


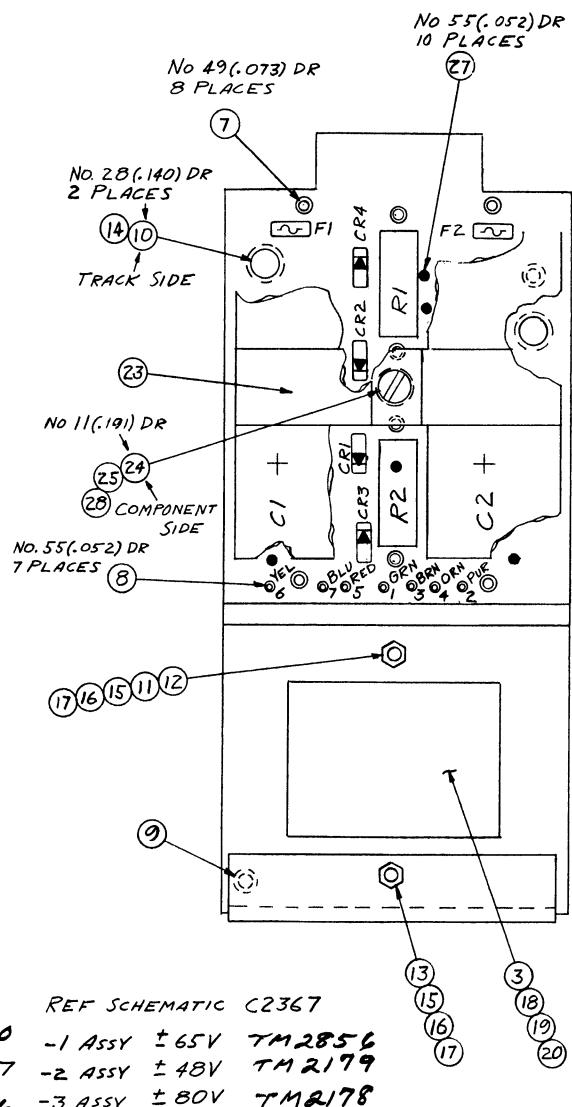
Figure 7-7. Power Supply Board Subassembly
D2962C

NOTES:

- 1 SCHEMATIC REF. D2961
 - 2 UNLESS OTHERWISE NOTED DRILL ALL HOLES
NO 55 (052) DR & INSTALL 46410 GRIPLET
INT CIR 'S REQUIRE NO 68 (031) DR
 - NO 65 (052) DR - 5 PLACES FOR ITEM 37 AND
11 PLACES FOR ITEM 34
 - ▲ NO 51 (087) DR - 8 PLACES FOR ITEM 32
 - NO 43 (089) DR - 4 PLACES FOR ITEM 33
 - NO 49 (073) DR - 6 PLACES FOR ITEM 25, 4 PLACES FOR ITEM 35 &
2 PLACES FOR ITEM 11
 - ▲ NO 38 (101) DR - 4 PLACES FOR ITEMS 27 & 28
 - NO 30 (128) DR - 2 PLACES FOR ITEM 26 AND
8 PLACES FOR ITEM 36
 - NO 11 (191) DR - 3 PLACES FOR ITEM 30 AND
4 PLACES FOR ITEM 31
- ⚠** INSTALL ITEM 37 BEFORE ASSEMBLY.
INSTALL ITEMS 32 & 33 (STAKE PIN) BEFORE ITEMS 30 & 31 (STANDOFF).
- ⚠** ITEMS 10, 11 AND 56 TO BE RAISED 1/8 ABOVE BOARD PRIOR TO SOLDERING.

ITEM NO	PART NO	DESCRIPTION	QTY	MANUFACTURER	CAT. NO.	FINISH	FINISH SPEC	CAT. SYM
LIST OF MATERIAL								
56	1	RC32GF10IK	RESISTOR 1000 W 10%	AB	606175			
55	2		WASHER, NO.6 FLAT x 1/64 THK. SST		404891			
54	A/R		22 GA BHT WIRE	ALPHA				
53	1	20885-65-1	TRANSISTOR INSULATOR	METAL CRAFT	080858			
52	2	ZOF223A1	CHOKE 2.2 MH	MILLER	760025			
51	1	1416-6	SOLDER LUG	SMITH	242756			
50	2	2155	FIBER WASHER	SMITH	404963			
49	2		NUT HEX 6-32x1/4 AF	SST	403035			
48	2		NUT HEX 4-40x1/4 AF		403030			
47	4		NUT HEX 2-56x3/16 AF		403010			
46	1		WASHER 6 SPLIT LOCK		404895			
45	2		4 SPLIT LOCK		404880			
44	2		4 FLAT x 1/64 THK.		404876			
43	4		WASHER 2 SPLIT LOCK		404861			
42	1		SCREN 6-32x1/4 FH		404359			
41	2		6-32x1/2 BH		404385			
40	2		4-40x1 BH		404246			
39	4		SCREN 2-56x3/16 BH	SST	404010			
38	A/R 46410	GRIPPLET		BERG				
37	5	2331272-1	MINI INSERT	AMP	247065			
36	8	A919	EYELET	STIMPSON				
35	4	2059	EYELET	STIMPSON				
34	11	S-6064	EYELET	US				
33	4	W93-102ET	STAKE PIN FEMALE	B CHAIN	744555			
32	8	R62-3ET	STAKE PIN MALE	B CHAIN	744550			
31	4	1246-11	STANDOFF	CTC	683168			
30	3	1246-9	STANDOFF	CTC	683140			
29	1	252-06-30-100	CONNECTOR	CINCH	241625			
28	1	6020-28A	CLAMP	AUGAT	184487			
27	1	6018-63A	CLAMP	AUGAT	184470			
26	1	TM2723	TRANSFORMER	TRANS INC	766223			
25	1	46206LFR5-64PC	SWITCH	SM/CR	SPECIAL 2/64" PC TERM. 725100			
24	2	1N4753A	DIODE	MOT	040819			
23	4	1N4004	DIODE	MOT	040572			
22	1	SN72723	INT CIR	TI	060429			
21	1	LNT41CN	INT CIR	NAT	060140			
20	1	2N3055	TRANSISTOR	RCA	080550			
19	1	2N223BA	TRANSISTOR	MOT	080469			
18	4	2N2222	TRANSISTOR	NAT	080467			
17	1	390238G050J14	CAPACITOR 2300MF 50V	SPRAGUE	023590			
16	1	066GH.58117075B	580MF 75V	SANGANO	023464			
15	1	TE-1307	50MF 50V	SPRAGUE	023345			
14	1	DO-501	500PF 1KV	CRL	021210			
13	1	035X5V0502Z	CAPACITOR DO5MF 100V	ERIE	021480			
12	1	T2P82K	POTENTIOMETER 2K	BECOMAN	627219			
11	1	MC320F821K	RESISTOR 8200 1W 10%	AB	606375			
10	1	4567	100 SR 5X	OHMMITE	622272			
9	1	RNG0D1472F	14 7K 1/2W 1%	CORNING	624375			
8	2	RNG0D1002F	10K 1/2W 1%	CORNING	625288			
7	1	RNG0D4021F	4 02K 1/2W 1%	CORNING	624760			
6	2	RCU76P72K	8 7K 1/4W 10%	AB	602432			
5	2	300K	1K		602372			
4	1	2R7K	2 70		602012			
3	2	RC076F222K	RESISTOR 2 2K 1/4W 10%	AB	602420			
2	1	C2951	HEAT SINK	FEC				
1	1	H03138A	PC. BOARD	FEC				

Figure 7-7. Parts List



ITEM	REQ	REQ	REQ	PART NO.	DESCRIPTION	MATL OR MFR	MATL SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
	-3	-2	-1							
28	1	1	1		WASHER, 6 INT TOOTH	SST	404893			
27	10	10	10	46410	GRIPPLET	BERG				
26	2	2	2	275 125	FUSE PICO	LITTLEFUSE	368110			
25	1	1	1		SCREW 6-32x5/16 BH	SST	404369			
24	1	1	1	1246-15	STANDOFF	CTC	683224			
23	1	1	1	B2075	HOLD DOWN CLIP	FEC				
22	2			066HL301T10DB	CAPACITOR 300MFD 100V	SANGAMO	023398			
21	2			RC42GF103K	RESISTOR 10K 2W $\pm 10\%$	AB	608508			
20	1			TM-2178	TRANSFORMER	TI	765678			
19	1			TM-2179	TRANSFORMER	TI	765679			
18	A/R	A/R	A/R	SST1	CABLE TIE	PANDUIT				
17	2	2	2		NUT HEX 4-40x1/4 AF	SST	403030			
16	2	2	2		WASHER NO. 4 INT TOOTH	PHOS.BRZ	404878			
15	2	2	2		WASHER NO. 4 FLAT	BRASS	NT.P.	404876		
14	2	2	2		SCREW 4-40x5/16 LG FL HD	SST	UNDERCUT	404202		
13	1	1	1		SCREW 4-40x1" BD HD	SST	404246			
12	1	1	1		SCREW 4-40x1 3/8 LG FL HD	SST	404265			
11	1	1	1	8706	SPACER	SMITH	683890			
10	2	2	2	1300-10	STANDOFF	CTC	683462			
9	2	2	2	PN46N 062	FLUSH NUT	PMP	403575			
8	7	7	7	S6064	EYELET	US				
7	8	8	8	2059	EYELET	STIMPSON				
6	2	2	2	066HL581T076B	CAPACITOR 580MFD 75VDC	SANGAMO	023464			
5	4	4	4	1N4004	DIODE	MOT	040572			
4		2	2	RC42GF682K	RESISTOR 6 8K 2W 10%	AB	608585			
3		1	1	TM2856	TRANSFORMER	TRAN. INC.	766290			
2	1	1	1	C2368	CHASSIS	FEC				
1	1	1	1	N0829B	PC BOARD	FEC				

Figure 7-8. Optional Loop Power Supply Board Subassembly C2324D

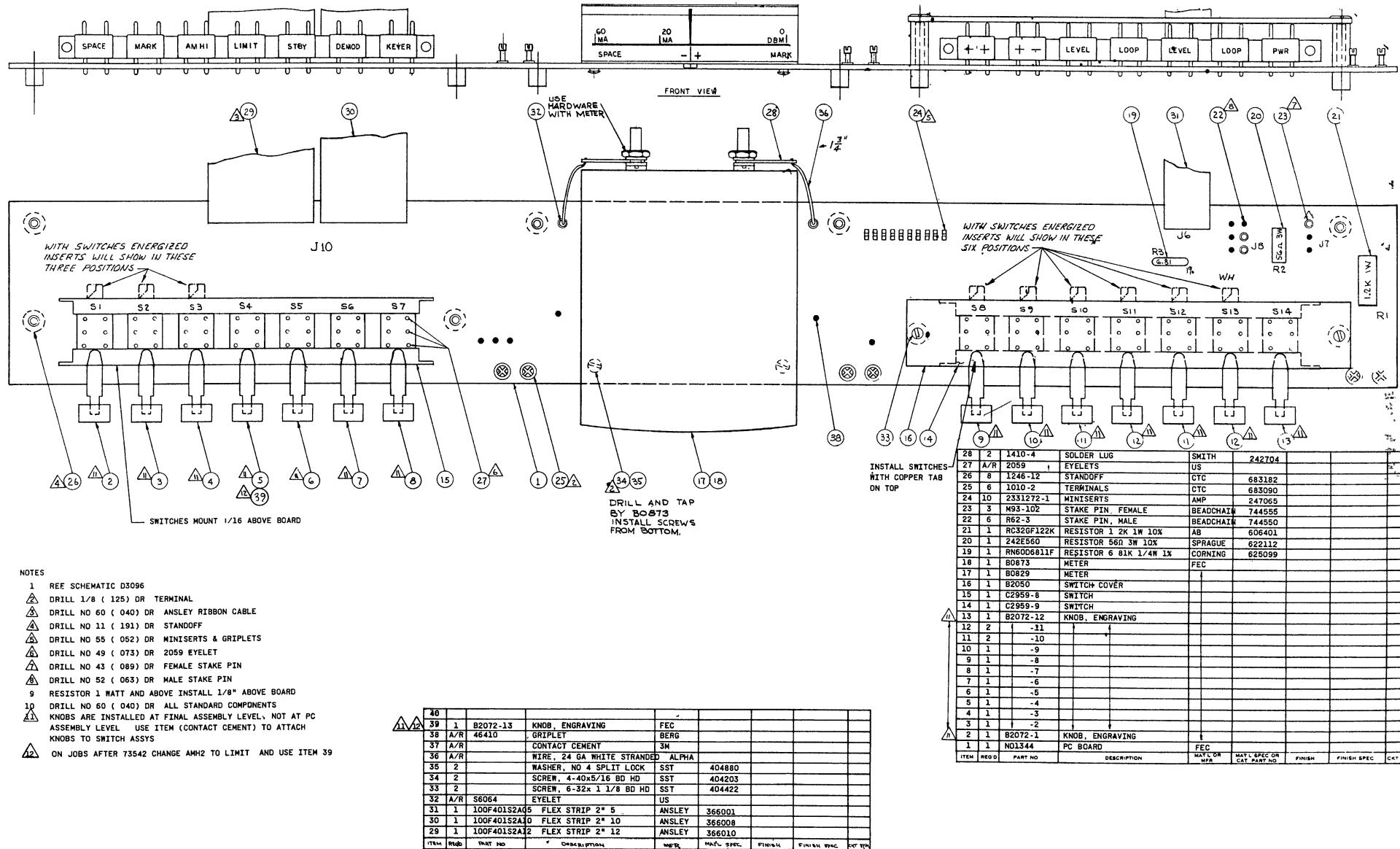
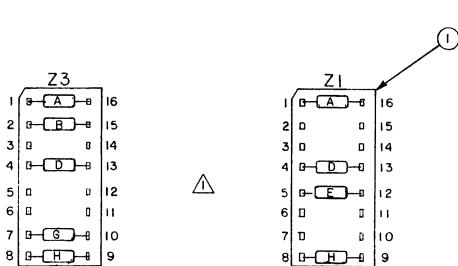


Figure 7-9. Front Panel Switch Board Subassembly
D3097C



A FOR RESISTOR POSITIONING SEE COLUMN MARKED Z1 & Z3
IN BILL OF MATERIAL
2 FOR SPECIFICATIONS SEE INPUT BANDPASS FILTER SELECTION
GUIDE A0521
3 SCHEMATIC REFERENCE D3738

Figure 7-10. Input Active Bandpass Filter Assembly

-16	1630Hz	850Hz	1185Hz	TO	2815Hz
-15	170Hz	140Hz	340Hz	TO	510Hz
-14	1585Hz	850Hz	965Hz	TO	2550Hz
-13	1420Hz	850Hz	1330Hz	TO	2750Hz
-12	1270Hz	850Hz	375Hz	TO	1645Hz
-11	1100Hz	850Hz	1350Hz	TO	2450Hz
-10	1050Hz	850Hz	975Hz	TO	2025Hz
-9	900Hz	850Hz	1250Hz	TO	2150Hz
-8	1500Hz	1400Hz	3000Hz	TO	4500Hz
-7	750Hz	650Hz	850Hz	TO	1600Hz
-6	1100Hz	1000Hz	2000Hz	TO	3100Hz
-5	1000Hz	850Hz	1500Hz	TO	2500Hz
-4	950Hz	850Hz	950Hz	TO	1900Hz
-3	500Hz	425Hz	765Hz	TO	1265Hz
-2	370Hz	340Hz	630Hz	TO	1000Hz
-1	300Hz	170Hz	500Hz	TO	800Hz
FIL NO.	+ 3dB BANDWIDTH	MAXIMUM SHIFT	USABLE FREQUENCY RANGE		

NOTE:

1. ASSY DWG. D4029
2. SCH. DWG. D3738

Figure 7-11. Input Active Bandpass Filter Selector Guide
A0521H

NOTES:

1. SCH REF C3308.
2. UNLESS OTHERWISE SPECIFIED DRILL
ALL HOLES NO55 (.052) DR. & INSTALL
46410 GRIPPLETS.
■ NO .60 (.040) DR. 6 PLACES & INSTALL
TRANSISTORS.
● NO .68 (.031) DR. - 6 PLACES & INSTALL I.C.
▲ NO .30 (.128) DR. 4 PLACES & INSTALL STANOFFS.
3. INSTALL STANOFFS ON COMPONENT SIDE &
SOLDER ON TRACK SIDE.
4. JOG I.C. LEADS.
5. AFTER PRODUCTION TESTING, SPRAY ENTIRE P.C. BOARD
WITH HUMISEAL TYPE 1B-15. DO NOT SPRAY BANANA
PLUGS.

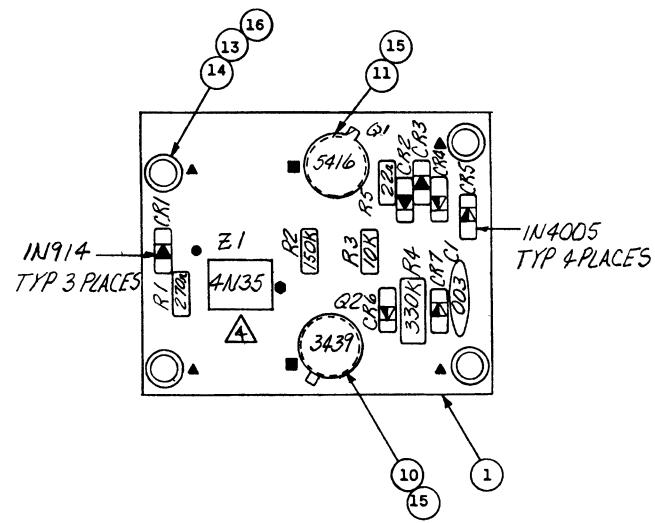
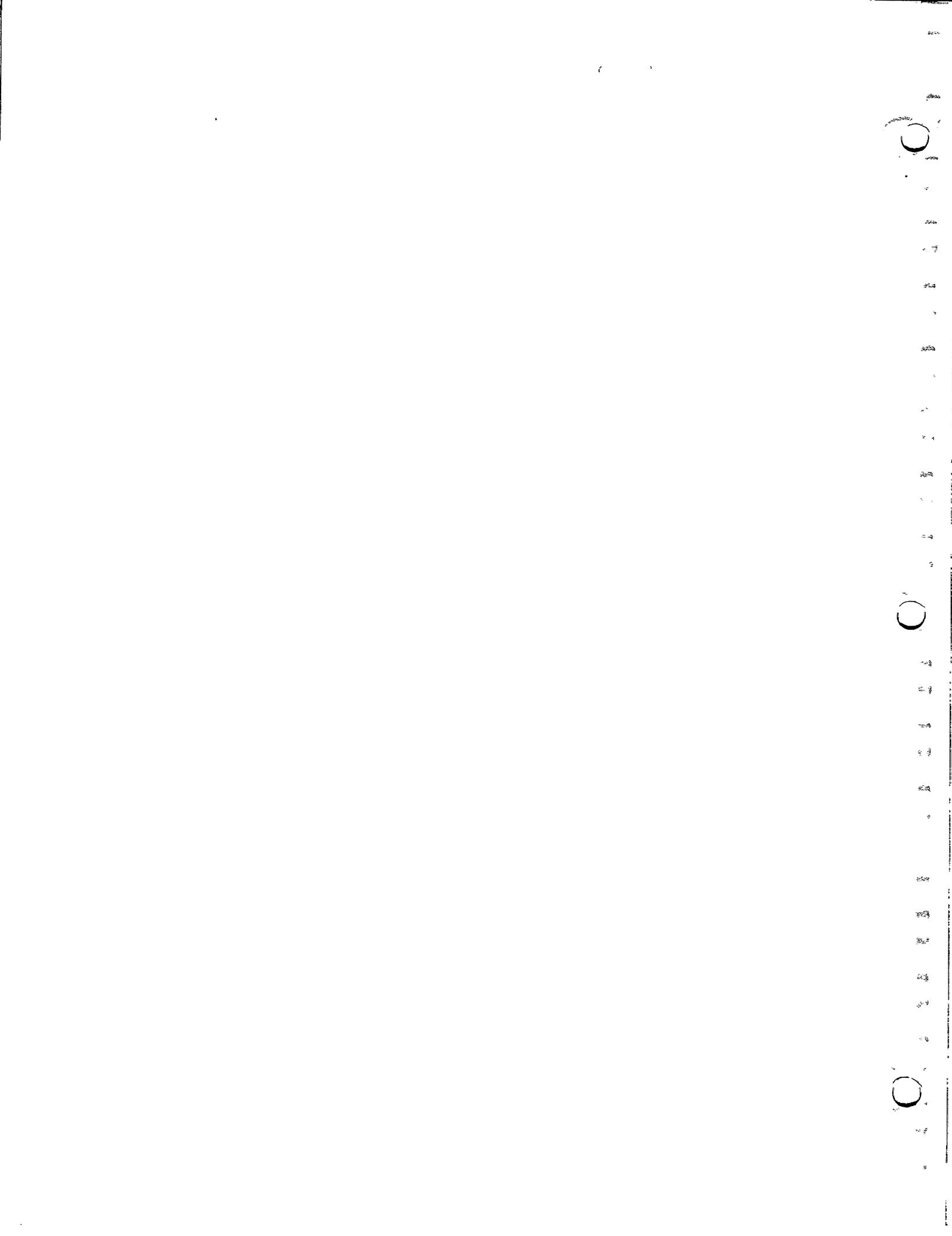


Figure 7-12. Optically Isolated High Level Neutral Keyer Assembly Drawing
C3240D

4	17		SCREW 2-56x5/16	T&C	404020	
4	16		WASHER NO.2 SPLIT LOCK	SST	404861	
2	15	2	A10020	ROSS	080836	
4	14	4	2188-12	CAMBION	683840	
	13	4	192	SMITH	246321	
1	12	1	4N35	GE	060448	
1	11	1	2N5416	MOT	080889	
1	10	1	2N3439	MOT	080566	
4	9	4	IN4005	GE	040594	
3	8	3	1N914	MOT	040238	
1	7	1	DD-302	CRL	021390	
1	6	1	RC20GF334K	RESISTOR 330K 1/2W 10%	AB	604890
1	5	1	RC07GF154K	RESISTOR 150K 1/4W 10%	AB	602708
1	4	1	RC07GF103K	RESISTOR 10K 1/4W 10%	AB	602540
1	3	1	RC07GF271K	RESISTOR 270Ω 1/4W 10%	AB	602288
1	2	1	RC07GF220K	RESISTOR 22Ω 1/4W 10%	AB	602132
1	1	1	NO1452	P.C. BOARD	FEC	
REQD	ITEM	REQD	PART NO.	DESCRIPTION	MATL OR MFR	MATL SPEC OR CAT PART NO.
-1			STD			LIST OF MATERIAL

Figure 7-12. Parts List

APPENDICES



APPENDIX FI
OPTIONAL FILTERBOARD

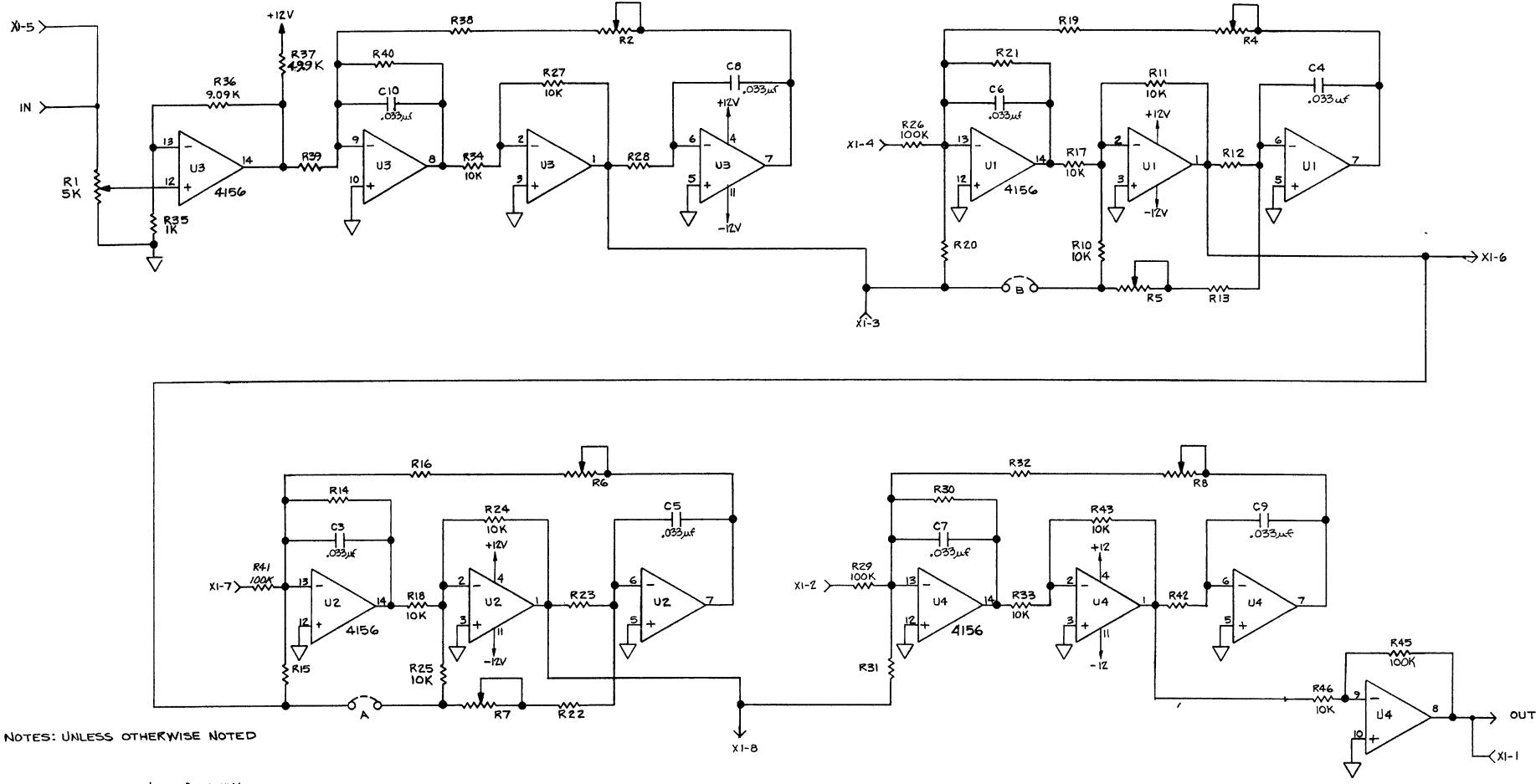
Due to customer requirements, the filterboard documented in the following pages is now available for use in the Model 1200A and the Model 1273. Filterboards D2818 and C3916 are plug-in interchangeable.

C3916 IS UPDATED VERSION OF
D2818
D2818 WAS ISSUED IN 234 VERSIONS

C

C

C



NOTES: UNLESS OTHERWISE NOTED

1. ALL RESISTORS 1/2W, 1% IN OHMS
2. POLES MUST BE TUNED BEFORE ZEROS
3. PWB REF NO 1991
4. ASSY REF. C3916

△ -42 REPLACES -33

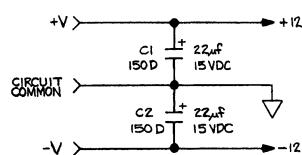


Figure FI-1. Filter Schematic
D5336T, Sheet 1

03916

-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19	-20	-21	-22	-23	-24	-25	-26	-27	-28	-29	-30	-31	-32		
JENTER FREQ (Hz) 382.5	467.5	552.5	631.5	722.5	801.5	872.5	977.5	1062.5	1147.5	1232.5	1317.5	1402.5	1487.5	1572.5	1657.5	1742.5	1827.5	1912.5	1997.5	2082.5	2167.5	2252.5	2337.5	2422.5	2507.5	2592.5	2677.5	2762.5	2847.5	2932.5	3017.5		
BANDWIDTH (Hz)	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70		
1ST STAGE																																	
POLE C.F (Hz)	343.7	428.6	513.6	598.5	683.5	768.5	853.5	938.4	1023.4	1108.4	1193.4	1278.4	1363.4	1448.4	1533.4	1618.4	1703.4	1788.4	1873.4	1958.4	2043.4	2128.4	2213.4	2298.3	2383.3	2468.3	2553.3	2638.3	2723.3	2808.3	2893.3	2976.3	
R39	332K	324K	316K	309K	301K	294K	294K	287K	287K	280K	280K	274K	274K	267K	267K	261K	261K	255K	255K	249K	249K	243K	243K	237K	237K	232K	232K	R39					
R40	332K	324K	316K	309K	301K	294K	294K	287K	287K	280K	280K	274K	274K	267K	267K	261K	261K	255K	255K	249K	249K	243K	243K	237K	237K	232K	232K	R40					
R28	14.0K	11.3K	9.31K	8.06K	6.98K	6.34K	5.62K	5.11K	4.75K	4.32K	4.02K	3.74K	3.57K	3.32K	3.16K	3.01K	2.8K	2.67K	2.55K	2.49K	2.37K	2.15K	2.01K	1.94K	1.87K	1.82K	1.78K	1.74K	1.65K	1.62K	R28		
R38	13.7K	10.7K	8.87K	7.50K	6.49K	5.76K	5.11K	4.44K	4.42K	4.12K	3.83K	3.48K	3.32K	3.09K	2.87K	2.74K	2.61K	2.43K	2.22K	2.1K	2.0K	1.91K	1.87K	1.87K	1.74K	1.69K	1.66K	1.63K	1.58K	R38			
R2 (POT)	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	R2 (POT)		
2ND STAGE																																	
POLE C.F (Hz)	363.4	446.7	533.6	618.9	704.0	789.1	874.1	957.2	1044.2	1129.2	1214.3	1297.3	1384.3	1469.3	1554.3	1639.4	1724.4	1809.4	1894.4	1979.4	2064.4	2149.4	2234.4	2319.4	2404.4	2487.4	2571.4	2659.4	2744.4	2829.4	2914.4	2979.5	POLE CF Hz
ZERO C.F (Hz)	305.8	389.5	473.5	557.8	642.3	726.9	811.5	891.0	981.0	1065.8	1150.6	1235.5	1310.3	1405.2	1490.1	1575.0	1660.0	1744.8	1829.8	1914.7	1999.6	2084.6	2169.5	2254.5	2339.5	2424.4	2510.4	2594.3	2679.3	2764.3	2849.2	ZERO CF Hz	
R20	110K	107K	107K	107K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	R20			
R21	110K	107K	107K	107K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	105K	R21			
R12	19.3K	10.7K	9.09K	7.87K	6.81K	6.04K	5.49K	4.79K	4.04K	3.42K	3.02K	2.74K	3.48K	3.32K	3.09K	2.94K	2.8K	2.67K	2.55K	2.43K	2.32K	2.2K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	R12	
R19	12.7K	10.2K	8.45K	7.32K	6.34K	5.67K	5.16K	4.53K	4.04K	3.42K	3.02K	2.74K	3.48K	3.32K	3.09K	2.94K	2.8K	2.67K	2.55K	2.43K	2.32K	2.2K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	R19	
R13	18.2K	13.7K	11.0K	9.09K	7.68K	6.65K	5.73K	5.23K	4.76K	4.32K	4.02K	3.57K	3.32K	3.16K	2.94K	2.74K	2.61K	2.49K	2.37K	2.24K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	1.54K	R13		
R4 (POT)	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	R4 (POT)		
R5 (POT)	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	R5 (POT)		
3RD STAGE																																	
POLE C.F (Hz)	399.2	484.4	586.6	684.7	787.7	824.8	909.9	994.9	1079.9	1165.0	1250.0	1345.0	1420.0	1505.0	1590.1	1675.1	1760.1	1845.1	1930.1	2015.1	2105.1	2185.1	2270.2	2355.2	2440.2	2525.2	2610.2	2695.2	2780.2	2865.2	2950.2	3035.2	POLE CF Hz
ZERO C.F (Hz)	474.4	558.0	642.0	726.3	810.8	895.4	980.0	1064.7	1149.5	1234.3	1319.1	1404.0	1486.8	1573.7	1668.6	1763.5	1858.4	1943.4	2028.3	2116.2	2203.1	2298.1	2383.0	2473.0	2569.2	2657.9	2746.8	2834.6	2923.6	3017.6	3102.7	ZERO CF Hz	
R14	100K	100K	100K	100K	102K	102K	102K	102K	100K	R14																							
R15	100K	100K	100K	100K	100K	102K	102K	102K	102K	100K	R15																						
R25	12.1K	10.0K	8.45K	7.32K	6.49K	5.9K	5.32K	4.75K	4.22K	3.67K	3.17K	2.74K	3.03K	3.01K	2.94K	2.74K	2.61K	2.49K	2.37K	2.24K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	1.58K	R25		
R16	11.5K	9.58K	8.06K	6.81K	6.04K	5.32K	4.75K	4.22K	3.67K	3.17K	2.74K	3.03K	3.01K	2.94K	2.74K	2.61K	2.49K	2.37K	2.24K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	1.58K	R16			
R7^2	-	8.00K	6.78K	6.04K	5.49K	4.67K	4.32K	4.04K	3.65K	3.4K	3.24K	3.01K	2.87K	2.67K	2.55K	2.43K	2.26K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	1.58K	R16					
R	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	R (POT)		
R7 (POT)	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	R7 (POT)		
4TH STAGE																																	
CENTER FREQ (Hz)	422.1	501.1K	592	677.0	761.9	846.9	921.9	1016.9	1101.9	1186.8	1271.8	1356.8	1441.8	1526.8	1611.8	1696.8	1781.8	1866.8	1951.8	2036.8	2121.8	2206.8	2291.8	2376.8	2461.8	2541.8	2621.8	2701.8	2786.8	2876.8	CENTER FREQ Hz		
R30	267K	274K	274K	280K	280K	280K	280K	274K	267K	267K	R30																						
R31	267K	274K	274K	280K	280K	280K	280K	274K	267K	267K	R31																						
R42	11.5K	9.58K	8.00K	7.15K	6.34K	5.76K	5.23K	4.75K	4.22K	3.67K	3.17K	2.74K	3.03K	3.01K	2.94K	2.74K	2.61K	2.49K	2.37K	2.24K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	1.58K	R42		
R32	11.0K	20.9K	17.8K	14.6K	5.76K	5.23K	4.75K	4.22K	3.65K	3.17K	2.74K	3.03K	3.01K	2.94K	2.74K	2.61K	2.49K	2.37K	2.24K	2.1K	2.0K	1.91K	1.87K	1.82K	1.74K	1.69K	1.65K	1.62K	1.58K	R32			
R8(POT)	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	1K	R8(POT)		

Figure FI-1. Filter Schematic

D5336T, Sheet 2

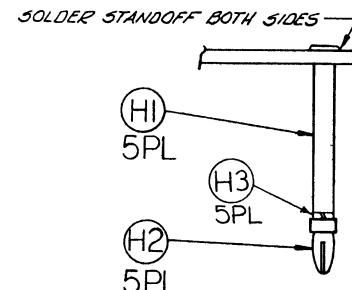
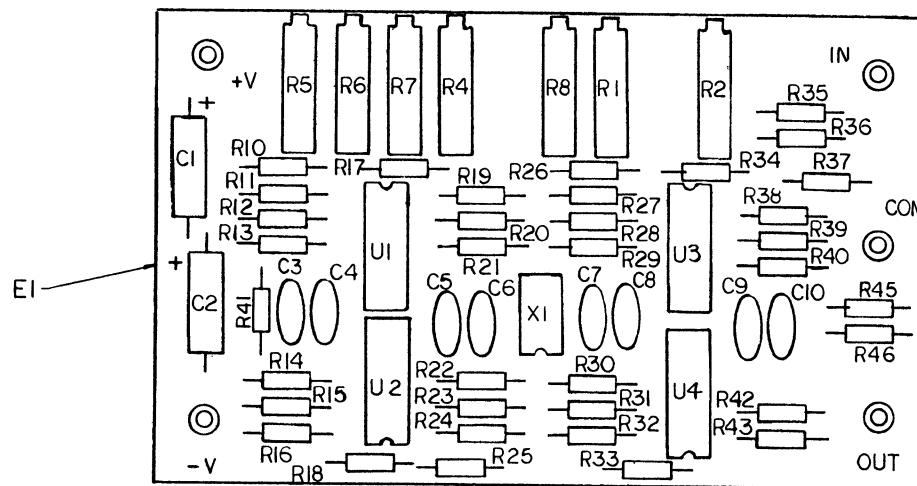
1273 NA

		A																																	
		-33	-34	-35	-36	-37	-38	-39	-40	-41	-42	-43	-44	-45	-46	-47	-48	-49	-50	-51	-52	-53	-54	-55	-56	-57	-58	-59	-60	-61	-62	-63	-64		
CENTER FREQ. Hz		2425	1575	500	700	900	1575	2000	2100	2125	2425	2975	1825	2175	2580	2700	875	1125	2425	400	890	2100	1700	2340	2468	1303	21.03	1280	2130	1500	2018	2072	1575	CENTER FREQ. Hz	
BANDWIDTH Hz		200	200	400	400	400	400	400	200	200	150	150	100	100	100	100	100	100	100	100	200	200	100	100	400	400	400	400	42.5	42.5	700	BANDWIDTH Hz			
1ST STAGE																															1ST STAGE				
POLE C.F.	R33	2330.15	1480.35	304.245	502.041	700.802	1375.91	1788.37	1898.27	2023.69	2323.56	2873.5	1748.93	2018.88	2529.18	2644.17	824.573	1074.31	2223.01	349.718	1993.81	1998.65	1998.76	2189.19	2409.18	102.44	1901.27	1079.5	1988.24	1299.04	1196.36	2050.32	1226.4	POLE CF Hz	
R39	118 K	124 K	95.3 K	80.6 K	73.2 K	64.5 K	61.9 K	61.9 K	113 K	110 K	107 K	150 K	147 K	200 K	196 K	237 K	232 K	60.4 K	261 K	237 K	113 K	118 K	209 K	200 K	66.5 K	61.9 K	61.9 K	64.9 K	432 K	432 K	422 K	422 K	R39		
R40	118 K	124 K	95.3 K	80.6 K	73.2 K	64.1 K	61.9 K	61.9 K	113 K	110 K	107 K	150 K	147 K	200 K	196 K	237 K	232 K	60.4 K	261 K	237 K	113 K	118 K	205 K	200 K	66.5 K	61.9 K	61.9 K	64.9 K	432 K	432 K	422 K	422 K	R40		
R28	2.05 K	3.32 K	15.8 K	9.53 K	6.81 K	3.48 K	2.67 K	2.55 K	2.37 K	2.1 K	1.65 K	2.74 K	3.32 K	191 K	1.82 K	5.9 K	4.53 K	2.15 K	1.37 K	6.04	2.43 K	3.01 K	2 K	4.42 K	2.95 K	4.42 K	2.49 K	3.74 K	2.49 K	2.37 K	3.92 K	R28			
R38	1.82 K	3.01 K	15.4 K	9.05 K	6.34 K	3.24 K	2.43 K	2.32 K	2.15 K	1.82 K	1.59 K	2.49 K	2.05 K	1.82 K	1.74 K	5.36 K	4.22 K	1.91 K	1.33 K	5.49	2.15 K	2.74 K	1.87 K	4.12 K	2.26 K	3.48 K	2.15 K	2.1 K	3.69 K	R38					
R2 (POT)	500.0	500.0	1 K	1 K	1 K	500.0	500.0	500.0	500.0	200.0	500.0	500.0	500.0	200.0	1 K	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	R2 (POT)				
2ND STAGE																																	2ND STAGE		
POLE C.F. Hz	R20	2380.52	1529.91	379.65	588.27	712.778	1747.2	1900.96	2001.27	2071.16	2377.35	2927.52	1789.26	2139.42	2538.51	2676.53	850.924	1011.12	2327.09	748.33	2058.97	2052.15	1691.79	2316.48	2436.5	1200.45	2004.28	1177.27	2031.37	1398.79	2008.08	2062.08	1387.36	POLE CF Hz	
ZERO C.F. Hz	R22	2227.51	1381.34	201.462	367.615	546.443	184.85	160.56	1699.72	1915.46	2210.31	2762.81	1666.96	2015.99	2472.5	2572.91	1771.221	1019.72	2019.78	2627.76	264.36	1890.57	1492.77	2232.69	2352.94	242.781	1702.67	902.828	1729.2	114.25	1971.94	2025.93	356.215	ZERO C.F. Hz	
R20	43.2 K	42.2 K	24.9 K	23.2 K	22.6 K	21 K	21 K	21 K	40.2 K	40.2 K	39.2 K	53.6 K	52.3 K	76.8 K	75 K	82.5 K	80.6 K	20.5 K	84.5 K	82.5 K	40.2 K	26.8 K	21.5 K	21 K	21.5 K	20.5 K	21 K	174 K	174 K	12.7 K	R20				
R21	43.2 K	42.2 K	24.9 K	23.2 K	22.6 K	21 K	21 K	21 K	40.2 K	40.2 K	39.2 K	53.6 K	52.3 K	76.8 K	75 K	82.5 K	80.6 K	20.5 K	84.5 K	82.5 K	40.2 K	26.8 K	21.5 K	21 K	21.5 K	20.5 K	21 K	174 K	174 K	12.7 K	R21				
R12	2.05 K	3.16 K	12.7 K	8.25 K	6.04 K	3.24 K	2.55 K	2.43 K	2.32 K	2.05 K	1.65 K	2.67 K	2.26 K	1.87 K	1.82 K	5.62 K	4.42 K	2.05 K	13 K	5.9 K	2.37 K	2.94 K	2.1 K	1.96 K	4.02 K	2.43 K	4.12 K	2.37 K	3.48 K	2.49 K	2.32 K	3.48 K	R12		
R19	1.78 K	2.94 K	12.1 K	7.68 K	5.62 K	3.01 K	2.26 K	2.15 K	2.05 K	1.78 K	1.54 K	2.43 K	2 K	1.78 K	1.67 K	5.11 K	4.12 K	1.82 K	124 K	5.36 K	2.1 K	267 K	182 K	1.87 K	374 K	2.1 K	3.83 K	2.1 K	316 K	2.1 K	2.1 K	3.24 K	R19		
R13	2.05 K	3.74 K	44.2 K	20.5 K	12.4 K	4.53 K	3.32 K	3.05 K	2.94 K	2.1 K	1.74 K	2.87 K	2.26	1.78 K	1.82 K	6.34 K	4.64 K	2.49 K	194 K	6.65	2.49	3.32 K	2 K	1.87 K	6.34 K	3.09 K	6.49 K	301 K	4.99 K	2.26 K	2.15 K	6.81 K	R13		
R4 (POT)	500.0	500.0	1 K	1 K	1 K	500.0	500.0	500.0	500.0	200.0	500.0	500.0	500.0	200.0	1 K	500.0	500.0	500.0	500.0	200.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	R4 (POT)					
R5 (POT)	200.0	200.0	1 K	1 K	500.0	500.0	500.0	500.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	1 K	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	R5 (POT)					
3RD STAGE																																	3RD STAGE		
POLE C.F. Hz	R14	2467.27	1616.69	571.413	776.744	980.026	160.26	2086.81	2187.04	2169.96	2470.13	3020.36	1658.85	2204	2602.87	2722.91	877.321	1107.52	2512.83	121.344	878.325	2144.94	1744.61	2362.86	2482.88	1386.77	210.09	1343.62	2217.16	1584.9	2077.79	2081.79	1719.04	POLE CF Hz	
ZERO C.F. Hz	R24	2336.75	1790.58	1076.84	1242.91	421.03	2026.23	2497.45	2575.1	2353.15	2652	3200.5	119.23	2344.26	2679.39	2811.66	110.02	1253.22	2899.15	521.62	969.23	2328.26	1930.46	2451.54	2571.43	1800.0	2578.04	1778.18	2004.58	1989.63	2064.95	2181.94	2488.18	ZERO C.F. Hz	
R14	41.2 K	41.2 K	16.5 K	17.4 K	18.2 K	18.7 K	19.1 K	19.1 K	1.38 K	38.3 K	38.3 K	51.1 K	51.1 K	75 K	75 K	76.8 K	76.8 K	19.1 K	75 K	76.8 K	19.1 K	75 K	18.7 K	19.1 K	18.7 K	19.1 K	18.7 K	19.1 K	18.7 K	19.1 K	10.2 K	R14			
R15	41.2 K	41.2 K	16.5 K	17.4 K	18.2 K	18.7 K	19.1 K	19.1 K	1.38 K	38.3 K	38.3 K	51.1 K	51.1 K	75 K	75 K	76.8 K	76.8 K	19.1 K	75 K	76.8 K	19.1 K	75 K	18.7 K	19.1 K	18.7 K	19.1 K	18.7 K	19.1 K	18.7 K	19.1 K	10.2 K	R15			
R25	2 K	2.94 K	8.45 K	6.19 K	4.87 K	2.94 K	2.32 K	2.21 K	1.96 K	1.58 K	2.61 K	2.21 K	1.87 K	1.52 K	1.91 K	1.74 K	1.69 K	4.97 K	3.92 K	11 K	4.99 K	2.2 K	2.49 K	3.24 K	196 K	3.32 K	1.91 K	2.8 K	2.15 K	2.55 K	R25				
R16	1.87 K	2.74 K	576 K	464 K	267 K	2.05 K	1.96 K	1.96 K	1.87 K	1.52 K	2.32 K	1.91 K	1.74 K	1.69 K	4.97 K	3.92 K	11 K	4.99 K	2.2 K	2.49 K	3.24 K	196 K	3.32 K	1.91 K	2.8 K	2.15 K	2.55 K	R16							
R22	1.58 K	2.1 K	2.15 K	2.1 K	1.78 K	1.54 K	1.5 K	1.58 K	1.33 K	2 K	1.82 K	1.62 K	1.58 K	4.12 K	3.32 K	2002	1 K	1 K	500.0	500.0	200.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	500.0	R22				
R6 (POT)	200.0	200.0	1 K	1 K	500.0	500.0	500.0	500.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	1 K	500.0	500.0	422 K	182 K	1.78 K	1.91 K	1.82 K	1.49 K	2.05 K	2 K	124 K	R22 (POT)						
R7 (POT)	200.0	200.0	500.0	500.0	500.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	1 K	500.0	500.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	R7 (POT)					
4TH STAGE																																	4TH STAGE		
CENTER FREQ. Hz	R20	2520.61	1670.88	713.052	910.17	108.65	781.86	220.586	2305.75	2227.35	2527.22	30722	190.72	2251.66	2631.05	2751.02	926.23																		

	-65	-66	-67	-68	-69	-70	-71	-72	-73	-74	-75	-76	-77	-78	-79	-80	-81	-82	-83	-84	-85	-86	-87	-88	-89	-90	-91	-92	-93	-94	-95	-96			
CENTER FREQ. Hz	2429	2182.5	1417.5	1989	1815	1785	1615	1575	2125	1100	900	1415	1585	980	1180	1650	1850	980	1870	1080	1940	1125	1425	960	1200	1320	2060	500	700	2550	420	540	CENTER FREQ. Hz		
BANDWIDTH Hz	700	70	70	120	120	135	135	260	260	130	130	100	100	130	130	130	130	100	100	250	250	130	130	250	250	250	250	130	200	85	85	BANDWIDTH Hz			
1ST STAGE																																1ST STAGE			
PALE C.F.	20737	2146.91	1981.94	1924.08	1754.1	1716.92	1546.55	1443.71	2293.32	1034.2	834.285	1364.24	1534.24	914.246	1114.17	1584.07	1784.04	929.341	1819.21	954.178	1813.53	1059.5	1359.11	834.346	1074.03	1693.48	1333.48	134.666	32.412	2448.56	3771.158	497.061	PALE CF. Hz		
R29	37.4K	280K	309K	182K	182K	169K	169K	93.1K	88.7K	182K	187K	226K	221K	187K	182K	174K	169K	237K	215K	102K	95.3K	182K	178K	105K	100K	95.3K	93.1K	200K	191K	110K	301K	287K	R39		
R40	37.4K	280K	309K	182K	182K	169K	169K	93.1K	88.7K	182K	187K	266K	221K	187K	182K	174K	169K	237K	215K	102K	95.3K	182K	178K	105K	100K	95.3K	93.1K	200K	191K	110K	301K	287K	R40		
R28	2.38K	2.26K	3.46K	2.49K	2.74K	2.8K	3.09K	3.32K	2.1K	1.64K	5.76K	3.97K	3.16K	5.23K	4.32K	3.01K	2.67K	5.23K	2.67K	5.11K	4.53K	3.57K	5.76K	4.53K	2.87K	2.49K	1.1K	7.68K	1.96K	12.7K	9.76K	R28			
R36	2.1K	2K	3.24K	2.86K	2.94K	2.95K	2.87K	3.09K	1.87K	4.48K	5.23K	3.32K	2.87K	4.75K	4.12K	2.8K	2.43K	4.64K	4.23K	4.53K	4.23K	4.32K	5.23K	4.22K	2.61K	2.26K	10.5K	7.15K	1.87K	12.4K	9.31K	R36			
R2 (PDT)	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	1K	500.2	500.2	1K	500.2	500.2	1K	200.2	1K	1K	1K	1K	R2(PDT)												
2ND STAGE																																2ND STAGE			
PALE C.F. Hz	2246.6	2166.1	1401	1956.61	1786.54	1752.91	1562.82	1511.35	2362.55	1068.66	868.39	1391.27	1561.32	948.512	1148.74	1619.06	1819.15	156.02	1846.4	1017.46	1879.52	1093.69	1393.34	894.849	137.93	1763.35	999.67	161.177	167.751	2502.41	398.937	519.244	PALE C.F. Hz		
ZERO C.F. Hz	1797.17	2107.02	1542.62	1557.23	1697.62	1642.53	1472.82	1311.62	2152.27	965.336	67.006	1309.07	1478.7	846.257	1044.92	1512.82	1712.27	875.62	1763.23	834.741	1682.34	990.140	1288.61	78.17	95.193	164.335	80.142	374.223	36.621	238.91	335.428	453.579	ZERO C.F. Hz		
R20	12.1K	110K	113K	66.9K	66.9K	59K	59K	31.6K	30.9K	63.4K	63.4K	80.6K	78.7K	63.4K	63.4K	61.9K	61.9K	80.6K	78.7K	34K	63.4K	61.9K	34K	33.2K	32.4K	32.4K	64.9K	64.9K	39.2K	100K	97.6K	R20			
R21	12.1K	110K	113K	66.9K	66.9K	59K	59K	31.6K	30.9K	63.4K	63.4K	80.6K	78.7K	63.4K	63.4K	61.9K	61.9K	80.6K	78.7K	34K	63.4K	61.9K	34K	33.2K	32.4K	32.4K	64.9K	64.9K	39.2K	100K	97.6K	R21			
R12	2.15K	2.21K	3.48K	2.49K	2.67K	2.74K	3.0K	3.16K	2.05K	4.53K	5.49K	3.48K	3.09K	5.1K	4.22K	3.01K	2.67K	4.99K	2.61K	4.75K	2.59K	4.22K	2.74K	4.23K	10.2K	7.15K	1.91K	12.1K	9.31K	R12					
R19	1.91K	1.96K	3.16K	2.82K	2.43K	2.49K	2.8K	2.94K	1.78K	4.22K	5.11K	3.24K	2.87K	4.39K	2.74K	2.43K	4.53K	2.37K	4.53K	2.32K	4.12K	3.24K	4.87K	4.02K	2.49K	2.15K	10K	2.65K	8.2K	11.5K	8.87K	R19			
R13	3.24K	2.1K	3.48K	2.49K	2.8K	2.87K	3.24K	4.02K	2.21K	4.99K	6.65K	3.65K	3.65K	3.64K	5.9K	4.54K	3.16K	2.74K	5.49K	2.61K	6.49K	4.87K	3.83K	7.87K	5.62K	3.24K	2.74K	15.4K	9.53K	1.96K	16.5K	11.8K	R13		
R4 (PDT)	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	1K	500.2	500.2	1K	500.2	500.2	1K	200.2	1K	1K	1K	1K	R4(PDT)												
R5 (PDT)	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	1K	500.2	500.2	1K	500.2	500.2	1K	500.2	500.2	1K	500.2	500.2	R5(PDT)												
3RD STAGE																																3RD STAGE			
PALE C.F. Hz	2572.5	2193.54	1433.47	2012.28	1042.23	1615.53	1649.49	1632.01	2453.19	1128.79	928.739	1437.69	1601.71	1008.85	1209.07	1679.37	1879.45	1002.42	1892.73	133.69	1995.55	1154.02	1454.29	103.18	1254.11	1875.14	21/5.69	571.665	783.343	255.19	438.433	558.71	PALE C.F. Hz		
ZERO C.F. Hz	3289.04	2260.21	1495.81	219.9	1950.23	1937.77	1762.3	1880.62	2723.27	1247.83	1051.5	1527.92	1679.74	1130.75	1329.32	1797.31	196.77	1094.46	1982.07	1301.85	22.29.45	1724.67	152.11	1265.28	1499.08	210.49	234.855	150.7.1	854.107	2776.6	521.445	439.596	ZERO C.F. Hz		
R14	10.7K	107K	10K	63.4K	64.9K	576K	576K	29.4K	29.4K	59K	59K	76.8K	57.4K	59K	59K	76.8K	76.8K	30.1K	30.1K	59K	59K	30.1K	30.1K	30.1K	30.1K	59K	59K	30.1K	30.1K	59K	59K	R14			
R15	10.7K	107K	10K	63.4K	64.9K	576K	576K	29.4K	29.4K	59K	59K	76.8K	57.4K	59K	59K	76.8K	76.8K	30.1K	30.1K	59K	59K	30.1K	30.1K	30.1K	30.1K	59K	59K	30.1K	30.1K	59K	59K	R15			
R23	1.87K	2.21K	3.4	2.97K	2.61K	2.94K	2.94K	1.96K	4.32K	5.23K	3.32K	3.01K	4.75K	4.02K	2.87K	2.95K	4.87K	2.59K	4.22K	4.23K	4.22K	3.39K	4.75K	3.57K	232K	205K	3.66K	2.19L	1.74K	10.5K	8.06K	R23			
R16	1.78K	1.96K	3.09K	2.15K	2.97K	2.43K	2.61K	2.74K	1.82K	4.02K	4.64K	3.09K	2.74K	4.53K	3.74K	2.61K	2.32K	4.53K	2.32K	4.02K	2.15K	3.92K	3.09K	4.53K	3.57K	232K	205K	3.66K	2.19L	1.74K	10.5K	8.06K	R16		
R22	1.05K	1.82K	2.87K	1.91K	2.1K	2.1K	2.26K	1.96K	1.5K	3.24K	3.83K	2.74K	2.43K	3.57K	3.09K	2.8K	2.62K	2.05K	2.61K	1.82K	3.16K	2.67K	2.8K	2.43K	1.78K	1.74K	5.36K	4.53K	1.54K	7.32K	6.04K	R22			
R6 (PDT)	200.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	1K	500.2	500.2	1K	500.2	500.2	1K	200.2	1K	1K	1K	1K	R6 (PDT)												
R7 (PDT)	200.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	500.2	1K	500.2	500.2	1K	500.2	500.2	1K	200.2	1K	1K	1K	1K	R7 (PDT)												
4TH STAGE																																4TH STAGE			
CENTER FREQU.	2726.99	2218.21	1453.24	2046.3	1976.32	1654.02	1604.05	1708.56	2559.15	1166.61	966.706	1666.11	1626.08	1046.66	1246.58	1716.48	1616.45	1031.2	1921.07	1208.89	2068.17	119.52	1039.08	1287.72	198.23	288.17	2561.12	1763.85	2622.27	462.751	593.645	CENTER FREQU. Hz			
R20	28K	279K	294K	169K	174K	154K	154K	78.7K	78.7K	162K	162K	210K	162K	162K	158K	210K	205K	80.6K	82.5K	154K	158K	102K	243K	249K	R20										
R24	28K	274K	294K	169K	174K	154K	154K	78.7K	78.7K	162K	162K	210K	162K	162K	158K	210K	205K	80.6K	82.5K	154K	158K	102K	243K	249K	R24										
R42	1.74K	2.15K	3.32K	2.37K	2.55K	2.61K	2.8K	1.87K	4.12K	4.99K	3.32K	2.94K	4.64K	3.83K	2.8K	2.49K	4.64K	4.02K	3.24K	4.42K	2.26K	3.74K	2.11K	3.83K	3.01K	4.22K	3.4K	2.21K	1.96K	3.06K	5.76K	1.74K	10K	7.68K	R42
R32	1.62K	1.91K	3.09K	2.1K	2.32K	2.37K	2.61K	1.78K	3.92K	4.75K	3.01K	2.67K	4.32K	3.65K	2.8K	2.26K	4.42K	2.26K	3.74K	2.11K	3.83K	3.01K	4.22K	3.4K	2.21K	1.96K	3.06K	5.76K	1.74K	10K	7.68K	R32			
R8 (PDT)																																			

-97		-98		-99		-100		-101		-102		-103		-104		-105		-106		-107		-108		-109		-110		-111		-112		-113		-114		-115		-116		-117		-118		-119		-120		-121		-122		-123					
CENTER FREQ Hz		1620		1740		2125		2975		1660		2140		1075		1925		1300		1700		1415		1585		2100		1900		2125		2295		1700		1800		2200		765		1445		425		935		2425		1575		1100		900			
BANDWIDTH Hz		85		85		260		260		200		200		200		200		150		150		135		135		TO		TO		120		120		TO		TO		100		100		100		150		150		150									
1ST STAGE		POLE CF		1576.83		1696.82		1934.42		2849.19		1559.78		2038.64		974.112		1823.63		1224.06		1623.96		1346.59		1516.55		2064.41		1864.42		2064.07		2234.05		1664.43		1764.42		2164.41		714.415		3194.26		374.681		304.354		2348.86		1498.93		1024.14		824.26	
R29		255K		255K		88.7K		84.5K		117.6K		113.3K		124K		115K		158K		154K		174K		169K		287K		294K		178K		174K		301K		294K		280K		243K		226K		261K		237K		143K		154K		161K		165K			
R40		255K		255K		88.7K		84.5K		117.6K		113K		124K		115K		158K		154K		174K		169K		287K		294K		178K		174K		301K		294K		280K		243K		226K		261K		237K		143K		154K		161K		165K			
R28		3.09K		2.87K		2.43K		1.67K		3.1		2.37K		4.99K		2.67K		3.92K		2.94K		3.57K		3.16K		2.39K		2.61K		2.32K		2.15K		2.87K		2.74K		2.21K		6.81K		3.48K		13K		5.49K		2.05K		3.22K		4.70K		5.88K			
R2		2.8K		2.61K		1.58K		2.84K		2.11K		4.75K		2.37K		5.65K		2.74K		3.42K		2.94K		2.1K		1.91K		2.67K		2.49K		1.96K		6.19K		3.24K		12.4K		4.99K		1.80K		2.97K		4.46K		5.35K									
R2 (PDT)		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0		500.0									
2ND STAGE		POLE CF		159.95		1719.97		2022.95		1611.75		2092.17		1025.7		1871.01		1263.87		1664.19		1382.7		1522.81		2083.59		1883.57		2096.65		2266.69		1683.35		1783.56		2183.6		740.794		121.28		339.953		910.981		2389.5		1539.11		1043.62		83.262			
ZERO CF Hz		1529.2		1649.05		2.02		1701.74		1453.05		1930.4		1874.432		116.42		144.41		1542.41		1273.65		1442.97		2024.56		1824.68		1997.05		2166.8		1624.83		1724.75		2124.51		662.026		1339		327.078		830.861		2265.46		1417.93		345.945		742.167			
R20		93.1K		93.1K		30.9K		40.7K		40.1K		41.2K		40.2K		54.9K		53.6K		60.4K		59K		110K		110K		64.9K		64.9K		110K		110K		107K		82.5K		80.6K		84.5K		80.6K		52.3K		53.8K		54.8K		55.3K					
R21		93.1K		93.1K		30.9K		40.7K		40.1K		41.2K		40.2K		54.9K		53.6K		60.4K		59K		110K		110K		64.9K		64.9K		110K		110K		107K		82.5K		80.6K		52.3K		53.8K		54.8K		55.3K									
R12		3.01K		2.8K		2.93K		1.65K		2.30K		4.75K		2.55K		3.83K		2.87K		3.05K		2.32K		2.55K		2.32K		2.1K		2.87K		2.67K		2.21K		4.94K		3.4K		12.1K		5.29K		2.1		3.1K		4.53K		5.58K							
R19		2.74K		2.55K		2.1K		2.74		2.05K		4.42K		2.32K		3.57K		2.67K		3.24K		2.05K		2.32K		1.87K		2.61K		2.43K		1.96K		3.04K		11.5K		4.75K		1.77K		2.88K		4.29K		5.08K											
R13		3.09K		2.8K		2.61K		2.43K		2.45K		5.9K		2.8K		4.42K		3.09K		3.83K		2.21K		2.49K		2.26K		2.1K		2.87K		7.6K		3.57K		17.4K		5.9K		3K		3.44K															

Figure FI-1. Filter Schematic
D5336T, Sheet 5



NOTES

1. SEE SEPARATE PARTS LIST PL-C3916
2. REFERENCE DRAWINGS
SCHEMATIC D5336
FABRICATION SHEET I OF NO. 1991
3. SOLDER HI BOTH SIDES
4. FOR CORRECT CENTER FREQUENCY, BANDWIDTH
AND BAUD RATE USE APPROPRIATE DASH NUMBER
5. SOLDER STAND-OFFS CLOSED ON TRACK SIDE.

Figure FI-2. Filter Assembly
C3916AE

CARD CODE	FEC PART NO.	QUANTITY		CNC. CODE	DESCRIPTION	MFR.	MFR. PART NO.	REFERENCE DESIGNATOR	UNIT COST	TOTAL COST
	NO1991A	1			FILTER, PWB	FEC	NO1991A	E1		
	625239	1			RES. 9.09K 1/8W	SC003	RN55D9091F	R36		
	625721	1			RES. 49.9K 1/8W	SC003	RN55D4992F	R37		
	028594	2			CAP. 150D 22uf 15V	SPR	150D22X9015 -B2	C1,C2		
	029983	8			CAP. .033uf	SC139	BP6309G	C3-C10		
	248617	1			I.C. SOCKET	AUGAT	308-AG-39	X1		
	061828	4			QUAD OP-AMP	RAY	4156	U1-U4		
	683842	5			STANDOFF	CAMB	2188-14	H1		
	246321	5			BANANA PLUG	SMITH	192	H2		
	627291	1			POT 5K	BOURN	3006P-1-502	R1		
	624299	1			RES. 1K 1/8W	SC003	RN55D1001F	R35		
	625270	11			RES. 10K 1/8W	SC003	RN55D1002F	R34,R27,R17,R11,R18,R24,R33,R43,R10,R25, R46		
	625811	4			RES. 100K 1/8W	SC003	RN55D1003F	R26,R41,R29,R45		
	404861	5			WASHER NO.2 SPLIT LOCK	T&C	MS35338-134	H3		

Figure FI-2. Parts List

C)

C)

C)