

4.4.3 Front Panel Controller

The ST-8000A uses an integrated keyboard decoder and display controller (U8) shown in Figure A1819 to handle the front panel keypad input and seven segment display outputs. This device debounces keypad entries to prevent the inadvertent entry of multiple keys, and buffers the display data for the multiplexed front panel numerical displays and indicators.

The keypad/display interface controller (U8) is an 8 bit microprocessor peripheral device that connects directly to the control board data bus (DB0 to DB7), the read (RD_L) and write (WR_L) signals, address bit 0 (A0), the front panel enable (FP_L), and system reset (RESET). The microprocessor reads and writes the control and data registers in this device to input keypad entries and load the display buffer output registers. An internal counter divides the system clock (PCLK) input to set the keypad and display scanning rate.

The keypad and the front panel display are scanned through the binary encoded scan line outputs (SL0 to SL3) in Figure A1819 and 3-to-8 line decoders in Figures A1820 and A1821. Keypad entries are detected as a TTL low on one of the row inputs (RL0 to RL3).

The seven segment display segment drivers are connected to the segment outputs (U8-24 to U8-31). Data on this output bus is inverted; to turn a segment ON, the corresponding output is held at a TTL low level when the digit is scanned. Because the segment outputs do not have sufficient drive capability, discrete PNP switching transistors (Q17 to Q24) in Figure A1819 buffer these outputs for all of the display segments. The display segments anodes of the common cathode seven segment display digits are all driven in parallel, as shown in Figure A1822, and one scanned digit is selected with the digit driver circuit in Figure A1821.

4.4.3 Keypad

The front panel keypad is a matrix of single pole momentary switches arranged in three rows of 9 switches. The low three bits of the scan line outputs (SL0 to SL2) drive a 3-to-8 line decoder (U7) to select one of 8 keypad columns by forcing that column select line low. If any of the keypad switches in that column are closed, one of the row lines (RL0 to RL3) will be forced low to signal the keypad/display controller (U8) that a key has been pressed.

Note that the keypad is arranged as 4 rows of 8 keys and 1 row of 3 keys. This keypad/display controller (U8) has a maximum capacity of 8 rows by 8 columns, so it cannot scan the 9 columns in a simple matrix fashion. However, by connecting three of the column drivers to the last column, and connecting that column to a fourth row line (RL3), the entire matrix of switches may be scanned.

When a keypress is detected, the keypad/display controller (U8) stores the row and column locations into a key buffer and interrupts the microprocessor by forcing the front panel interrupt line (KBINT) high.

ST-8000A firmware determines the function of all front panel keypad keys; there are no hardwired switch functions.

4.4.3 Numerical Displays

The front panel assembly has 15 common cathode seven segment display digits and two additional LEDs driven in a multiplexed fashion by the keypad/display controller (U8). The scan line outputs (SL0 to SL3) select one of 16 digit drivers using two 3-to-8 line decoders shown in Figure A1821. For each of the 16 scan line selections, a single common cathode

digit driver transistor is enabled through an inverting buffer. As each digit is selected in turn, the segments are turned ON that correspond to the data presented on the keypad/display controller data output lines in Figure A1819.

The keypad/display controller (U8) is configured to scan the entire front panel display every 20 ms or 50 times per second to avoid visual flicker. In addition, the keypad/display controller blanks the display as the scan lines change so that display digit contrast is improved.

Figure A1822 illustrates the assignment of the digits to the front panel locations. Five digits are assigned to the MARK and SPACE frequency windows, four digits to the BAUD window, and a single digit to the CHANNEL display. The two LED's mirror the channel selection, but they are scanned as an independent digit during scan time slot 15.

The digit assignments for the front panel are summarized below:

DISPLAY	DIGIT SCAN NUMBER				
-----	-----	-----	-----	-----	-----
MARK	4	3	2	1	0
SPACE	9	8	7	6	5
BAUD		13	12	11	10
CHANNEL					14
LED					15

Each seven segment display digit has segments assigned as shown below:

SEGMENT	BIT							
	7	6	5	4	3	2	1	0
-----	-	-	-	-	-	-	-	-
SEG dp	X							
SEG g		X						
SEG f			X					
SEG e				X				
SEG d					X			
SEG c						X		
SEG b							X	
SEG a								X

4.4.3 LED Indicators

In addition to the multiplexed front panel display digits, there are 16 latched front panel LED indicators illustrated in Figure A1823. The two octal latches (U1, U2) are connected to the control board data bus (DB0 to DB7). The signals to load the LED latches come directly from an I/O output address decoder on the control board (LED0_L, LED1_L). The LED latch data is inverted; a TTL 0 turns the corresponding LED ON.

The LED data bus bit assignments for the front panel are summarized below:

LED0_L (U1)	BIT							
	7	6	5	4	3	2	1	0
-----	-	-	-	-	-	-	-	-

MARK	X							
CENTER		X						
SPACE			X					
SHIFT				X				
SYNC					X			
FSK						X		
MARK ONLY							X	
SPACE ONLY								X

	BIT							
LED1_L (U2)	7	6	5	4	3	2	1	0
-----	-	-	-	-	-	-	-	-
REGEN	X							
AMH		X						
HOLD			X					
REV				X				
ENTER					X			
DIV						X		
MUTE							X	
REMOTE								X