CHAPTER 5
THEORY OF OPERATION

5.1 GENERAL

This chapter describes the theory of operation of the ST-8000A. It includes descriptions of the demodulator, modulator, control, front panel, and power supply. The ST-8000A is an audio Frequency Shift Keyed (FSK) MODEM (MOdulator-DEModulator).

5.2 FSK SYSTEM APPLICATION

The ST-8000A is used to convert RS-232 or MIL-188 serial digital data into FSK audio tones. These tones are sent to distant stations using radio or wire lines. Digital data is used to FSK an audio tone. The FSK audio tone drives a radio transmitter or is connected to wire lines. The FSK modem at the receiving station detects these tones and converts the signal to digital data.

5.2.1 Radio FSK Data System

Figure 2.14 shows a typical radio FSK data system using the ST-8000A. Each radio system includes three to five major electronic components:

1. Data Terminal
2. Encryption Device (Optional)
3. ST-8000A Modem
4. Radio Transceiver
5. Remote Control System (Optional)

The Data Terminal device may be as simple as a keyboard and a printer. Or, it may be as complicated as a computer system. Data to and from the Data Terminal is digital. RS-232 or MIL-188 interface levels may be used.

The Encryption Device is optional. When used, it is installed between the Data Terminal and ST-8000A. Data into and out of the Encryption Device is digital RS-232 or MIL-188. Only the Data Terminal and Encryption Device need to be "secure units". The ST-8000A and radio process only encrypted "black" data.

The FSK Modem serves as a data format converter. It converts RS-232 or MIL-188 digital data to and from FSK audio tones. The ST-8000A's operation is similiar to that of a common telephone

modem. The ST-8000A includes additional signal processing to make up for distortion by radio propagation.

The radio may be separate receive and transmit devices, connected for transmit/receive control. The radio system may operate at any radio frequency (RF). Data to and from the radio equipment is audio FSK tones in the range of 300 to 3000 Hz. Radio characteristics determine data rate and tone frequencies used. The Push To Talk (PTT) control of the radio may be controlled by the ST-8000A keyline output.

The Remote Control System is optional. It sets and controls all ST-8000A operational parameters. A typical remote control system is a data terminal (VT-100, for example) or a computer system. Between one and nine ST-8000A modems may be controlled by one remote control system. Some systems include remote computer control of the radio.

5.2.2 Wire Line FSK Data System

Figure 2.16 shows a typical Wire Line FSK Data System. A wire line system is very similar to a radio data system. Except, in the wire line system, a wire connection replaces the radio link. A wire line system includes two to four major equipment items:

1. Data Terminal
2. Encryption Device (Optional)
3. ST-8000A Modem
4. Remote Control System (Optional)

The functions of these items are as described in section 5.2.1.

5.3 FUNCTIONAL DESCRIPTION

Figure 5.1 shows the major sections of the ST-8000A Modem. The ST-8000A includes a:

1. Demodulator circuit
2. Modulator circuit
3. Microprocessor Control circuit
4. Front Panel Display and Keypad Entry circuits

5. Power Supply.

One shielded aluminum cabinet contains the ST8000A. It is 19" wide (48.3 cm) by 3.5" high (8.9 cm) by 18" deep (45.7 cm). The ST-8000A is designed to be mounted in a standard "19 Inch Rack Cabinet". All external connections to the ST-8000A are made via 4 rear panel connectors. The ST-8000A front panel includes displays and LED indicators. These show modem tone frequencies, data rate, and selected parameter settings. A 27-key keypad allows manual entry of data to set operational parameters. ST-8000A parameters may also be set and read via the rear panel REMOTE port (J4). The following sections will discuss these circuits in greater detail.

5.3.1 Demodulator Circuits

Figure 5.2 shows a block diagram of the ST-8000A demodulator section. Demodulator circuits accept FSK signals and convert the signals to base band digital pulses (MARK or SPACE). The major functional requirements are:

1. Accept and filter the input FSK signal.
2. Discriminate and separate MARK and SPACE signals
3. Adjust for input signal amplitude variations.
4. Provide for varying FSK frequencies and data rates.
5. Detect and combine MARK and SPACE data signals.
7. Provide data outputs (RS-232 and MIL-188).
8. Provide control of signal processing.

FSK input signals from rear panel connector J2 (AUDIO I/O) pass through an impedance matching, balanced to unbalanced, isolating transformer. The input impedance is set by jumper A1J6 for 600 ohms or 10,000 ohms. Setting jumper A1J6 is described in section 2.5.1. Input signals pass through input filters and separate MARK and SPACE filters. The microprocessor control system sets the center frequency and bandwidth of the MARK and SPACE filters. The filtered MARK and SPACE signals are peak detected to provide outputs to the:

1. Front panel bar-graphs.
2. AMH (Automatic MARK Hold) circuit.
3. AGC (Automatic Gain Control) circuit.

The AMH Threshold and Delay are set by option switches A1SW1 (Threshold) and A1SW2 (Delay). The Threshold is adjustable in 6 dB increments over a range of -42 dBm to 0 dBm (600 ohm input). The Delay adjustment range is 1.0 to 5.0 seconds in 0.5 second increments. The AMH feature is turned ON or OFF under microprocessor control. Section 2.5.2 describes AMH settings.

The AMH circuit provides the Carrier Detect (CD) or Loss Of Signal (LOS) output signal. The CD/LOS polarity is set by jumper A1J9 as described in section 2.5.3. The CD/LOS signal is output to rear panel connector J1 (DATA I/O).

The AGC circuit adjusts the filtered MARK and SPACE signals for input signal amplitude variations. The signals then pass to

separate tone detectors. Programmable low pass filters follow the tone detectors to remove noise and other undesired signals. The cut off frequency of each low pass filter is set by microprocessor control (LP CLOCK). The pre-detection signals are output as the UNDETECTED MARK and SPACE signals on connector J1 (DATA I/O).

The detected and filtered MARK and SPACE pulses pass through MARK ONLY, SPACE ONLY and M/S (MARK/SPACE) pulse discriminators. The DETC MODE output of the microprocessor controller selects which discriminator output is sent to rear panel connector J1 (DATA I/O).

Signals with data rates higher than 600 baud (601 to 1200 baud) use a "High Speed" demodulator circuit. The output of the input filter stage drives a heterodyne mixer. This converts the signal to an Intermediate Frequency (IF) of approximately 12 kHz. The microprocessor control (HS LOCAL OSC) provides the Local Oscillator for this mixer. The IF signal passes through multiple section IF filters and amplitude limiter stages. A Phase Locked Loop detector detects the "High Speed" data signal.

Microprocessor control selects "High Speed" (601 - 1200 baud) or "Low Speed" (30 - 600 baud) detector outputs. The microprocessor provides polarity control (NORMAL/REVERSE) and Regeneration (REGEN) of the received data signal. Separate amplifiers provide RS-232 (MARK = -V) and MIL-188 (MARK = +V) output signals to rear panel connector J1 (DATA I/O). Microprocessor control detects received data pulses and generates a mid-bit clock output signal to J1.

The ST-8000A Built In Test (BIT) feature includes FSK audio loopback between the modulator and demodulator circuits. The audio input to the demodulator is disconnected from connector J2 (AUDIO IN) during BIT loopback tests. For these tests the demodulator input is connected to the modulator FSK audio output. This provides internal testing of all demodulator and modulator signal processing circuits. Three amplitude levels of BIT tests are included, 0 dBm, -20 dBm, and -45 dBm. BIT functions are set by microprocessor control (BIT CONTROL). When the Diversity Option is installed (Option -01), microprocessor control sets this feature.

The demodulator provides MARK and SPACE output signals that drive the front panel MARK and SPACE bar-graphs (MARK BAR OUT, SPACE BAR OUT). These signals provide calibrated front panel indications for the amplitude (in dBm) of the input FSK MARK and SPACE signals.

5.3.2 Modulator and Keyline Circuits

The ST-8000A Modulator circuit accepts Transmit Data (TXD) input from rear panel connector J1 (DATA I/O). Either RS-232 (MARK = -V) or MIL-188 (MARK = +V) format may be set by jumper A2J2 as explained in section 2.5.8. The microprocessor control sets the desired transmit data polarity (NORMAL/REVERSE).

A crystal controlled digital synthesizer generates the FSK modulator audio signals. The TXD input signal switches the modulator synthesizer between MARK and SPACE frequencies. The MARK and SPACE frequencies are set by microprocessor control. FSK modulator signals are generated at 100 times the desired output frequencies. An EPROM look-up table and D/A (Digital to Analog) converter generate a 100 step digital approximation of a sinewave. The D/A output is then low pass filtered to smooth the steps and eliminate harmonic distortion. The modulator output signal has more than 40 dB of harmonic suppression. All other spurious (undesired) signals are suppressed by more than 60 dB.

The modulator output signal passes through the front panel OUTPUT LEVEL control. The output level may be adjusted over a range of 0 dBm (maximum) to less than -35 dBm (600 ohm reference). The front panel bar-graphs indicate the actual output in dBm (600 ohm) when CH displays "2". The output FSK signal then passes through amplifiers and an isolating 600 ohm transformer to rear panel connector J2 (AUDIO I/O).

The input transmit data signal from J1 (DATA I/O) also drives the AUTO MUTE and Keyline circuits. TXD activity (MARK/SPACE transitions) is detected by the microprocessor control circuit. When an active transmit data (TXD) signal is present, the Keyline output terminals to J2 (AUDIO I/O) and J1 (DATA I/O) are shorted together. The isolated relay contact output is often used to turn the transmitter ON and OFF as explained in section 2.6.1.1.2.

When TXD activity ceases, the keyline relay opens after a delay set by switches A2SW1 and A2SW2. Setting the MUTE DELAY is explained in section 2.5.7. This delay may be set from 1.0 ms (milliseconds) to 9.999 Seconds in 1.0 ms increments. Jumper A1J8 allows ON/OFF control of the modulator FSK tone output by the AUTO MUTE feature (see section 2.5.4). A MUTE from the front panel or remote command turns the output tones OFF.

The ST-8000A DRTS (Data Request To Send) input on J1 allows immediate ON/OFF control of the keyline (and modulator output). A logical "high" (+V) signal to DRTS results in immediate closure of the keyline relay. This occurs regardless of activity on TXD. About 200 ms after DRTS is set to +V, the DCTS (Data Clear To Send) output signal to J1 activates. The DCTS signal may be used to "hold off" TXD until the transmitter's circuitry has stabilized. The microprocessor control provides a transmit data clock (TX CLOCK) output to rear panel connector J1 (DATA I/O). This may be used to synchronize external transmit data sources to the ST-8000A.

5.3.3 Microprocessor Control Circuits

The ST-8000A Microprocessor Control circuits perform the following tasks:

1. Controls all demodulator operating parameters.
2. Synthesizes filter clock signals to the demodulator.
3. Computes and sets demodulator filter bandwidths.
4. Provides receive data regeneration (REGEN).
5. Recovers mid-bit receive data clock.
6. Synthesizes MARK and SPACE modulator signals.
7. Sets modulator baud rate.
8. Generates transmit data clock.
9. Controls AUTO-MUTE feature and Keyline.
10. Controls the BIT feature.
11. Interprets and sets parameters from the keypad.
12. Sets all front panel displays and indicator LEDs.
13. Interfaces with and interprets all remote control input.
14. Performs all other required control and computation.

The ST-8000A Microprocessor Control circuit uses an 8-bit microprocessor (Z-80A). Three types of memory devices are used: (1) RAM (Random Access Memory), (2) PROM (Programmable Read Only Memory), and (3) EEPROM (Electrically Erasable ROM). All program "firmware" for the ST-8000A is contained in the PROM. Program execution and temporary storage use RAM. The EEPROM provides non-volatile storage of the currently set parameters. The previous parameters are restored from the EEPROM device each time AC power is turned ON.

The control system includes a "Dead-Man" timer circuit that senses microprocessor activity. If activity ceases (non-functioning processor), the "Dead-Man" circuit resets the microprocessor. This circuit guards against incorrect operation that might be caused by AC power "brown-outs" or transients. If the EEPROM contents are valid, the previous parameters are restored upon reset. If the EEPROM contents were disturbed by the fault, default parameters are restored upon reset. See section 2.7 for a list of the default parameters.

Microprocessor Control includes four direct digital frequency

synthesizers and three programmable clock dividers. The synthesizers provide clock outputs to the MARK and SPACE demodulator filters, Modulator FSK output, and the Local Oscillator to the "High Speed" demodulator mixer stage. Programmable dividers provide the Low Pass filter clock, 1.0 ms timing pulses for AUTO MUTE delay timing, and the data rate clock for the Remote control port. The microprocessor, synthesizers, and two clock dividers are timed from one 4.9152 MHz crystal controlled oscillator. A 6.144 MHz crystal controlled oscillator provides timing for the AUTO MUTE Delay circuit.

A serial I/O UART (Universal Asynchronous Receiver/Transmitter) provides interface between the remote control terminal and the microprocessor. Rear panel connector J4 (REMOTE) links the remote control terminal to the ST-8000A. Jumper A2J7 (see section 2.5.8) may be set for use of an RS-232 or MIL-188 remote control data format. The remote control data rate is set by option switch A2SW3. Setting this switch is explained in section 2.5.5. The microprocessor controller interprets and executes all remote control commands.

When the ST-8000A is used in a multiple unit "daisy-chain" connection for remote control, each ST-8000A must be set to a different unit address. Option switch A2SW4 sets this address, explained in section 2.5.6. In a multiple unit system, only one unit should use terminations on the remote control data signals. See section 2.5.9 for details on setting termination jumpers A2J4 and A2J8. Up to nine ST-8000A Modems may be controlled by one terminal or computer.

The microprocessor provides receive data regeneration (REGEN) and mid-bit clock recovery (MID-BIT CLK). Clock polarity is set by jumper A2J6. This jumper is discussed in section 2.5.8.

The microprocessor interfaces with the front panel displays and keypad. It interprets and executes all keypad entries. These entries are processed under firmware control. The demodulator and modulator parameters are then adjusted as required. The controller sets front panel displays and indicators to reflect current operating parameters.

5.3.4 Front Panel Circuits

The ST-8000A Front Panel includes all switches, displays, and indicators to manually operate the modem. The displays and indicators show all current parameters when remote control is used. Figure 5.5 shows the front panel interface. Figure 3.1 shows the front panel.

Operation of each key of the 27-key keypad is discussed in section 3.3. These keys are used to enter parameters and change operating modes of the ST-8000A. Figure 3.2 shows an expanded view of the keypad.

The Front Panel displays include 2 five-digit indicators to show MARK and SPACE frequencies. A four-digit display shows the BAUD RATE. A single digit shows the selected display and control CHANNEL. These displays show demodulator (CH 1) or modulator (CH 2) parameters. Eighteen LED (Light Emitting Diode) indicators show the current modes of the selected channel. The controller sets all displays and LED's.

The OUTPUT LEVEL front panel control allows direct adjustment of the modulator output amplitude, as discussed in section 5.3.2. The POWER switch controls all power to the ST-8000A.

5.3.5 Power Supply

All circuits of the ST-8000A are powered by a regulated DC power supply. The voltages are regulated to produce operating voltages of +5.0 VDC, +8 VDC, and -8 VDC. All DC outputs are current limited and short-circuit protected. The +5 VDC regulator integrated circuit is mounted to a rear panel heat sink. Internal cables link the power supply to other circuit assemblies.

5.3.6 Cabinet

The cabinet houses all assemblies of the ST-8000A. It includes cables, AC power circuitry, the low-voltage power transformer, and rear-panel I/O connections.

All AC power components are chosen to meet safety requirements of UL-1950 and "Host Nation" (EC, or European Community) EN-60950. This includes the rear panel AC power connector, RFI filter, AC power switch, AC voltage and frequency selector switches, fuse and fuse holder, connectors, power transformer, and wire used. AC power voltages of 115 or 230 VAC ($\pm$10%) may be used at frequencies from 47 to 440 Hz.

Rear panel connectors J1 (DATA I/O), J2 (AUDIO I/O), and J4 (REMOTE CONTROL) are military MS27508-series round connectors. An additional rear panel hole is provided for the optional Diversity connector (J5). A hole cover is included on all modems without this option.

The ST-8000A cabinet is constructed of extruded aluminum front, rear, and side panels. Top and bottom covers are aluminum sheet. All exterior aluminum surfaces have a conductive iridite finish. The combination of the heavy extrusions and iridite finish produces a durable cabinet that is strong and RFI "tight".

All rear panel I/O connections are by-passed and filtered. Key internal circuit boards use four layer construction with internal layers devoted to power and ground busses to minimize RFI generation. The recessed lips of the cabinet extrusions produce a "choke-flange" seal between the cabinet and the top and bottom covers. This minimizes RFI radiation and susceptibility. The ST-8000A exceeds FCC Part 15 and VDE RFI requirements.

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