ST8000A FSK MODEM

CHAPTER 4

THEORY OF OPERATION

4.1 GENERAL

This section describes the theory of operation of the ST8000A including the demodulator, modulator, control, front panel, and power supply. The ST8000A is an audio *Frequency Shift Keyed* (FSK) *MODEM* (MOdulator-DEModulator).

4.1.1 FSK System Application

The ST8000A is used to convert RS-232 or MIL-188 serial digital data into FSK audio tones which may then be propagated to distant stations using radio or wire lines. Digital transmit data is used to frequency modulate an audio tone. The FSK audio tone drives a radio transmitter or is connected to "telephone-type" wire lines. The FSK modem at the receiving station detects these audio tones and converts the signal back into digital data for printing, display, or storage.

4.1.1.1 FSK Radio Data Station

Figure 4.1 shows a typical radio FSK data system using the ST8000A. Each radio system includes three to five major electronic components: (1) Data Terminal, (2) Encryption Device (Optional), (3) ST8000A FSK Modem, (4) Radio Transceiver, and (5) Remote Control System (Optional).

The Data Terminal device may be as simple as a keyboard and a printer or as complicated as a computer system. Data to and from the Data Terminal is digital, using RS-232 or MIL-188 interface levels.

The Encryption Device is optional and is installed between the Data Terminal and ST8000A when used. Data into and out of the Encryption Device is also digital RS-232 or MIL-188 data. Note that, when encryption is used, only the Data Terminal and Encryption Device need be "secure units" as the ST8000A and radio transceiver process only encrypted "black" data.

The FSK Modem serves as a data format converter, converting RS-232 or MIL-188 digital data to and from FSK audio tones. The ST8000A is much like a common telephone modem in operation *except that it includes additional signal processing to compensate for distortion contributed by radio propagation*. This manual presents a detailed discussion of the ST8000A FSK Modem.

The Radio Transceiver may also be separate receiver and transmitter devices, interconnected for transmit/receive control. The radio system may operate at any radio frequency, VLF, LF, HF, VHF, UHF, etc. Data to and from the radio equipment is audio FSK tones in the range of 300 to 3000 Hz. Radio characteristics such as radio frequency and bandwidth determine data rate and tone frequencies which may be used for a given application. The Push-To-Talk (PTT) transmit/receive control of the transceiver may be controlled by the ST8000A keyline output.

Figure 4.1 RADIO FSK DATA SYSTEM

The Remote Control System is optional and may be used to set and control all ST8000A operation parameters. A typical Remote Control System is a data terminal (VT-100, for example) or a computer system. Between one and eight ST8000A (and/or 1280A) FSK modems may be controlled by one Remote Control System. Some radio data systems also include remote computer control of the radio equipment as well.

4.1.1.2 Wire Line FSK Data System

A typical Wire Line FSK Data System is shown in Figure 4.2. A wire line system is very similar to a radio data system except that the radio link is replaced by a wire line connection. A wire line system includes two to four major equipment items; (1) Data Terminal, (2) Encryption Device (optional), (3) ST8000A FSK Modem, and (4) Remote Control System (optional). The function of these items is as described above in section 4.1.1.1.

Figure 4.2 illustrates a typical 4-wire data connection. In this system, the ST8000A FSK modulator output audio is connected directly to a 600 ohm balanced-wire data line (dedicated "phone lines", for example). These wires are then connected to the distant station's demodulator FSK audio input. Tone frequencies and data rate of the sending ST8000A must match the tones and data rate of the receiving distant station's demodulator. Likewise, a second pair of 600 ohm balanced wires connect the distant station's modulator to the local station's demodulator. As before, tones and data rates must match between the two stations. Since the "transmit" and "receive" connections of each station use separate wire pairs, this system may be operated "Full Duplex" (FDX) where both stations may send and receive simultaneously.

The ST8000A may also be connected to a 2-wire data line system. The simplest 2-wire connection is to parallel the FSK output and FSK input terminals of each ST8000A (set demodulator input impedance to 10,000 ohms). With this connection, the data stations are generally operated in "Half Duplex" (HDX) mode in which only one station sends data at a time. If different tone frequency pairs are used for sending and receiving, the system may also be operated in FDX, but with bandwidth and therefore data rate restrictions.

4.1.2 Functional Description

Figure 4.3 illustrates the major sections of the ST8000A FSK Modem. The ST8000A includes a (1) Demodulator Circuit, (2) Modulator Circuit, (3) Microprocessor Control Circuit, (4) Front Panel Display and Keypad Entry Circuits, and (5) Power Supply Circuits. The entire ST8000A is contained in one shielded aluminum cabinet, approximately 17" wide (43.18 cm) by 3.5" high (8.89 cm) by 17" deep (43.18 cm). Rack mounting adapters are included so that the ST8000A may be installed in a standard 19" wide equipment rack cabinet. All external connections to the ST8000A are made via 4 (or 5 with Option -01) rear-panel MIL-style round connectors. The ST8000A front panel includes displays and LED indicators that show modem tone frequencies, data rate, and selected parameter settings. A 27-key keypad allows manual entry of data to set operational parameters. ST8000A parameters may also be set and read via the rear panel Remote Control Port (J4).

4.1.3 Internal Assemblies

ST8000A circuitry is contained in five major assemblies: (1) Modem, Assembly A1, (2) Control, Assembly A2, (3) Front Panel, Assembly A3, (4) Power Supply, Assembly A4, and (5) Cabinet, Assembly A5. Assembly A1 (Modem) contains both the demodulator and modulator circuits.

Figure 4.4 shows a pictorial description of the internal ST8000A assemblies and the required interconnecting cables. The majority of ST8000A circuitry is contained in Assemblies A1 (Modem) and A2 (Control). Assembly A2 is mounted on top of Assembly (A1), but may be pivoted upwards without removing any cable for alignment, test, and maintenance. Assembly A3 (Front Panel) is attached to the front of the cabinet. The Power Supply (Assembly A4), Power Transformer, and AC power components are mounted on the right-hand portion of the Cabinet (Assembly A5). Rear Panel I/O connectors J1, J2, J4, and J5 (Option -01) each include internal cables that connect to Assembly A1 (Modem).

Interconnecting cables and signals are diagrammed in Figure 4.5. The Control Assembly (A2) coordinates the operation of all ST8000A circuits. With the exception of the AC Power connector (J3), all external I/O (Input/Output) connections are made via the Modem Assembly (A1).

Figure 4.3 ST8000A FUNCTIONAL DIAGRAM

Figure 4.4 ST8000A INTERNAL CABLING

4.2 MODEM, Assembly A1

The majority of the ST8000A demodulator and modulator circuitry is contained on the Modem Board, Assembly A1. This circuitry will be discussed in detail using block diagrams and schematic diagrams for Assembly A1. A few circuits of the demodulator and modulator are located on other assemblies. These circuits will be identified and the reader should refer to the appropriate sections for further details.

4.2.1 Demodulator

The general circuit arrangement of the ST8000A demodulator section is shown in Figure 4.6. With the exception of receive data polarity, regeneration, and mid-bit receive clock circuits, all demodulator circuits are contained on the Modem Circuit Board (Assembly A1). Two different demodulator filters and detectors are used; (1) the "Main" demodulator for data rates between 30 and 600 baud, and (2) the "High Speed" (high data rate) demodulator for data rates between 601 and 1200 baud. Only one of the demodulator outputs are selected by control signals and passed through regeneration and clock recovery circuits to RS-232 and MIL-188 Receive Data (RXD) drivers to rear panel connector A5J1 (Data I/O).

4.2.1.1 Demodulator Input and BIT Circuits

Please refer to Figures 4.4, 4.5, 4.7, and Schematic A1787. FSK audio input from rear panel connector A5J1 (pins 10 and 12) pass through cable A5W1 to Modem connector A1J1 (pins 5 and 6). The ST8000A input signal amplitude range is -45 to +6 dBm (4.35 mV to 1.54 V rms). Transformer T2 and resistor R2 (with jumper J6) set the demodulator input impedance. With jumper J6 removed, the input impedance is 10,000 ohms $\pm$10%; with J6 installed, the input impedance is 600 ohms $\pm$10%. Device CR2 is a metal oxide varistor (MOV) protective device that prevents damage to the demodulator input circuitry from induced line transients, such as voltage spikes induced in wire lines during an atmospheric storm. CR2 is "inactive" for all data levels within specification (-45 to +6 dBm). Transformer T2 converts the balanced input audio signal to an unbalanced signal. T2 is manufactured to meet the breakdown and isolation requirements of FCC Part 68 (USA) and VDE (Germany and England).

The unbalanced signal from T2 is one input to switch U1b. When "BIT" (Built-In Test) is not in use, U1b passes the signal on to stage U2b. When BIT is active, U1b connects the demodulator input to an internal FSK test signal derived from the modulator circuits. This connection allows "internal loop-back testing". Switch stage U1a provides three different levels of loop-back test signals; 0 dBm, -20 dBm, and -40 dBm. The BIT system therefore tests the demodulator over its full dynamic range. The BIT level at 0 dBm is set by control R1. The -20 dBm and -40 dBm levels are set by attenuator resistors R15, R18, and R17. BIT loop-back test are controlled by signals "BCA" and BCB", generated by the Control Board (A2). BIT control modes are shown in Table 4.1.

Figure 4.6 DEMODULATOR BLOCK DIAGRAM

TABLE 4.1
BIT CONTROL SIGNAL

BCB	BCA	MODE
0	0	Demodulate FSK Input
0	1	BIT Loop-back @ 0 dBm
1	0	BIT Loop-back @ -20 dBm
1	1	BIT Loop-back @ -40 dBm

"0" = 0 Vdc
"1" = +5 Vdc

Stage U2b is a 2-pole low-pass filter with a voltage gain of 3.0 and a cut-off frequency of 300 Hz. This stage sets the lower frequency response of the demodulator. Stage U2a is a 2-pole high-pass filter with unity gain and a cut-off frequency of 5000 Hz. This stage limits high frequency response to prevent aliasing of the following Mark and Space digital Switched Capacitor Filters (SCF's). The combination of T2, stage U2a, and the Mark and Space filters themselves sets the upper frequency response of the ST8000A to 3000 Hz. The output of Stage U2a drives the Main Mark and Space filters (U10a and U3a) and the High Speed demodulator (U14).

4.2.1.2 Mark and Space Filters (Main Demodulator)

This section refers to Figures 4.4, 4.5, and 4.8 and Schematic Diagrams A1788, A1789, A1790, and A1791. The Mark and Space filter circuits are identical. The Mark filter will be described in detail with corresponding Space filter references parenthesized. For example, "U10b (U3b)" is a reference to U10b in the Mark filter and U3b in the Space filter.

The Mark demodulator filter has two 2-pole bandpass filter sections, separated by the gain control circuit. The two Mark filters are synchronous and tracked; each is set to the same center frequency. The "Q's" or bandwidths of the two filter sections are also coupled. The device used for the Mark filter is a digital "Switched Capacitor Filter" (SCF).

SCF devices are characterized by very stable operating parameters and a center frequency that is directly proportional to the frequency of the applied clock signal. Thus, the demodulator Mark (and Space) filter center frequencies are set electronically by changing the frequency of the filter clock signal MCLK (SCLK). This clock signal is generated by synthesizers on the Control Circuit Board (Assembly A2). The "Q" or bandwidth of the Mark (Space) filters is set by switch selection of precision resistors. Switch selection of Q is also set by the Control Board (A2).

Device U10a (U3a) is the first 2-pole Mark (Space) filter stage. Control R52 (R69) is adjusted so that the filter center frequency is exactly 1/50th of the input clock frequency. This and the corresponding control for stage U10b (U3b) - R63 (R82) - are the only adjustments required for filter alignment. The "Q" of stage U10a (U3a) is set by U11 (U4) selection of precision resistors R67, R68, and R70 through R75 (R30, R33 through R38 and R83). This provides 8 different unique "Q" settings via control signals MQ1, MQ2, and MQ3 (SQ1, SQ2, SQ3). Switch stage U29b (U21c) provides a second "Low-Q" range, selected by control signal MQL (SQL). Another set of 8 "Q" values are available by setting MQ1, MQ2, and MQ3 (SQ1, SQ2, SQ3) when MQL is set for "Low-Q". Thus a total of 16 values of Mark (Space) filter "Q" or bandwidth are available.

Stage U19b (U13b) is a 2-pole low-pass filter with unity gain and cut-off frequency of 8 kHz. This filter removes the digital switching transients from the output of SCF stage U10a (U3a). The output of U19b (U13b) is used to drive the Mark and Space bar graphs and the peak detector for the Automatic Mark Hold (AMH) and gain control circuits. Stages U19c and U20 (U13c and U12) provide variable gain which may be set digitally in 6 dB increments from 0 dB to +42 dB via control signals DGA, DGB, and DGC. The same gain is set for both Mark and Space filter channels. See Section 4.2.1.5 and Table 4.5 for further discussion of the gain control circuits.

Stage U19d (U13d) is a "gain compressor" amplifier. The output of the gain control stage (U19c or U13c) varies in 6 dB increments as gain is automatically adjusted. Stage U19d (U13d) compresses these 6 dB gain-change increments down to changes of approximately $\pm$0.5 dB. This stage does not cause radical clipping of the input signal waveform. The output signal to the second Mark (Space) filter stage is therefore a constant +10 dBm $\pm$0.5 dB, for all input signal levels between -45 dBm and +10 dBm.

Stage U10b (U3b) is the second 2-pole Mark (Space) filter. The MCLK (SCLK) filter clock from the Control Board (A2) has a frequency that is 50 times that of the desired Mark (Space) center frequency. The same clock signal feeds both stage U10a and U10b (U3a and U3b). The Mark and Space clock synthesizers on the Control board generate a TTL-level clock signal that may be set from 15,000 Hz to 150,000 Hz in 25 Hz increments, providing Mark or Space filter settings of 300 to 3000 Hz in 0.5 Hz increments. MCLK and SCLK are related to the chosen Mark and Space frequency as shown in formulas (1) and (2):

$$\text{MCLK} = 50 \times (\text{MARK Frequency}) \quad (1)$$

$$\text{SCLK} = 50 \times (\text{SPACE Frequency}) \quad (2)$$

As in the first stage, switches U28 and U29a (U22 and U21b) set the "Q" if the Mark (Space) second stage filter. A total of 16 values of "Q" or bandwidth may be set using the MQ1, MQ2, MQ3, and MQL (SQ1, SQ2, SQ3, SQL) control signals. Stage U19a (U13a) is a 2-pole low-pass filter with unity gain and cut-off frequency of 8 kHz, again to remove switching transients from the SCF output signal.

Although filter "Q" is the controlled parameter of the Mark and Space filter circuit configuration, the front panel entry parameters are Mark and Space Frequency (MARK and SPACE) and Data Rate (BAUD). The Control Board (A2) sets the filter Q based on Formula (3).

$$Q = \frac{\text{Center Frequency}}{\text{Bandwidth}} = \frac{\text{MARK}}{1.5 \times \text{BAUD}} = \frac{\text{SPACE}}{1.5 \times \text{BAUD}} \quad (3)$$

The 2-stage composite values of Mark and Space filter "Q" are shown in Table 4.2. The Mark

and Space filter Q's are set independently. For reference, the equivalent bandwidth for a 2000 Hz center frequency is shown in Table 4.2.

TABLE 4.2
MARK and SPACE "Q" VALUES

MQ1 SQ1	MQ2 SQ2	MQ3 SQ3	MQL SDL	Q	BW @ 2000 Hz
1	1	1	0	2.1	952 Hz
1	1	0	0	2.3	870 Hz
1	0	1	0	2.6	769 Hz
1	0	0	0	2.9	690 Hz
0	1	1	0	3.2	625 Hz
0	1	0	0	3.7	540 Hz
0	0	1	0	4.5	444 Hz
0	0	0	0	5.9	339 Hz
1	1	1	1	6.1	328 Hz
1	1	0	1	7.9	253 Hz
1	0	1	1	9.9	202 Hz
1	0	0	1	11.7	171 Hz
0	1	1	1	13.7	146 Hz
0	1	0	1	17.5	114 Hz
0	0	1	1	23.2	86 Hz
0	0	0	1	33.6	60 Hz

4.2.1.3 Peak Detector

This section refers to Figure 4.8 and Schematic Diagram A1792. The outputs of the first stage Mark filter (U19b) and Space filter (U13b) are a filtered but not gain-controlled version of the input FSK signal. These signals are peak detected in stages U27a and U27d, filtered by C60, and buffer amplified by stages U27b and U27d. Control R159 calibrates the AMH and gain control levels. Stage U27c sets a +30 dB output to drive low-level sections of the AMH and gain control circuits. The non-buffered peak-detected output of C60 also connects to the optional Diversity circuit (Option -01).

4.2.1.4 Automatic Mark Hold (AMH)

Refer to Figure 4.8 and Schematic Diagram A1793. The output from R159 (A1792) drives logarithmic converter stage U8. This device generates ten separate outputs that switch in 3 dB increments as the input amplitude varies from -27 dBm to 0 dBm. Log converter stage U7 is driven by the +30 dB output of stage U27c. Its outputs switch in 3 dB increments from -54 to -30 dBm. The two log-converters (U8 and U7) therefore provide switched output increments of 3 dB from -57 dBm to 0 dBm.

The Automatic Mark Hold (AMH) detector circuit uses alternates outputs from U8 and U7, providing 6 dB increments for the AMH threshold. Switch SW1 may be set for AMH thresholds from -42 dBm to 0 dBm (see Table 4.3). As a given amplitude threshold is exceeded, the corresponding output of U8 or U7 switches from opne circuit to ground. When this occurs at the output selected by SW1, the input to diode D5 is pulled low and stage U9b is switched to an output "0" state - a data signal is present. When the input signal amplitude is consistently below the value set by SW1, D5 is turned OFF and capacitor C20 is charged through switch SW2 and resistors R6 through R14. When the charging voltage on C20 exceeds 2.5 volts DC, stage U9b output switches to "1" (+5V), indicating Loss Of Signal (LOS). Resistors R6 through R14 are chosen so that the AMH turn-off delay may be set in 0.5 second increments from 1.0 to 5.0 seconds (see Table 4.4). Stage U9a allows defeat of the AMH circuit by the Control Board (A2) via control signal AMHC. Switch U21a is activated when the "High Speed" demodulator is used, setting an AMH level of -42 dBm for all data rates greater than 601 baud. AMH input amplitude threshold values for SW1 settings are shown in Table 4.3. AMH delay values vs SW2 settings are shown in Table 4.4.

TABLE 4.3
AMH SW1 THRESHOLD SETTINGS

SW1 SWITCH SECTION								
1	2	3	4	5	6	7	8	AMH Threshold
0	0	0	0	0	0	0	1	-42 dBm
0	0	0	0	0	0	1	x	-36 dBm
0	0	0	0	0	1	x	x	-30 dBm
0	0	0	0	1	x	x	x	-24 dBm
0	0	0	1	x	x	x	x	-18 dBm
0	0	1	x	x	x	x	x	-12 dBm
0	1	x	x	x	x	x	x	-6 dBm
1	x	x	x	x	x	x	x	0 dBm

"0" = Switch Section "Open"
"1" = Switch Section "Closed"
"x" = Switch Section Position Does Not Matter

TABLE 4.4
AMH SW2 DELAY SETTINGS

SW2 SWITCH SECTION

1	2	3	4	5	6	7	8	AMH Delay after LOS
0	0	0	0	0	0	0	1	1.0 Seconds
0	0	0	0	0	0	1	0	1.5 Seconds
0	0	0	0	0	1	0	0	2.0 Seconds
0	0	0	0	1	0	0	0	2.5 Seconds
0	0	0	1	0	0	0	0	3.0 Seconds
0	0	1	0	0	0	0	0	3.5 Seconds
0	1	0	0	0	0	0	0	4.0 Seconds
1	0	0	0	0	0	0	0	4.5 Seconds
0	0	0	0	0	0	0	0	5.0 Seconds

"0" = Switch Section "Open"
"1" = Switch Section "Closed"

4.2.1.5 Gain Control

Refer to Figure 4.8 and Schematic Diagram A1793. The gain control circuit uses the remaini outputs of log-converters U8 and U7. Thus, the gain control is also set in 6 dB increment but offset by 3 dB from AMH settings. Resistor pack RN1 and capacitors C38 through C45 smoo the rapid transition outputs of U8 and U7. Stage U18 logically combines the eight log-convert outputs into a three-line control signal to set the gain of Mark filter stages U20/U19c a Space filter stages U12/U13c (DGA, DGB, and DGC). The Control Board (A2) reads this level determine the input signal amplitude. Gain control characteristics are summarized in Table 4.

TABLE 4.5
GAIN CONTROL

GAIN CONTROL			U19c & U13c		
DGA	DGB	DGC	A_{vo}	A_{dB}	V_{in} to Demodulator
0	0	0	1	0	+3 dBm
0	0	1	2	6	-3 dBm
0	1	0	4	12	-9 dBm
0	1	1	8	18	-15 dBm
1	0	0	16	24	-21 dBm
1	0	1	32	30	-27 dBm
1	1	0	64	36	-33 dBm
1	1	1	128	42	-39 dBm and lower

"0" = Logic Low (0 V)
"1" = Logic High (+5 V)

4.2.1.6 Mark and Space Tone Detectors

Refer to Figure 4.9 and Schematic Diagrams A1794 and A1795. Stages U37a and U37d (U30a and U3 for Space) full-wave rectify the Mark (Space) filter output. Stage U37b (U30b) is a 2-po low-pass filter that removes audio frequency components from the rectified signal. Stage U3

(U30c) is a buffer amplifier that supplies the Undetected Mark (Undetected Space) signals rear panel connector A5J1 (through Modem connector J3-1 and J3-2)

4.2.1.7 Mark and Space Data Low-Pass Filters

Refer to Figure 4.9 and Schematic Diagrams A1794, A1795, and A1796. Stages U38 (Mark) and U (Space) are 7-pole linear-phase digital Switched Capacitor Filters (SCF's). The cut-o frequency of each is set by the frequency of the filter clock signal (LPCLK) generated by synthesizer on the Control Board (A2). The clock frequency is 96 times the desired low-pa cut-off frequency of the filter. The Control Board (A2) microprocessor computes the requir Data Low-pass Filter clock frequency according to formula (4):

$$LPCLK = 96 \times 0.75 \times (\text{Baud Rate}) = 72 \times (\text{Baud Rate}) \quad (4)$$

Controls R199 (Mark) and R118 (Space) provide DC offset compensation of the detector a low-pass filter circuits. Stages U39a (Mark) and U39b (Space) are unity-gain low-pass filte to smooth the outputs of stages U38 and U31.

4.2.1.8 Diversity Circuit (Option -01)

Refer to Figure 4.9 and Schematic Diagram A1796. This circuitry is optional and only includ if the ST8000A is purchased with "Option -01" installed. When Diversity Option -01 installed, an additional rear panel connector (A5J5) is provided for connection to a secc ST8000A FSK Modem.

Stages U40d and U40a (U40b and U40c for Space) act as analog "wired-OR gates" and accept t dominant of the two detected Mark or Space signals. The Diversity feature is enabled by swit U46. U46 also combines the Peak Detected outputs of C60 of both modems and the AMH outpu (U9b) of both modems. Jumpers J13 and J14 must be in the "DIV" positions when diversity used.

When Option -01 is not installed in the ST8000A, jumpers J13 and J14 should be placed in t "NDIV" positions. Diversity components within the dotted lines of A1796 and rear par connector A5J5 are not installed if Option -01 is not included.

4.2.1.9 Data Detectors

Refer to Figure 4.9 and Schematic Diagram A1797. The detected Mark and Space pulses from J and J14 drive three different pulse detectors. Stages U48a, U48b, and U48d provide Mark-On detection. Stage U48c provides Mark/Space detection. Stages U49a, U49b, and U49c provi Space-Only detection. The operation of the Mark-Only and Space-Only detectors is identica The Mark-Only detector will be described with Space-Only references parenthesized.

The input Mark data from J13 (J14) is a positive voltage pulse (0 to +3 volts DC). The circu of D39, C81, and R224 (D45, C86, R229) form a positive peak detector which tracks the positi peak of the detected Mark (Space) pulse. Stage U48a (U49a) is an isolation amplifier to preve loading of C81 (C86). Components D38, C82, and R221 (D44, C85, R233) form a negative pe detector that measures the difference between the minimum voltage of the Mark (Space) pulse a the +8 VDC power supply. U48b (U49b) is also an isolation amplifier to prevent loading of C (C85). The positive peak amplitude (U48-1, U49-1) and negative peak output (U48-7, U49-7) a summed in resistors R218 and R219 (R235, R236) to produce a bias voltage at U48-12 (U49-10) th is mid-way between the maximum and minimum values of the Mark (Space) data pulse. The origin Mark (Space) data pulse is connected to the other input of U48d (U49c) so that the output U48-14 (U49-8) is a replica of the detected Mark (Space) pulse, but with "zero-signal" bias removed. Thus, the circuit will detect Mark or Space data even when an interfering signal noise causes biasing during the "non-Mark" ("non-Space") times of the data stream. Componen D36, D37, R216, and D35 (D48, D47, R239, D46) provide a "clamp" that prevents the loss of threshold switching reference during long periods of continuous Mark or Space states.

Stage U48c provides differential Mark/Space data pulse detection. In this circuit, the two da signals are differentially compared, producing a data output at U48-8. Components D40 - D4 C83, C84, R217, and R220 provide an "Automatic Threshold Correction" that compensates f moderate differential fading. The Mark/Space detector and ATC circuit is most efficient at da rates of 100 baud and less.

Only one detector output is are selected by switch U41. Four different modes of detection a selected by control signals DMA and DMB from the Control Board (A2). The four detector mod are shown in Table 4.6.

TABLE 4.6
DETECTOR MODES

DMB	DMA	DETECTOR MODE
0	0	M/S using the MO & SO Detectors
0	1	Mark-Only
1	0	Space-Only
1	1	M/S using M/S Detector and ATC

The differential output of U41 is combined in U50a and the resulting pulse signal is amplifi and limited in slicer stage U50b. R238, D49, and D50 convert the bi-polar output of U50b TTL levels (Mark = +5V).

4.2.1.10 High Speed Demodulator

Refer to Figure 4.9 and Schematic Diagrams A1799 and A1800. The High Data Rate demodulat section is only used when the demodulator data rate is between 601 and 1200 baud.

Input audio data from the input low-pass filter (U2-1) is converted by mixer stage U14 and U2 to an intermediate frequency (IF) of 10,000 Hz. A synthesizer on the Control Board (A provides a local oscillator injection signal (HSCLK) that is 10,000 Hz higher in frequency th the mid-frequency of the selected Mark and Space frequencies. For example, if Mark and Spa are specified as 1500 Hz and 2500 Hz, respectively, the mid-frequency is 2000 Hz and the HSC frequency is set to 12,000 Hz. HSCLK frequency is set as defined by formula (5).

$$HSCLK = 10{,}000 + \frac{(Mark + Space)}{2} \qquad (5)$$

The IF output of the mixer drives an 8-pole, 4-stage Butterworth bandpass filter made up stages U32, U33, U24, and U15. Jumpers J11, J12, J9, and J8 allow stage-by-stage alignment this filter. The resulting filter has a bandwidth of 2150 Hz and an ultimate stop-ba rejection of over 60 dB. One control is provided to align each filter stage (R133, R138, R14 R95). Jumpers J12, J11, J9, and J8 are used for filter alignment and must be installed f normal operation of the filter.

The output of the bandpass filter drivers the limiter stage U16b. This stage provides constant amplitude output to the detector, U25. U25 is a Phase-Locked Loop (PLL) detector wi center frequency set by control R150. Detected high-speed data is output from U25 (Mark = +5V

The detected data output also drives level-shifter stage U16a and switch U17. U17 provides Ma and Space signal outputs to drive the front panel bar graphs when the "High Speed Demodulato section is used.

4.2.1.11 Detector Selection and Received Data Output

Refer to Figure 4.9 and Schematic Diagram A1798. Either the detected data from the "mai demodulator (from U50b) or the "High Speed" demodulator (U25) is selected by digital swit stage U53. Detector output is selected by the HSLS signal from the Control Board (A2). T RXD output signal is passed to the Control Board (A2) where is is further processed f Normal/Reverse polarity switching, Receive Regeneration, and Receive Mid-bit Clock recovery (s Section 4.3.6).

After polarity adjustment and regeneration, the received data again passes back to the Moc Board (A1) to U55 (pin 4). Stage U55b is a signal gate for the Automatic Mark Hold (AM feature. The AMH signal from U9b either allows received data to pass to the output amplifie (AMH = 0) or locks the output signal to a constant Mark condition (AMH = 1).

Following the AMH gate, received data passes through U54a or U55a and U54b to generate MIL-1 and RS-232 RXD outputs, respectively. Components R244, D51, and D52 limit the MIL-188 outp voltage to ±6 VDC.

The AMH signal is also used to generate the Carrier Detect (CD) output signal on the Data I connector A5J1. Stage U55c and jumper J15 allow selection of either polarity for Carrier Dete output (LOS = +V or LOS = -V). Stage U54d provides an RS-232/MIL-188 compatible CD outp signal. Set the polarity to "LOS = -V" for an RS-232 compatible DCD output.

4.2.2 Bar Graph Outputs

Refer to Figure 4.16 and Schematic Diagram A1801. The circuitry for the front panel bar grap is split between the Modem Board (A1) and the Front Panel Board (A3). Only the circuits locat on the Modem Board will be discussed at this time. See section 4.4.1 for further details the front panel bar graph indicators themselves.

The front panel bar graph indicators serve several functions. When receiving data at 600 ba or less, the bars indicate the amplitude and tuning accuracy of signals that pass through t first stages of the Mark and Space demodulator channel filters. The bars are accurate calibrated and show the instantaneous input signal level of the Mark and Space signals. Wh the front panel is set to display "Channel 2" (CH2), the bars indicate the amplitudes of t Mark and Space modulator output signals.

The receive Mark and Space signals are selected by U43 and U44 to provide the correct signa to the bars. Below 600 baud, the receive signals are supplied from U19-7 (Mark filter) a U13-7 (Space filter). Above 600 baud, signals are supplied from U17-14 (Mark) and U17- (Space). These outputs are selected by U43a and U43b under control of the HSLS control signa

The modulator output signal from U5-1 is switched between Mark and Space by U43c and transm data (TTLTXD) from the Control Board (A2).

The choice of bar graph display of receive signals (Channel 1) or transmit signals (Channel is controlled by switch U44 and the CHSEL control signal from the Control Board (A2).

The selected Mark and Space signals are rectified in stages U45a (Mark) and U45d (Space Buffer amplifiers U45b and U45c provide the Mark and Space tuning bar signals to the front par display. Controls R210 and R215 allow for low-amplitude calibration of the tuning bars.

The balance of the tuning bar circuit is discussed in section 4.4.1.

4.2.3 Modulator and Keyline

Refer to Figure 4.10 and Schematic Diagrams A1802 and A1803. As can be seen from Figure 4.1 the modulator circuit is split between the Modem Board (A1) and the Control Board (A2). On the circuitry on the modem will board is discussed in this section. Control Board modulat circuitry is discussed in section 4.3.4.2.

A modulator frequency synthesizer on the Control Board (A2) generates a TTL-level pulse tra (TFSK) whose frequency is 50 times that of the desired output audio tone. Transmit da shifting of the Mark/Space frequency is included within this synthesizer. The 50x FSK da drives counter stage U26 and Read Only Memory (ROM) U36. ROM U36 is programmed to output different 8-bit digital values, one for each of the 50 steps of a digitized sine wave. The R output is latched in U35 and converted to analog form in the Digital-to-Analog Converter (DA U34. This analog signal is filtered by stage U5b. The output at U5-7 is a smoothed, 50-st approximation of a sine-wave. Use of 50 steps assures that distortion is very low. A harmonics are less than -40 dBm and all spurious products are suppressed below -60 dBm at t FSK modulator output. The TFSK signal frequency is set as in forumla (6):

TFSK = 50 x (Transmit Mark Tone) -or- = 50 x (Transmit Space Tone) (6)

The "FSKCLK" signal is fed back to the synthesizer circuit to assure that data transitions occ

when the sine wave slope is zero. Modulator tone output may be muted by installation of jump
J10. The MUTE signal is generated by the Control Board (A2).

The output of U5-7 provides a +2 dBm BIT test signal (to switch U1). The output also pass
to the Front Panel A3) to the Output Level potentiometer control. The output of this contr
then passes back to the Modem Board (A1) to stage U5a, U5a provides a voltage gain of 5 a
drives the balanced output amplifier, U6a and U6b. Resistors R45 and R46 and transformer
provide a 600 ohm balanced modulator output. As in the case of the demodulator input circui
MOV device CR1 provides protection against line-induced transients. Transformer T2 meets t
insulation and isolation requirements of FCC Part 68 and VDE.

The MUTE signal also drives the keyline relay, K1 through transistor Q1. This relay provid
isolated contacts for the keyline output on rear panel connectors A5J1 (J1-15 and J1-16) a
A5J2 (J2-5 and J2-6). The keyline may also be connected as a "phantom circuit" where t
center-tap of the modulator output transformer is switched to ground or to a DC voltage. So
radio circuits require this form of transmit/receive control. "Phantom keyline" control is s
by jumper J7. J7 is set "open" unless a "phantom" keyline circuit is required.

4.3 CONTROL ASSEMBLY A2

The Control Board (A2) is a microprocessor based sub-assembly that contains all Modem Boa (A3) filter frequency synthesizers, the AFSK transmit tone synthesizer, control bit latche and the front panel interface circuits. In addition, the Transmit Data (TXD) and Recei data (RXD) polarity, regeneration, and receive clock recovery circuits are included on th board.

The following sections contain detailed descriptions of the Control Board circu illustrated in Schematic Diagrams A1806 to A1827. Refer to the block diagram in Figure 4. and the schematic diagrams during this discussion.

4.3.1 Microprocessor Controller

The ST-8000A Control Board (Assembly A2) uses a conventional dedicated microprocess architecture with 32K bytes of read only (EPROM) memory for firmware storage, 2K byt of read/write (RAM) memory, and 2K bytes of electrically alterable (EEPROM) memory. T Z80A microprocessor uses a 4.9152 MHz clock (PCLK) generated by a TTL crystal oscillator. T 330 ohm pullup resistor on U15-6 ensures that the clock signal meets the minimum high volta level requirements of the Z80A. The Control Board uses both memory mapped and I/O port mapp peripheral devices and latches. The Z80A operates with no wait states.

Note the 10K ohm pullup resistors on the microprocessor write, WRM.L (U15-22), and read, RDM (U15-21), control signals. These resistors hold these control lines high when the process is in the power on reset condition since these control lines are in a high impedan tri-state condition at that time. Without the pullup resistors, a false memory wri signal might corrupt the parameters stored in the non-volatile parameter storage memory (U2

The Z80A has two maskable interrupt sources: the serial channel controller interrupt, INT (U56-12), and the front panel keypad interrupt, KBINT (U64-1). These two interrupt sourc are combined by a 2 input NAND gate (U56) to produce a common interrupt signal to drive t microprocessor interrupt input (U15-16). The front panel interrupt signal, KBINT, must inverted since it is an active high signal. When an interrupt occurs, the microprocess must poll both the serial controller (U66) shown in Schematic A1815 and the front par controller to see which device requested the interrupt.

The non-maskable interrupt, NMI (U15-17), provides a real time clock reference for correct calculating ST-8000A timing delays. This square wave timing signal is generated by t programmable timer (U1) in Schematic A1807, and it is set for a 1.0 ms period.

The RESET (U9-5) and RESET.L (U9-6, U15-26) signals are generated by a "deadman" tim and power on reset circuit (U9). During normal ST-8000A operation, the deadman tim reset signal, SANITY.L (U9-7), is pulsed low periodically by the microprocessor. Should sc abnormal situation cause the microprocessor to cease operation, the deadman timer will for a hardware reset of the ST-8000A. When a reset occurs, the RESET and RESET.L outputs a pulsed low and high, respectively, for approximately 0.25 seconds.

Figure 4.11 CONTROL BLOCK DIAGRAM

Due to the number of latches and devices on the control board, the Z80A read and wri control signals are buffered by two buffer gates to generate RD.L (U10-8) and WR.L (U10-11 respectively. Note that the un-buffered signals RDM.L and WRM.L are connected directly the EPROM (U4), the RAM (U3), and the EEPROM (U2).

4.3.2 System Clocks

A programmable timer (U1) in Schematic A1807 generates the reference frequency for all the frequency synthesizers, CKREF (U1-10), the low pass filter clock, LPCLK (U1-13), a the microprocessor real time reference clock, NMI (U1-17).

All of the ST-8000A frequency synthesizers are referenced to the same 4.9152 MHz cryst oscillator that drives the microprocessor clock, PCLK (U1-9,15). One 16 bit programmab timer divides PCLK by 6 to generate the 819,200 Hz reference clock, CKREF (U1-10), used all filter and transmit tone synthesizers. In addition, the 4.9152 MHz clock is divided various constants to generate the low pass filter clock, LPCLK (U1-13), for the Modem Boa (A1). An inverting buffer is provided on CKREF to increase the fan-out capability.

A separate 6.144 MHz oscillator reference is used for the NMI clock. This clock is divid by 6144 to produce a 1000 Hz square wave signal, NMI (U1-17), for the 1.0 ms real time cloc Note that the NMI signal is disabled until the NMI control signal, NMIENA (U1-16), is s high.

The block diagram in Figure 4.12 identifies the significant Control Board (A2) clo signals.

4.3.3 Memory and I/O Address Map

The microprocessor memory is divided into memory mapped and I/O port mapped sections. A memory and I/O port address decoding is illustrated in Schematic Diagrams A1806 and A1807

Decoding for the firmware memory (U4) is illustrated in Schematic A1806. Memory address b 15, A15 (U15-5), and memory request, MREQ.L (U15-19) are combined by a two input OR gate (U1 to generate the EPROM chip select signal (U4-20) when both signals are low.

Except for the firmware memory chip select, all memory and I/O address decoding contained in Schematic A1807. A 3-to-8 line decoder (U11) is the primary memory mapped devi decoder, and it is enabled by the combination of address bit 15, A15 (U11-6), high and memo request, MREQ.L (U11-5), low. A second address decoder (U12) provides additional decodi for several write only latches when it is enabled by write, WR.L (U12-4), low and o memory address select line (U11-13) low.

The I/O port mapped devices are decoded by two 3-to-8 line decoders (U13, U14). T devices on the first decoder (U13) are both I/O input and output peripheral devices whi those on the second decoder (U14) are I/O output only latched registers.

The memory and I/O address map for the ST-8000A control board is summarized in Tables 4
and 4.8 below (all addresses are shown in HEX format):

TABLE 4.7
MEMORY MAPPED ADDRESSES

ADDRESS	REF	DESCRIPTION	R/W
0000H - 7FFFH	U4-20	27256 EPROM for firmware storage	READ
8000H - 87FFH	U3-18	2K x 8 RAM for temporary storage	READ/WRITE
8800H - 8FFFH	U2-18	2K x 8 EEPROM for parameter storage	READ/WRITE
A000H - A007H	U12-5	Synthesizer latches	WRITE
A000H	U41-11	MARK transmit tone, low byte	WRITE
A001H	U43-11	MARK transmit tone, high byte	WRITE
A002H	U40-11	SPACE transmit tone, low byte	WRITE
A003H	U42-11	SPACE transmit tone, high byte	WRITE
A004H	U45-11	MARK filter synthesizer, low byte	WRITE
A005H	U46-11	MARK filter synthesizer, high byte	WRITE
A006H	U49-11	SPACE filter synthesizer, low byte	WRITE
A007H	U50-11	SPACE filter synthesizer, high byte	WRITE
E000H	U5-1,19	Transmit delay switch SW1	READ
E800H	U6-1,19	Transmit delay switch SW2	READ

TABLE 4.8
I/O PORT MAPPED ADDRESSES

PORT	REF	DESCRIPTION	I/O
00H	U66-33	Serial controller	INPUT/OUTPUT
08H			
10H	J8-12	Front Panel select (FP_L)	INPUT/OUTPUT
18H	U1-21	Programmable timer	INPUT/OUTPUT
20H	U8-1,19	Unit Address switch SW4	INPUT
28H	U7-1,19	Remote Port rate switch SW3	INPUT
30H	U44-1,19	AMHO, level, RS232/MIL, KBINT, TXD	INPUT
38H - 3FH	U14-5	Misc. control latches	OUTPUT
38H	U47-11	MARK and SPACE filter Q latch	OUTPUT
39H	U48-11	NMI, Regen, RX/TX control latch	OUTPUT
3AH	U51-11	AMHC, Det. Mode, Channel, Mute, BIT	OUTPUT
3BH	U9-7	Sanity timer	OUTPUT
3CH	J8-13	Front panel LED latch 0 (LED0_L)	OUTPUT
3DH	J8-14	Front panel LED latch 1 (LED1_L)	OUTPUT
3EH	U52-11	High speed RX synthesizer, low byte	OUTPUT
3FH	U53-11	High speed RX synthesizer, high byte	OUTPUT

4.3.4 EPROM, EEPROM, and RAM Memory

The ST-8000A memory address map is summarized in Table 4.9 below:

TABLE 4.9
MEMORY ADDRESSES

ADDRESS	REF	DESCRIPTION	R/W
0000H - 7FFFH	U4-20	27256 EPROM for firmware storage	READ
8000H - 87FFH	U3-18	2K x 8 RAM for temporary storage	READ/WRITE
8800H - 8FFFH	U2-18	2K x 8 EEPROM for parameter storage	READ/WRITE

Schematic A1806 illustrates the firmware EPROM (U4), the non-volatile parameter EEPROM (U2 and the 2k x 8 RAM memory (U3). The ST-8000A firmware is loaded in an industry standard 3 x 8 byte EPROM with 250 ns access time. In this unit, address bit 15, A15 (U15-5) selec either the EPROM when A15 is low or the EEPROM and RAM when A15 is high. Note that t memory request signal, MREQ.L (U15-19) enables memory decoding only during memory acce cycles, not during I/O port access cycles. The microprocessor read signal, RDM.L (U15-21 is connected directly to the EPROM (U4-22), RAM (U3-20), and EEPROM (U2-20) output enab inputs. The microprocessor write signal, WRM.L (U15-22), is connected to the RAM write inp (U3-21) and the EEPROM write input (U2-21).

4.3.5 Memory Mapped Latches and Buffers

The ST-8000A controls the MARK and SPACE transmit tone and bandpass filter synthesize through memory mapped latches. In addition, the transmit delay time switch setting is re from memory mapped switch buffers. These buffer addresses are summarized in Table 4.10 belo

TABLE 4.10
MEMORY MAPPED LATCHES AND BUFFERS

ADDRESS	REF	DESCRIPTION	R/W
A000H - A007H	U12-5	Synthesizer latches	WRITE
A000H	U41-11	MARK transmit tone, low byte	WRITE
A001H	U43-11	MARK transmit tone, high byte	WRITE
A002H	U40-11	SPACE transmit tone, low byte	WRITE
A003H	U42-11	SPACE transmit tone, high byte	WRITE
A004H	U45-11	MARK filter synthesizer, low byte	WRITE
A005H	U46-11	MARK filter synthesizer, high byte	WRITE
A006H	U49-11	SPACE filter synthesizer, low byte	WRITE
A007H	U50-11	SPACE filter synthesizer, high byte	WRITE
E000H	U5-1,19	Transmit delay switch SW1	READ
E800H	U6-1,19	Transmit delay switch SW2	READ

Each of the synthesizers requires a 16 bit constant to set the output square wave frequenc A detailed description of these registers is presented in a subsequent section and only t memory addresses are listed here. Two other modem square wave signals are generated on t control board; the high speed synthesizer, HSCLK (U23-19), and the low pass filter cloc LPCLK (U64-12). The HSCLK synthesizer uses I/O mapped latches while LPCLK is a square wa signal generated by the on board programmable timer (U1).

The ST-8000A reads the transmit delay setting as a 16 bit value set by switches S and SW2 in Schematic A1810. For both switches, the OPEN or OFF position is read as a T 1 or high signal while CLOSED or ON is read as TTL 0 or low signal.

4.3.6 I/O Mapped Peripherals

The ST-8000A uses I/O input and output addresses for several peripheral devices a control bit latches. An I/O memory map is shown in Table 4.11.

TABLE 4.11
I/O PORT MAPPED PERIPHERALS

PORT	REF	DESCRIPTION	I/O
00H	U66-33	Serial controller - Regen control	INPUT/OUTPUT
01H	U66-33	Serial controller - Regen data	INPUT/OUTPUT
02H	U66-33	Serial controller - Remote control	INPUT/OUTPUT
03H	U66-33	Serial controller - Remote data	INPUT/OUTPUT
10H	J8-12	Front Panel controller - data	INPUT/OUTPUT
11H	J8-12	Front Panel controller - control	INPUT/OUTPUT
18H	U1-21	Programmable timer - CKREF clock	INPUT/OUTPUT
19H	U1-21	Programmable timer - LPCLK clock	INPUT/OUTPUT
1AH	U1-21	Programmable timer - NMI clock	INPUT/OUTPUT
1BH	U1-21	Programmable timer - control register	INPUT/OUTPUT
20H	U8-1,19	Unit Address switch SW4	INPUT
28H	U7-1,19	Remote Port rate switch SW3	INPUT
30H	U44-1,19	AMHO, level, RS232/MIL, KBINT, TXD	INPUT
38H	U47-11	MARK and SPACE filter Q latch	OUTPUT
39H	U48-11	NMI, Regen, RX/TX control latch	OUTPUT
3AH	U51-11	AMHC, Det. Mode, Channel, Mute, BIT	OUTPUT
3BH	U9-7	Sanity timer	OUTPUT
3CH	J8-13	Front panel LED latch 0 (LED0_L)	OUTPUT
3DH	J8-14	Front panel LED latch 1 (LED1_L)	OUTPUT
3EH	U52-11	High speed RX synthesizer, low byte	OUTPUT
3FH	U53-11	High speed RX synthesizer, high byte	OUTPUT

Schematic A1815 illustrates the dual channel serial controller (U66) used for receive da regeneration and the remote control port. This serial controller contains internal baud ra generators to independently set the data rate for the remote control port and receive da regeneration. For a detailed description of the regeneration circuit and remote contr circuit, see Sections 4.3.12 and 4.3.13, respectively.
The front panel controller is a programmable keyboard/display interface device described section 4.4.3. For this discussion, note that the interface requires two I/O addresse one for control and the other for data.

The programmable timer, U1, in Schematic A1807, contains three 16 dividers. The registers are loaded at the I/O addresses shown above to set the selected low pa filter cutoff frequency, LPCLK (U1-13), and the two fixed rate clocks: NMI (U1-01) and CKR (U64-12).

The remaining I/O address assignments control various operational latched output bit
The sections below detail each of these registers.

4.3.6.1 UNIT ADDRESS and REMOTE PORT RATE

The Unit Address switch, SW4 in Schematic A1809, sets the ST-8000A unit address. This regist
is an 8 bit, read only input.

The remote port rate switch, SW3 in Schematic A1809, selects the data rate for the remo
control port. This registers is an 8 bit, read only input.

TABLE 4.12
UNIT ADDRESS AND REMOTE PORT DATA RATE

PORT	REF	DESCRIPTION	I/O
20H	U8-1,19	Unit Address switch SW4	INPUT
28H	U7-1,19	Remote Port rate switch SW3	INPUT

4.3.6.2 RECEIVE SIGNAL LEVEL and STATUS BITS

The microprocessor can read the audio level of the receive signal and the Automatic Ma
Hold (AMH) condition with an I/O mapped buffer shown in Schematic A1808. In addition, th
register contains the state of the transmit data RS232/MIL188 option jumper setti
in Schematic A1816, and the remote port RS232/MIL188 option jumper setting in Schemat
A1815.

The state of KBINT (U64-2) in Schematic A1806 is also provided in this register. Since t
different interrupt sources are combined in a single microprocessor interrupt signal, th
register may be read to determine whether the interrupt came from the front par
keyboard/display controller or the serial controller. The state of the TXD input may be re
in this register as well.

TABLE 4.13
RECEIVE SIGNAL LEVEL and STATUS BITS

PORT	REF	DESCRIPTION	I/O
30H	U44-1,19	AMHO, level, RS232/MIL, KBINT, RXD	INPUT

The bit assignments in this register are shown in Table 4.14.

TABLE 4.14
BIT ASSIGNMENTS - CONTROL REGISTER
Input: LEVEL.L

BIT	REF	CONN	DESCRIPTION	
0	U44-4	J7-23	Automatic Mark Hold (AMHO):	1 = LOS, 0 = SIGNAL
1	U44-17	J7-20	AGC Gain A (DGA)	

2	U44-2	J7-21	AGC Gain B (DGB)
3	U44-6	J7-22	AGC Gain C (DGC)
4	U44-11	U64-2	Front Panel controller Interrupt (KBINT): 0 = intr req
5	U44-15	J2SW	Transmit Data RS232/MIL188: 1 = MIL188, 0 = RS232
6	U44-8	J5SW	Remote Port RS232/MIL188: 1 = MIL188, 0 = RS232
7	U44-13	U59-3	Modem Receive Data (RXDTR): 1 = MARK, 0 = SPACE

4.3.6.3 MARK/SPACE BANDPASS FILTER Q

The Q's of the MARK and SPACE input filters on the modem board are selected with latch control bits on the Control Board. Since each filter requires 4 bits, a single 8 bit lat is used as shown in Schematic A1808.

TABLE 4.15
MARK/SPACE Q LATCH

PORT	REF	DESCRIPTION	I/O
38H	U47-11	MARK and SPACE filter Q latch	OUTPUT

TABLE 4.16
MARK/SPACE Q - BIT ASSIGNMENT
Output: OUT0.L

REF	DESCRIPTION	CONN
U47-2	MARK Filter Q High/Low	to J7-15
U47-5	MARK Filter Q bit 3	to J7-14
U47-6	MARK Filter Q bit 2	to J7-13
U47-9	MARK Filter Q bit 1	to J7-12
U47-12	SPACE Filter Q High/Low	to J7-19
U47-15	SPACE Filter Q bit 3	to J7-18
U47-16	SPACE Filter Q bit 2	to J7-17
U47-19	SPACE Filter Q bit 1	to J7-16

The Q values selected with these control bits are listed in Table 4.2.

4.3.6.4 CONTROL REGISTER 1

Several miscellaneous control signals are latched in an octal D-type latch (U48) shown Schematic A1808. This latch contains a reset input, RESET.L (U48-1), that will force all the control signals to a low state when the power is first turned ON. This reset ensures th the NMI control signal, NMIENA (U48-2), signal is low during power on initialization.

TABLE 4.17
CONTROL REGISTER 1

PORT	REF	DESCRIPTION	I/O
39H	U48-11	NMI, Regen, RX/TX control latch	OUTPUT

The function of each control signal is summarized below in Table 4.18.

TABLE 4.18
CONTROL REGISTER 1 - BIT ASSIGNMENT
Output: OUT1.L, BIT x

BIT	REF	DESCRIPTION	TO
7	U48-2	NMI Enable bit (NMIENA)	U1-16
6	U48-5	REGEN Enable (REGEN)	U63-5, U64-5
5	U48-6	Resync RXD (RSYNC)	U64-11, U56-1, U65-2
4	U48-9	RXD Normal/Reverse (RXDNR)	U57-1
3	U48-12	TXD Normal/Reverse (TXDNR)	U57-4
2	U48-15	TXD Enable (TXENABLE)	U56-10
1	U48-16	[not assigned]	
0	U48-19	Diversity Enable (DIVC)	J7-25

Output: OUT1.L, BIT 7:
The NMI Enable bit (NMIENA) activates the NMI real time clock in Schematic A1807 for t microprocessor. A high signal enables NMI (NMIENA = 1). When a reset occurs, this bit forced low to disable NMI (NMIENA = 0).

Output: OUT1.L, BIT 6:
The Regeneration Enable bit (REGEN) determines whether the data terminal RXD output in Figu A1816 is connected to the demodulated RX data from the modem or to the control boa regeneration serial controller. When regeneration mode is disabled (REGEN = 0), the mod receive data signal, RXDTR (U57-2), is connected to the modem terminal receive data outpu RXDFR (U63-11). When regeneration is enabled (REGEN = 1) the modem receive dat RXDTR, is connected to the regeneration serial controller receive data input, RXDB (U66-2 and the regenerated data from the transmit data output, TXDB (U66-25) is connected to t modem terminal data connector receive data output, RXDFR. For regeneration to work properl the correct data rate and word length must be programmed into the serial controller chann B.

Output: OUT1.L, BIT 5:
The ST-8000A has the ability to resynchronize the receive data, RXDTR, signal to a recover receive data clock. D-latch U55 in Schematic A1816 samples the RXDTR signal from the mod

and re-clocks this data with a stable internal data rate clock. The result of th resynchronizing operation is to reduce the jitter in the data terminal receive data outpu RXDFR (U63-11). When enabled (RSYNC = 1) the receive data is resynchronized. When disabl (RSYNC = 0) receive data is passed to the data terminal without re-clocking.

Output: OUT1.L, BIT 4:
The ST-8000A provides independent control over transmit and receive data polarity, shown in Figure A1816. When set for NORMAL receive data (RXDNR = 0), RXDTR from the mod is passed through to RXDB (U57-3) without change. When enabled (RXDNR = 1) the RXDTR sign from the modem is inverted before it reaches RXDB (U57-3).

Output: OUT1.L, BIT 3:
The ST-8000A provides independent control over transmit and receive data polarity, shown in Schematic A1816. When set for NORMAL transmit data (TXDNR = 0), TXDIN from the mod is passed through to TXD (U57-6) without change. When enabled (TXDNR = 1) the TXDIN sign from the modem is inverted before it reaches TXD.

Output: OUT1.L, BIT 2:
The ST-8000A Built In Tests (BIT) require that the external TXD input be disabled duri testing. When disabled (TXENABLE = 0) the data terminal TXDIN input is blocked at U56- When enabled (TXENABLE = 1) the data terminal TXDIN input is connected to the TXD (U57- output.

Output: OUT1.L, BIT 0:
If the diversity option is installed in the ST-8000A, diversity mode is enabled when th signal is high (DIVC = 1) and disabled otherwise.

4.3.6.5 CONTROL REGISTER 2

Several miscellaneous control signals are latched in an octal D-type latch (U51) shown Schematic A1808. All of these control signals are passed to the modem board.

TABLE 4.19
CONTROL REGISTER 2

PORT	REF	DESCRIPTION	I/O
3AH	U51-11	AMHC, Det. Mode, Channel, Mute, BIT	OUTPUT

The function of each control signal is summarized in Table 4.20.

TABLE 4.20
CONTROL REGISTER 2 - BIT ASSIGNMENT
Output: OUT2.L, BIT x

BIT	REF	DESCRIPTION	TO
7	U51-2	Automatic Mark Hold Enable (AMHC)	J7-24
6	U51-5	High Speed Enable (HSLS)	J7-26
5	U51-6	Detector Mode (DMA)	J7-27
4	U51-9	Detector Mode (DMB)	J7-28
3	U51-12	Channel Select (CHSEL)	J7-32
2	U51-15	Transmit Mute (MUTE)	J7-33
1	U51-16	Loopback Enable (BCB)	J7-36
0	U51-19	Loopback Enable (BCA)	J7-34

Output: OUT2.L, BIT 7:
The Automatic Mark Hold Enable signal (AMHC) enables and disables the AMH circuit on t
modem board. The automatic mark hold feature is enabled when AMHC = 1 and is disabled wh
AMHC = 0.

Output: OUT2.L, BIT 6:
The High Speed Enable selects the low or high speed demodulator on the modem card. The hi
speed demodulator is enabled when HSLS = 1 and is disabled when HSLS = 0.

Output: OUT2.L, BIT 5, 4:
The detector mode is selected with bits 5 and 4. The detector options are listed in Tab
4.21.

TABLE 4.21
DETECTOR MODES

DMB	DMA	Detector Mode
0	0	MARK/SPACE
0	1	MARK ONLY
1	0	SPACE ONLY
1	1	MARK/SPACE = ATC.

Output: OUT2.L, BIT 3:
The modem board has two channels: the modulator and the demodulator. The Channel Sele
control signal determines whether the transmit or receive tones are displayed on the fro
panel bar graph displays. The demodulator is selected when CHSEL = 1, and the modulat
channel is selected when CHSEL = 0.

Output: OUT2.L, BIT 2:
The Transmit Mute signal enables and disables the output AFSK tones. When MUTE = 0, t
transmit tones are enabled and the radio keyline relay is activated or closed. When MU
= 1, the transmit tones are disabled, and the PTT relay is not activated.

Output: OUT2.L, BIT 1, 0:
The Loopback enable control bits enable and disable an analog loopback that connects the AF
output signal to the audio input. Three different loopback gain options are available:

TABLE 4.22
LOOPBACK CONTROL

BC	BA	Loopback Mode
0	0	Disabled
0	1	0 dBm
1	0	-20 dBm
1	1	-40 dBm

4.3.7 MARK/SPACE Transmit Tone Generator

The AFSK tone oscillator illustrated in Schematic A1811 is a 16 bit full adder operating a digital signal synthesizer with a square wave output set to 50 times the audio to frequency. Two sets of latches store the constants for the MARK and SPACE tones, and t transmit data signal, TXD (U55-12), selects either the MARK tone (TXD = 0) or SPACE tone (T = 1).

The D-type latch is included to synchronize the changes between MARK and SPACE to that porti of the synthesized sine wave output where the slope is 0. In this fashion, the distorti is minimized. The synchronizing signal, FSKCLK (U55-11) pulses once per sine wave cycle.

The MARK/SPACE tone digital synthesizer is a 16 bit full adder implemented with four 4 b full adders (U24 - U27). On each rising edge of CKREF (U17-11, U16-11), a 819,000 Hz cloc the current 16 bit sum is latched into two D-type latches (U16, U17). These latch outputs a then added to the tone constant stored in either the MARK or SPACE tone latch depending the state of the sampled TXD signal (U55-9, U55-8). When a MARK is transmitted, t MARK constant registers (U41, U43) are enabled on the adder inputs. When a SPACE transmitted, the SPACE constant registers (U40, U42) are enabled on the adder inputs. T selected constant is summed with the previous sum latched in two octal latches (U16, U17) form a new sum that will be latched on the next rising edge of CKREF to complete the cycl The output of this synthesizer, TFSK (U17-19) has a nominal frequency of 50 times the select tone frequency.

Figure 4.13 summarizes the digital frequency synthesizer operation. The digit synthesizers generate their output frequency through addition. The frequency is determin by the magnitude of the constant loaded into the input latches and the clock referen frequency driving the synthesizer. For example, if a constant 001 hex is loaded into t MARK latch, and TXD = 0, then the sum at the output of the latches U16 and U17 will incremented by 1 count for each rising edge of CKREF. After 32,768 rising edges, the TF output will change from 0 to 1. Then, after another 32,768 rising edges, the TFSK signal wi change from 1 to 0. The total time for one cycle is 65,536 clock cycles of CKREF. If CKR is set to 819,200 Hz, the TFSK output will have a frequency of 12.5 Hz. If the MARK lat is changed to a constant of 002 hex, then TFSK will equal 25 Hz. The largest constant th can be loaded into the MARK register is 32,767, and the resulting output signal approximately 409,587 Hz. Thus, this synthesizer may be set to any frequency between 12.5 and 409,600 Hz in steps of 12.5 Hz.

At low frequencies or when the constant is an exact divisor of 819,200, the output wavefo on TFSK (U17-19) is a 50% duty cycle square wave. However, if the constant is not integer divisor, the relationship between the constant and CKREF generates signal jitte While this jitter is visible on an oscilloscope, the resulting sine wave output is smooth by the sine wave approximation process and the 50 times over sampling.

In the ST-8000A the tone synthesizer generates output frequencies on TFSK of 15,000 Hz a 150,000 Hz in steps of 25 Hz. The resulting output from the AFSK generator on the modem ca is 300 to 3000 Hz in 0.5 Hz increments. For each tone frequency, the constant loaded ir the MARK and SPACE register is calculated using the following formulae (7) and (8):

MARK AFSK TONE CONSTANT = MARK TONE FREQUENCY x 4 (7)

SPACE AFSK TONE CONSTANT = SPACE TONE FREQUENCY x 4 (8)

For example, to transmit a MARK tone of 2125 Hz and a SPACE tone of 2295 Hz, the MA constant is 8,500 and the SPACE constant is 9,180. The lowest tone constant is 1,200 for 3 Hz, and the highest is 12,000 for 3000 Hz.

4.3.8 MARK Filter Synthesizer

The MARK filter synthesizer is illustrated in Schematic A1812. This synthesizer generat the filter clock, MCLK (U19-19), used to set the center frequency of the MARK bandpa filter on the Modem Board (J7-1). The operation of this synthesizer is identical the transmit tone synthesizer described in the previous section, and the output of th synthesizer is 50 times the selected MARK frequency.

The MARK filter constant is loaded into two octal D-type latches (U45, U46). The outp frequency of the MARK filter synthesizer is calculated using formula (9).

MARK FILTER CONSTANT = MARK TONE FREQUENCY x 4 (9)

4.3.9 SPACE Filter Synthesizer

The SPACE filter synthesizer is illustrated in Schematic A1813. This synthesizer generat the filter clock, SCLK (U21-19), used to set the center frequency of the SPACE bandpa filter on the Modem Board (J7-3). The operation of this synthesizer is identical to t transmit tone synthesizer described in the previous section, and the output of th synthesizer is 50 times the selected SPACE frequency.

The SPACE filter constant is loaded into two octal D-type latches (U49, U50). The outp frequency of the SPACE filter synthesizer is calculated using formula (10).

SPACE FILTER CONSTANT = SPACE TONE FREQUENCY x 4 (10)

4.3.10 HIGH SPEED Local Oscillator

The HIGH SPEED Local Oscillator synthesizer is illustrated in Schematic A1814. Th synthesizer generates the clock, HSCLK (U23-19), used to set the IF center frequer of the HIGH SPEED detector on the modem board (J7-7). The operation of this synthesizer identical to the transmit tone synthesizer described in the previous section, except th

the output of this synthesizer is set to the center frequency of the HIGH SPEED data signal pl
10,000 Hz.

The HIGH SPEED oscillator constant is loaded into two octal D-type latches (U52, U53). T
output frequency of the HIGH SPEED filter synthesizer is calculated using formula (11).

$$\text{HIGH SPEED CONSTANT} = \frac{1}{12.5}\left\{\left(\frac{\text{MARK + SPACE}}{2}\right) + 10{,}000\right\} \qquad (11)$$

4.3.11 LOW PASS Filter Clock

The LOW PASS filter clock controls the corner frequency of the low pass filter in t
detector of the modem board. The programmable timer (U1) in Schematic A1807 generates th
clock signal, LPCLK (U1-13), and it is passed to the filter on the modem board (J7-5). Th
oscillator is simply a 16 bit counter with a clock reference frequency of 4.9152 MHz. T
16 bit constant is loaded into the programmable timer.

For a given data rate, the LOW PASS filter constant is calculated using formula (12).

$$\text{LOW PASS CONSTANT} = (\ 4{,}915{,}200\ ) / (\ 72 \times \text{DATA RATE}\ ) \qquad (12)$$

This constant varies between 6,827 for 30 bits per second to 57 for 1200 bps.

4.3.12 Regeneration

Schematic A1815 illustrates the serial channel controller (U66) used for receive data (RXDT
regeneration and the remote control port. This controller has an internal baud ra
clock that sets the data rate for both channels.

When regeneration is active (REGEN = 1) asynchronous characters received on the RXDB (U66-2
input of the serial controller are passed to the TXDB (U66-25) output. Regenerati
receives and re-transmits each receive character removing any received jitter and nois
Note that regeneration is only possible when receiving asynchronous start-stop characte
with character lengths of 5 to 8 data bits.

The serial controller operates in an interrupt driven mode during regeneratic
Any character received on the RSCB (U66-27) input causes INT.L (U66-5) to go low signali
a data available interrupt. The microprocessor controller reads the serial controller
clear this interrupt flag.
In addition, note that regeneration can only work properly when the data presented to t
RXDB (U66-27) input has polarity set such that a MARK equals TTL high and SPACE equa
TTL low. This should be the case when the MARK tone is set for the correct tone and t
receive data normal/reverse, RXDNR (U57-1), are set correctly for the desired signal. T
regenerated signal on RXDFR (U63-11) will have MARK high and SPACE low independent of t
RXDNR setting.

Whether regeneration is enabled or not, a data rate clock equal to 16 times the recei
channel baud rate is generated on the TXCLK (U66-26) output of the serial controlle
This clock provides a time reference signal for the clock recovery circuit describ
in the next section. The frequency of this clock is set by the BAUD RATE setting on the fro
panel; it is set to 16 times that rate.

4.3.13 Remote Control Port

The dual channel serial controller (U66) channel A is connected to the Remote Control port the ST-8000A. In Schematic A1815, note that the polarity of the data on this port may set to RS232 or MIL188 levels with the jumper J5. When in the RS232 position, J5SW lo the port has normal RS-232 MARK and SPACE signal levels.

The remote port REMRXD is converted to TTL level (U59-6) and passed to the RXDA input the serial controller (U66-13) after passing through the RS232/MIL188 polarity gate. T ST-8000A may read the Remote Port Clear to Send signal, REMCTS (U59-8), to control output fl control.

The remote port REMTXD signal comes from the TXDB (U66-15) output of the seri controller and the RS232/MIL188 polarity gate. The REMTXD signal is combined with the RT (U66-17) serial controller output so that this signal is held in the MARK hold state when RT is low. Note that the RTSA output drives the REMRTS (U62-8) signal on the remote contr port. In addition, a REMDTR (U62-11) and REMCTS (U62-6) signals are provided.

The remote port is configured as a multi-drop output where up to 8 ST-8000A remote po transmit data outputs, REMTXD, may be connected in parallel (or "wire-ORed"). Diodes and D3 in Figure A1815 actively pull REMTXD to MARK and SPACE levels when RTSA (U66-17) is l or enabled, and allow the REMTXD to float when RTSA is high. Thus, the output data line connected only when this unit has a response to transmit. The zener diodes D1 and D4 lim the REMTXD output voltage swing to MIL188 levels. To improve noise immunity on t common transmit data output line, REMTXD, one and only one ST-8000A in an installation of o to 8 units should have jumper J3 set to connect -8 VDC and the resistor to the output lin This resistor defaults the line to a MARK or negative voltage level when no unit is active sending.

4.3.14 Synchronous Data Clocks

Schematic A1816 illustrates the receive data clock, RXCLK (U60-11), recovery circuit f
serial data received by the Modem Board. Basically, this circuit synchronizes an interr
clock to the edges in the serial receive data, RXDTR (U57-2), from the modem card. Clo
Recovery circuits are also shown in simplified from in Figure 4.14.

Changes in the receive data signal generate pulses (U57-11) that reset a 4 bit counter (U5
each time a change occurs. This counter is driven by a clock running at 16 times the ba
rate, TXCLKB (U58-1), and the output of the most significant bit of the counter (U58-6) wi
change after 8 TXCLKB cycles. If this clock is properly set, the clock transition occurs
the center of the data bit and a correct receive data recovered clock, RXCLK (U60-11
is generated. Jumper J4 selects either normal or inverted clock for RS232 or MIL188 recei
data.

A D-type latch is driven by the recovered clock (U55-3) to re-clock the receive da
(U55-5). In some cases, re-clocking the data will reduce receive data jitter and impro
system performance. Note that the receive data re-clocking latch will work with eith
synchronous or asynchronous receive data since it does not depend on a start or stop bi
nor does data polarity matter.

The baud rate clock TXCLKB (U58-1) is simply divided by 16 in a four bit counter (U5
to generate the TXCLK (U60-3) synchronous transmit clock. Since the transmit data input, TXD
(U59-1), directly drives the tone generator, there is no need to change this clock phase f
RS232 and MIL188 data. The ST-8000A transmits correctly in either case.

4.4 FRONT PANEL (ASSEMBLY A3)

The Front Panel (A3) in constructed on two circuit boards, one for front panel numeric displays and LED indicators, and one for display driver circuitry. Assembly A3 also includ the 27-key keypad and the physical front panel of the cabinet. The physical relationship the major front panel components is shown in Figure 4.15.

Front Panel circuitry will be discussed in the order in which it appears in schematic diagra A1818 through A1824. Refer to these diagrams and the Block Digram in Figure 4.16 for t following discussions.

4.4.1 Bar Graph Indicators

Refer to Figure 4.16 and Schematic Diagram A1818. Two identical bar graph circuits are use one for Mark data, and one for Space data. The Mark circuitry will be described with Spa circuit references parenthesized.

DC-level tuning bar signals originate on the Modem Board (A1) as described in Section 4.2. These 0 to +5 VDC analog signals are passed via Cable A5W6 from A1J9-1 to A3J2-1 (Mark) a A1J9-2 to A3J2-2 (Space) (See Figures 4.4 and 4.5).

The Mark (Space) bar display is made up of two ten-segment LED bar-graph indicators and the driver IC's (DS34, DS35, U10, U11 for Mark and DS37, DS36, U14, and U13 for Space). Each b shows a 3 dB increment in Mark or Space data signal amplitude. Driver U10 (U14) and displ DS34 (DS37) show the upper 30 dB range of signal strength from -24 to +6 dBm. Amplifier U (U9a) has a gain of 30 dB and drives the low-level indicator circuits, U11 and DS35 (U13 a DS36). This bar shows signal strengths between -54 dBm and -30 dBm. Display drivers U10 a U11 (U14 and U10) are connected in "progressive mode"; the input LED bar and all lower lev bars are illuminated. The bars are arranged on the front panel with the lowest level indicati to the left. Thus, signal strength is indicated from left to right as the amplitude increase As noted in Section 4.2.2, low-level calibration of the bar graphs is set by adjustment controls A1R15 (Mark) and A1R24 (Space) (See schematic diagram A1801). There are no bar gra adjustments on the Front Panel (A3).

4.4.2 Modulator Output Level

Please refer to Schematic Diagram A1818. The Output Level adjustment (R27) is located on t Front Panel (A3). This control sets the output level of the modulator as discussed in secti 4.2.3. Output level increases with a clockwise rotation of the screw-driver adjustment. Wh "CH2" is selected for front panel display and control, the Mark and Space bar indicato indicate the modulator output level in dBm (3 dB increments).

Figure 4.15 FRONT PANEL ASSEMBLY

4.4.3 Front Panel Controller

The ST-8000A uses an integrated keyboard decoder and display controller (U8) shown Schematic A1819 to handle the front panel keypad input and seven segment display outputs This device debounces keypad entries to prevent the inadvertent entry of multip keys, and buffers the display data for the multiplexed front panel numerical displays a indicators.

The keypad/display interface controller (U8) is an 8 bit microprocessor peripheral devi that connects directly to the control board data bus (DB0 to DB7), the read (RD.L) and wri (WR.L) signals, address bit 0 (A0), the front panel enable (FP.L), and system reset (RESET The microprocessor reads and writes the control and data registers in this device to inp keypad entries and load the display buffer output registers. An internal counter divides t system clock (PCLK) input to set the keypad and display scanning rate.

The keypad and the front panel display are scanned through the binary encoded scan li outputs (SL0 to SL3) in Figure A1819 and 3-to-8 line decoders in Schematics A1820 and A182 Keypad entries are detected as a TTL low on one of the row inputs (RL0 to RL3).

The seven segment display segment drivers are connected to the segment outputs (U8-24 to U8-31 Data on this output bus is inverted; to turn a segment ON, the corresponding output is he at a TTL low level when the digit is scanned. Because the segment outputs do not ha sufficient drive capability, discrete PNP switching transistors (Q17 to Q24) in Figure A18 buffer these outputs for all of the display segments. The display segments anodes of t common cathode seven segment display digits are all driven in parallel, as shown in Schemat A1822, and one scanned digit is selected with the digit driver circuit in Schematic A1821

4.4.4 Keypad

The front panel keypad is a matrix of single pole momentary switches arranged in three ro of 9 switches. The low three bits of the scan line outputs (SL0 to SL2) drive a 3-to-8 li decoder (U7) to select one of 8 keypad columns by forcing that column select line low. any of the keypad switches in that column are closed, one of the row lines (RL0 to RL3) wi be forced low to signal the keypad/display controller (U8) that a key has been pressed.

Note that the keypad is arranged as 4 rows of 8 keys and 1 row of 3 keys. Th keypad/display controller (U8) has a maximum scanning capacity of 8 rows by 8 columns, it cannot scan the 9 columns in a simple matrix fashion. However, by connecting three of t column drivers to the last column, and connecting that column to a fourth row line (RL3), t entire matrix of switches may be scanned.

When a keypress is detected, the keypad/display controller (U8) stores the row and colu locations into a key buffer and interrupts the microprocessor by forcing the front par interrupt line (KBINT) high.

ST-8000A firmware determines the function of all front panel keypad keys; there are hardwired switch functions.

4.4.5 Numerical Displays

The front panel assembly has 15 common cathode seven segment display digits and t additional LEDs driven in a multiplexed fashion by the keypad/display controller (U8). T scan line outputs (SL0 to SL3) select one of 16 digit drivers using two 3-to-8 line decode shown in Schematic A1821. For each of the 16 scan line selections, a single common catho

digit driver transistor is enabled through an inverting buffer. As each digit is select in turn, the segments are turned ON that correspond to the data presented on t keypad/display controller data output lines in Schematic A1819.

The keypad/display controller (U8) is configured to scan the entire front panel displ every 20 ms or 50 times per second to avoid visual flicker. In addition, the keypad/displ controller blanks the display as the scan lines change so that display digit contrast improved.

Schematic A1822 illustrates the assignment of the digits to the front panel location Five digits are assigned to the MARK and SPACE frequency windows, four digits to the BA window, and a single digit to the CHANNEL display. The two LED's mirror the chann selection, but they are scanned as an independent digit during scan time slot 15.

The digit assignments for the front panel are summarized in Table 4.23.

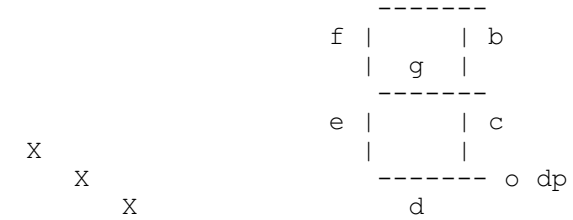
TABLE 4.23
FRONT PANEL DISPLAY SCAN

DISPLAY	DIGIT SCAN NUMBER
MARK	4 3 2 1 0
SPACE	9 8 7 6 5
BAUD	13 12 11 10
CHANNEL	14
LED	15

Each seven segment display digit has segments assigned as shown in Table 4.24.

TABLE 4.24
SEVEN-SEGMENT DISPLAY

	BIT							
SEGMENT	7	6	5	4	3	2	1	0
SEG dp	X							
SEG g		X						
SEG f			X					
SEG e				X				
SEG d					X			
SEG c						X		
SEG b							X	
SEG a								X



4.4.6 LED Indicators

In addition to the multiplexed front panel display digits, there are 16 latched fro panel LED indicators illustrated in Schematic A1823. The two octal latches (U1, U2) a connected to the control board data bus (DB0 to DB7). The signals to load the LED latch come directly from an I/O output address decoder on the control board (LED0.L, LED1.L The LED latch data is inverted; a TTL 0 turns the corresponding LED ON.

The LED data bus bit assignments for the front panel are shown in Table 4.25.

TABLE 4.25
LED DATA BUS

	BIT							
LED0_L (U1)	7	6	5	4	3	2	1	0
MARK	X							
CENTER		X						
SPACE			X					
SHIFT				X				
SYNC					X			
FSK						X		
MARK ONLY							X	
SPACE ONLY								X

	BIT							
LED1_L (U2)	7	6	5	4	3	2	1	0
REGEN	X							
AMH		X						
HOLD			X					
REV				X				
ENTER					X			
DIV						X		
MUTE							X	
REMOTE								X

4.5 POWER SUPPLY, ASSEMBLY A4

The Power Supply, Assembly A4, provides DC power for all assemblies of the ST8000A. Plea refer to Figure 4.17 and Schematic Diagram A1825. Portions of the power supply are actual a part of the Cabinet, Assembly A5. Please also refer to Figures 4.4, 4.5 and 4.18.

The Power Supply provides three regulated DC voltages to ST8000A circuits: (1) +5 VDC @ 2 Amperes, (2) +8 VDC @ 0.2 Amperes, and (3) -8 VDC @ 0.2 Amperes. These are the only DC pow supply voltages used in the ST8000A.

4.5.1 +5 VDC Power Supply

The power transformer (A5T1) supplies 17.50 VAC CT to connector J1 (pins 1, 2, and 3 Full-wave rectifier D1 and D2 and filter capacitor C1 provide an unregulated +10.0 volts DC the three-terminal regulator input. Capacitor C2 and C3 provide decoupling to assure stab operation of the regulator. The +5VDC regulator itself (A5VR1) is mounted on the rear par of the cabinet with a finned heat-sink to minimize heat within the ST8000A cabinet. Capacito A5C1 and A5C2 provide additional decoupling for proper operation of the regulator. T regulator connects to J5 of the power supply through cable A5W11. A type LM123/STEEL integrat circuit is the +5V regulator device.

4.5.2 +8 and -8 VDC Power Supplies

The power transformer (A5T1) supplies 20.5 VAC CT via connector J1 (pins 3, 4, and 5). Dioc D3, D4, D5, and D6 and capacitors C8 and C9 make-up a full-wave bridge recifier syste providing $\pm$ 12.0 VDC to the positive (VR1) and negative (VR2) 3-terminal regulator integrat circuits. Capacitors C4, C5, C6, and C7 provide decoupling to assure stable operation of the regulators. The +8V and -8V regulators are each mounted to heat sinks on the circuit board

4.6 CABINET (ASSEMBLY A5)

The Cabinet (Assembly A5) houses all assemblies of the ST8000A, includes inter-assembly cable
provides rear-panel I/O connections, and includes additional power supply circuitry. Plea
refer to Figures 4.4, 4.5, and 4.18.

4.6.1 AC Power Connections

Figures 4.4 and 4.18 show the AC power input connector (J3), power transformer (T1), a
associated AC power input wiring.

AC power input may be 115 VAC or 230 VAC at a frequency from 47 to 440 Hz. Approximately
Watts of power are required to operate the ST8000A. AC power is connected to terminals "
(Ground), "D" (Neutral), and "K" (Line or "hot") of J3. All other J3 pins are unused.

The Safety Ground (pin "A") is connected via a Green wire to the ground terminal of the AC inp
line filter (FL1) and to the rear panel GROUND screw terminal. The power line "Neutral" (p
"D") is connected via a White wire to the Neutral terminal of the AC line filter. The pow
line "Line" (or "Hot") (pin "K") is connected to the Fuse holder (F1) via a Black wire. T
fuse is a type 3AG "Slow-Blow" with a 1.0 Ampere rating. A 1.0 Ampere fuse is used for bo
115 VAC and 230 VAC operation.

The AC power line filter (FL1) is UL, CSA, and VDE approved. The filter provides attentuati
of RFI from 40 dB at 0.15 MHz to 65 dB above 1.0 MHz (differential and common mode). Th
filter prevents conduction of internal radio frequency interference (RFI) from the ST8000A a
ST8000A susceptability to conducted external RFI.

The "Neutral" output of the AC filter connects to the power transformer T1 via the Whi
transformer pimary input lead. The "Line" (or "Hot") output of the AC filter connects to t
front panel AC Power Switch (A5S2) via Cable A5W15. The AC power switch connects to the re
panel 115/230 VAC selector switch (A5S1) also via cable A5W15.

The rear panel 115/230 VAC switch (A5S1) is used to select the 115 V or 230 V primary inp
connections to the power transformer, T1. This switch is mechanically protected on the re
panel to prevent accidental incorrect adjustment. It is not necessary to open the ST800
cabinet or make internal wiring modifications to change between 115 VAC and 230 VAC AC pow
input.

All AC power input wires, cables, and terminals are insulated and protected with sleeving
prevent accidental shocks when the ST8000A top or bottom covers are removed (such as f
servicing or when setting internal option switches.

4.6.2 Power Transformer

The AC power transformer, T1, includes a single tapped primary with connections for 115 VAC 230 VAC power line voltage input. These transformer leads connect to the AC input volta selector switch (A5S1) via cable A5W13. Transformer T1 includes a built-in thermal circu breaker that conforms to UL and VDE requirements. The breaker will trip if an overload caus over-heating of the transformer, preventing the possiblity of smoke or fire. Once tripped, t internal breaker will automatically reset when the overload is removed and after the transform has cooled.

The secondary of the power transformer T1 is a five-wire, center-tapped winding, providing 17 VCT for the +5V regulator and 20.5 VCT for the +8V and -8V regulators. T1 secondary connected to A4J1 via cable A5W14.

4.6.3 +5V Regulator

As discussed in section 4.5.1, the +5VDC regulator integrated circuit is mounted on the re panel of the cabinet. It connects to A4J5 via cable A5W11.

4.6.4 Interior Cable Assemblies

Please refer to Figures 4.4 and 4.5. A total of 15 cable assemblies are used to interconne ST8000A assemblies and rear panel connectors. These cable assemblies are clearly labeled a non-interchangeable. The following Tables detail each cable wire and connection points.

TABLE 4.26
CABLE A5W1
AUDIO I/O (A1J6 to A5J2)

MODEM A1J6	AUDIO I/O (Rear Panel) A5J2	SIGNAL	LEVEL
1	1	Modulator FSK Audio Output	0 dBm Maximum
2	3	Modulator FSK Audio Output	0 dBm Maximum
3	5	Keyline Relay Output	Relay Contact
4	6	Keyline Relay Output	Relay Contact
5	10	Demodulator FSK Audio Input	+6 dBm Maximum
6	12	Demodulator FSK Audio Input	+6 dBm Maximum
7	37	Shield (Ground)	Ground

NOTES: 1. All un-designated pins on A5J2 are not used.
2. Relay contract ratings are 50 VDC @ 50 ma maximum.

TABLE 4.27
CABLE A5W2
DIVERSITY (A1J7 to A5J5)

MODEM A1J7	DIVERSITY (Rear Panel) A5J5	SIGNAL	LEVEL
1	1	Diversity Mark Data	+5 VDC Maximum
2	2	Diversity Space Data	+5 VDC Maximum
3	3	Diversity Peak Detector Data	+5 VDC Maximum
4	4	Diversity AMH data	+5 VDC Maximum
5	5	Ground	Ground

NOTE: This cable only supplied when Option -01 is installed.

TABLE 4.28
CABLE A5W3
DATA I/O (A1J3 and A1J4 to A5J1)

MODEM A1J3	DATA I/O (Rear Panel) A5J1	SIGNAL	LEVEL
1	7	Demod Undetected Mark Audio Output	+5 dBm Maximum
2	9	Demod Undetected Space Audio Output	+5 dBm Maximum
3	10	Carrier Detect Output	RS232/MIL188
4	12	Demodulator Analog Ground	Ground
5	13	Ground	Ground
6	14	Ground	Ground
7	15	Keyline Relay Output	Relay Contacts
8	16	Keyline Relay Output	Relay Contacts
9	19	Transmit Clock Output	RS232
10	20	Transmit Data Input	RS2323/MIL188
A1J4			
1	21	Demod Mid-Bit Clock Output	RS232
2	22	Demodulator RS232 RXD Output	RS232
3	23	Demodulator MIL188 RXD Output	MIL188
4	24	Modulator Analog Ground	Ground
5	25	Ground	Ground
6	26	Ground	Ground
7	36	Modulator Analog Ground	Ground
8	37	Shield (Ground)	Ground
9	--	Data Port RTS Input	RS232
10	--	Data Port CTS Output	RS232

NOTES: 1. All un-designated pins on A5J1 are not used.
2. Data Port RTS and CTS control signals are provided to allow flow-control of the data terminal transmit device. These may be connected to spare pins of A5J1 at the user's discretion.
3. Relay contact ratings are 50 VDC @ 50 ma maximum.

TABLE 4.29
CABLE A5W4
REMOTE CONTROL (A1J5 to A5J4)

MODEM A1J5	REMOTE CONTROL (Rear Panel) A5J4	SIGNAL	LEVEL
1	1	Remote Data Input (REMRXD)	RS232/MIL188
2	2	Remote Status Input (REMCTS)	RS232/MIL188
3	3	Remote Data Output (REMTXD)	RS232/MIL188
4	4	Remote Status Output (REMRTS)	RS232/MIL188
5	5	Remote Status Output (REMDTR-"CTS")	RS232/MIL188

TABLE 4.30
CABLE A5W5
MODEM to CONTROL (A1J1 to A2J1)

MODEM A1J1	CONTROL A2J1	SIGNAL	LEVEL
1	1	Mark Filter Clock (MCLK)	TTL
2	2	Ground	Ground
3	3	Space Filter Clock (SCLK)	TTL
4	4	Ground	Ground
5	5	Low-Pass Filter Clock (LPCLK)	TTL
6	6	Ground	Ground
7	7	High Speed Clock (HSCLK)	TTL
8	8	Ground	Ground
9	9	Transmit FSK Sigbal (TFSK)	TTL
10	10	FSK Synchronizing Clock	TTL
11	11	Ground	Ground
12	12	Mark Q Set #1 (MQ1)	TTL
13	13	Mark Q Set #2 (MQ2)	TTL
14	14	Mark Q Set #3 (MQ3)	TTL
15	15	Mark Low Q Set (MQL)	TTL
16	16	Space Q Set #1 (SQ1)	TTL
17	17	Space Q Set #2 (SQ2)	TTL
18	18	Space Q Set #3 (SQ3)	TTL
19	19	Space Low Q Set (SQL)	TTL
20	20	Demodulator Gain A (DGA)	TTL
21	21	Demodulator Gain B (DGB)	TTL
22	22	Demodulator Gain C (DGC)	TTL
23	23	AMH Output (AMHO)	TTL
24	24	AMH Control (AMHC)	TTL
25	25	High Speed Control (HSLS)	TTL
26	26	Detector Mode A (DMA)	TTL
27	27	Detector Mode B (DMB)	TTL
28	28	Receive Data To Regen (RXDTR)	TTL
29	29	Receive Data From Regen (RXDFR)	TTL
30	30	Transmit Data to Modem (TTLTXD)	TTL
31	31	Channel Select (CHSEL)	TTL
32	32	FSK Output Mute Control (MUTE)	TTL
33	33	BIT Control A (BCA)	TTL
34	34	BIT Control B (BCB)	TTL
35	35	Ground	Ground
36	36	Transmit Clock Output (TXCLK)	RS232/MIL188
37	37	Transmit Data Input (TXDIN)	RS232/MIL188
38	38	Receive Mid-Bit Clock (RXCLK)	RS232/MIL188
39	39	Ground	Ground
40	40	Remote Data Input (REMRXD)	RS232/MIL188
41	41	Remote Status Input (REMCTS)	RS232/MIL188
42	42	Remote Data Output (REMTXD)	RS232/MIL188
43	43	Remote Status Output (REMRTS)	RS232/MIL188
44	44	Remote Status Output (REMDTR)	RS232/MIL188
45	45	Diversity Control (DIVC)	TTL
46	46	Data Port RST Input (DRTS)	RS232/MIL188
47	47	Data Port CTS Output (DCTS)	RS232/MIL188

50	50	Ground	Ground

CABLE A5W6
MODEM to FRONT PANEL (A1J9 to A3J2)

MODEM A1J9	FRONT PANEL A3J2	SIGNAL	LEVEL
1	1	Mark Bar Graph Signal (BMK)	Analog, 0 - +5VDC
2	2	Space Bar Graph Signal (BSP)	Analog, 0 - +5VDC
3	3	Modulator to Level Control (MOA)	Audio, +2 dBm
4	4	Level Control to Modulator (MOB)	Audio, 0 to +2 dBm
5	5	Level Control Common (MOC)	Modulator Ground
6	6	Ground	Ground

Table 4.32
CABLE A5W7
CONTROL to FRONT PANEL (A2J2 to A3J1)

CONTROL A2J2	FRONT PANEL A3J1	SIGNAL	LEVEL
1	1	Data Bus #7 (D7)	TTL
2	2	Data Bus #6 (D6)	TTL
3	3	Data Bus #5 (D5)	TTL
4	4	Data Bus #4 (D4)	TTL
5	5	Data Bus #3 (D3)	TTL
6	6	Data Bus #2 (D2)	TTL
7	7	Data Bus #1 (D1)	TTL
8	8	Data Bus #0 (D0)	TTL
9	9	Read Data (Low) (RDL)	TTL
10	10	Write Data (Low) (WDL)	TTL
11	11	Address #0 (A0)	TTL
12	12	Front Panal (Low) (FPL)	TTL
13	13	LED Control #0 (LED0)	TTL
14	14	LED Control #1 (LED1)	TTL
15	15	Front Panel Clock (FPCLK)	TTL
16	16	Reset (RESET)	TTL
17	17	Keyboard Interupt (KBINT)	TTL
18	18	(not used)	----
19	19	Ground	Ground
20	20	Ground	Ground

Table 4.33
CABLE A5W8
MODEM to POWER SUPPLY (A1J8 to A4J2)

MODEM A1J8	POWER SUPPLY A4J2	SIGNAL	LEVEL
+5 VDC Power (Vcc)		+5 VDC	
2	2	+5 VDC Power (Vcc)	+5 VDC
3	3	+8 VDC Power (V+)	+8 VDC
4	4	-8 VDC Power (V-)	-8 VDC
5	5	Power Supply Ground	Ground
6	6	Power Supply Ground	Ground

Table 4.34
CABLE A5W9
CONTROL to POWER SUPPLY (A2J3 to A4J3)

CONTROL A2J3	POWER SUPPLY A4J3	SIGNAL	LEVEL
1	1	+5 VDC Power (Vcc)	+5 VDC
2	2	+5 VDC Power (Vcc)	+5 VDC
3	3	+8 VDC Power (V+)	+8 VDC
4	4	-8 VDC Power (V-)	-8 VDC
5	5	Power Supply Ground	Ground
6	6	Power Supply Ground	Ground

Table 4.35
CABLE A5W10
FRONT PANEL to POWER SUPPLY (A3J3 to A4J4)

F PANEL A3J3	POWER SUPPLY A4J4	SIGNAL	LEVEL
1	1	+5 VDC Power (Vcc)	+5 VDC
2	2	+5 VDC Power (Vcc)	+5 VDC
3	3	+8 VDC Power (V+)	+8 VDC
4	4	-8 VDC Power (V-)	-8 VDC
5	5	Power Supply Ground	Ground
6	6	Power Supply Ground	Ground

Table 4.36
CABLE A5W11
REGULATOR to POWER SUPPLY (A5VR1 to A4J5)

REGULATOR A5VR1	POWER SUPPLY A4J5	SIGNAL	LEVEL
1	1	+10 VDC Unregulated (VUNREG)	+10 VDC
2	2	Power Supply Ground	Ground
3	3	+5 VDC Regulated (Vcc)	+5 VDC

Table 4.37
CABLE A5W12
AC POWER to FUSE & FILTER (A5J3 to A5F1 & A5S1)

POWER A5J3	DEVICE	SIGNAL	LEVEL
A	A5FL1-G	AC Power Safety Ground (GND)	Chassis Ground
D	A5FL1-N1	AC Power Neutral (N)	115/230 VAC
K	A5F1-1	AC Power Line to Fuse (L)	115/230 VAC
A5F1-2	A5FL1-L1	AC Power Line from Fuse	115/230 VAC

Table 4.38
CABLE A5W13
TRANSFORMER PRIMARY (A5T1 to A5FL1 & A5S1)

TRANS A5T1	DEVICE	SIGNAL	LEVEL
WHITE	A5FL1-N2	AC Power Neutral to Transformer	115/230 VAC
BLK/WH	A5S2-1	115 VAC AC Primary Tap	115 VAC
BLACK	A5S2-3	230 VAC AC Primary Tap	230 VAC

Table 4.39
CABLE A5W14
TRANSFORMER SECONDARY (A5T1 to A4J1)

TRANS A5T1	POWER SUPPLY A4J1	SIGNAL	LEVEL
BLUE	1	8.75 VAC for +5 VDC Supply	8.75 VAC
BLUE	2	8.75 VAC for +5 VDC Supply	8.75 VAC
BROWN	3	Secondary Center Tap (CT)	Ground
ORANGE	4	10.25 VAC for ±8 VDC Supplies	10.25 VAC
ORANGE	5	10.25 VAC for ±8 VDC Supplies	10.25 VAC

Table 4.40
CABLE A5W15
AC POWER SWITCH (A5S2 to A5FL1 & A5S1)

A5S2	DEVICE	SIGNAL	LEVEL
1	A5S1-2	AC Power Switch Output	115/230 VAC
2	A5FL1-L2	115/230 VAC Line from Filter	115/230 VAC