HAL COMMUNICATIONS CORP.
ST-8000A

BUILT-IN-TEST (BIT) FEATURE
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1. PURPOSE:

The ST-8000A includes a "Built-In-Test" (BIT) feature that may be used at any time to rapidly test key circuits of the FSK Modem. The primary intended use of the BIT feature is for in-field confirmation of ST-8000A operability. Field operators may invoke BIT at any time. If all steps of the BIT pass, the operator may then proceed with operation with a high confidence that the ST-8000A is fully operational. If any Built-In-Test step fails, the ST-8000A should be replaced and returned to HAL Communications for repair. The BIT feature may also be used by HAL personnel to confirm operational status of new and repaired units.

2. BIT ACTIVATION:

The ST-8000A BIT feature is <u>not</u> automatically invoked. BIT use requires active operator entry of either a series of front panel keypad keys or transmission of unique commands from a Remote Control terminal connected to the ST-8000A rear panel Remote Control Port (connector J4). The BIT feature can not be accidentally invoked by any received data combination, data obtained via either the Audio I/O Port (connector J2) or Data I/O Port (connector J1). BIT is not automatically invoked upon ST-8000A AC power ON.

During the time that BIT sequences are running, the ST-8000A is <u>not</u> available for coding or decoding of Radio or Wire-Line data (data via connector J2). BIT activation causes the following changes inside the ST-8000A:

1. Demodulator audio input is disconnected from J2, pins 10 & 12 and connected to the modulator output, forming an internal audio loopback. The internal audio loopback connection includes three calibrated attenuator settings to test demodulator operation. The loopback test levels used are 0 dBm, -20 dBm, and -45 dBm.

2. The modulator data input signal is disconnected from Data I/O connector J1 (pin 20). This signal is used internally by BIT to confirm modulator and demodulator operation.

The ST-8000A operator may start the BIT sequence in two different ways: (1) via front panel keypad key entry; and (2) via Remote Control port command entry. These two entry techniques are detailed in the following sections. 2.1 BIT Entry via Front Panel Keypad:

To start BIT from the front panel, perform the following steps:

1. Turn ST-8000A AC Power ON.

2. Wait until normal MARK, SPACE, BAUD, and CHANNEL numbers are displayed on the front panel.

3. In sequence, press and release first the 2nd, then the BIT, and finally the ENTER keypads. A three-key sequence is required to prevent accidental BIT activation.

Built-In-Tests will now be run in the sequence described in Section 4. Once the BIT sequence has started, the operator has two additional options:

4. To RESTART BIT at Step #0, press BIT.

5. To cancel BIT and return the ST-8000A to normal operation, press CLEAR. BIT steps are immediately disabled and the ST-8000A is returned to the operational parameters in use prior to activating BIT.

2.2 BIT Entry via Remote Control Commands:

To start BIT using Remote Control commands, perform the following steps:

1. Turn ST-8000A AC Power ON.

2. Wait until normal MARK, SPACE, BAUD, and CHANNEL numbers are displayed on the front panel.

3. Select the unit using the "Cxx" ("xx" = Channel No.) and R1 commands.

4. Enter the Remote Control command T1.

Built-In-Tests will now be run in the sequence described in Section 4. Once the BIT sequence has started, the operator has two additional options:

5. To RESTART BIT at Step #0, re-enter the T1 Remote Control command.

6. To cancel BIT and return the ST-8000A to normal operation, enter the T0 (DISABLE) Remote Control command. BIT steps are immediately disabled and the ST-8000A is

returned to the operational parameters in use prior to activating BIT.

3. BIT TEST RESULT INDICATIONS:

During the time that the Built-In-Test feature is running, the front panel "CH" (Channel), "BAUD", "SPACE", and "MARK" indicators are used to show the BIT status and results.

Immediately upon activation of BIT, the MARK display will show "8000A" and the SPACE display will show "-bit-". These characters remain on the MARK and SPACE displays throughout the duration of BIT.

The "CH" (Channel) display indicates the number of the BIT sequence in process. There are a total of thirteen (13) BIT sequences, indicated by "0" through "9" and "A", "B", and "C".

The "BAUD" display shows "FAIL" and flashes if any step fails and "PASS" after all 13 BIT steps pass. The "BAUD" display is normally blank during the operation of BIT if no failures occur.

If BIT has been activated by Remote Control command, descriptive text for each step is printed on the remote control terminal, followed by "PASSED" or "FAILED" as each test step is completed.

3.1 BIT Step Successful:

As each BIT step is run, the number of that step is shown on the "CH" display. Successful completion of that BIT step is indicated by progressing of the "CH" display to the next step number (or letter). The BAUD display remains blank during each successful step, but shows "PASS" when all 13 steps have been successfully completed.

If BIT has been activated via the Remote Control port, the characters "PASSED" are printed following the description of the test conducted. Successful completion of all 13 steps of the BIT are indicated by printing "ST-8000A PASSED ALL TESTS" on the Remote Control terminal. Except for BIT "Test B" (see 4.12), messages are output to the Remote Control terminal only when BIT has been activated via Remote Control.

3.2 BIT Step Failure:

If any test should fail, the following sequence is observed:

1. The word "FAIL" appears on the BAUD display.

2. The failed BIT step number appears on the CH display.

3. The ST-8000A halts at this BIT step and will not proceed further.

Procedure after BIT step failure differs slightly between front panel activation and Remote Control activation of BIT.

If BIT has been activated via the front panel keypad and a step fails:

4a. Upon failure of a step, the ST-8000A remains locked in that BIT step and pressing the front panel "BIT" or "CLEAR" keypads will not restart BIT or reset to normal operation. However, cycling the AC Power switch OFF and back ON will restore the ST-8000A to normal operation at the parameters set before activation of BIT.

If BIT has been activated via Remote Control command T1 and a step fails:

4b. Upon failure of a step, the ST-8000A remains locked in the BIT step but will respond to a T0 command, restoring the ST-8000A to normal operations at the parameters set before activation of BIT. This feature is included to allow operator access to the Remote Control command menus (T9). As in the case of front panel BIT access, cycling of the AC power switch OFF and back ON will also restore normal ST-8000A operation.

5. The phrase "FAILED" is continuously sent to the remote control terminal. "FAILED" is repeated until ST-8000A AC Power is turned OFF or until the remote control command T0 is entered.

Note that, although a BIT step failure may be by-passed, a failure has nonetheless occurred. Continued operation of a failed ST-8000A is not recommended. However, should a failure occur, BIT activation should be repeated to confirm the failure mode.

4.0 ST-8000A BIT STEPS:

A total of 13 BIT steps are conducted, "0" through "9" and "A" though "C". The following is a description of each of these steps.

4.1 Microprocessor Alive Test (Test 0):

When BIT is invoked, the letters "8000A" appear in the MARK numerical display, "-bit-" appears in the SPACE numerical display, the BAUD display is cleared and CHANNEL is set to "0". Also, the MARK and SPACE level indicators and all LED's are cleared.

If BIT is activated via remote control, the following message is sent to the remote control terminal:

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HAL  ST-8000A HF MODEM
BUILT-IN-TEST (BIT) SUMMARY
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When this step passes, BIT automatically proceeds to "Test 1". "Test 0" requires approximately 0.5 seconds to complete.

4.2 Internal Clock Test (Test 1):

BIT "Test 1" tests the Programmable Interval Timer (8254) and its generated clocks. This step verifies the internal timing clock, the Low-pass filter clock and the Transmit Sync clock. Operation of other clocks are confirmed during "loop-back" steps ("Test 6" through "Test A").

If BIT is activated via remote control, the following message is sent to the remote control terminal:

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1.. Timer Frequency Test ....  PASSED   (or repeated FAILED)
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When this step passes, BIT automatically proceeds to "Test 2". "Test 1" requires approximately 0.5 seconds to complete.

4.3 ROM Checksum Test (Test 2):

BIT "Test 2" checks the firmware ROM (A2U4) for errors by calculating a sum-check of the entire ROM contents. "Test 2" fails if the sum-check value does not agree with the factory calculated

correct value.

If BIT is activated via remote control, the following message is sent to the remote control terminal:

2.. EPROM Memory Test ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test 3". "Test 2" requires approximately 0.5 seconds to complete.

4.4 Random Access Memory (RAM) Test (Test 3):

BIT "Test 3" checks the Random Access Memory (RAM, A2U3). Test patterns are written to the RAM and verified. "Test 3" fails if any single read value does not match the value written. Front panel displays will flicker when the RAM configuration is restored.

If BIT is activated via remote control, the following message is sent to the remote control terminal:

3.. RAM Memory Test ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test 4". "Test 3" requires approximately 1.0 seconds to complete.

4.5 EEPROM Test (Test 4):

BIT "Test 4" verifies EEPROM (A2U2) operations. EEPROM sections used by the main program are tested. Previous EEPROM data is saved in RAM and replaced after the test is completed. "Test 4" fails if the read operation does not match the write operation.

If BIT is activated via remote control, the following message is sent to the remote control terminal:

4.. EEPROM Memory Test ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test 5". "Test 4" requires approximately 1.5 seconds to complete.

4.6 Front Panel Indicator Test (Test 5):

BIT "Test 5" requires operator observation. At the start of "Test 5", all segments and LED's are

turned ON for 2.5 seconds. The operator must visually verify that this does occur. All LED indicators and display segments are then turned OFF for 2.0 seconds. The operator must also visually verify that all segments turn OFF.

Pass or failure of "Test 5" must be confirmed by operator observation. Test 5 always concludes with "PASSED" on the front panel display. If the operator should miss this test or be unsure of its result, he should re-invoke BIT by pressing the front panel BIT keypad or by re-entering the T1 Remote Control command. Note, however, that this will also cause repeat of BIT steps "Test 0" through "Test 4".
If BIT is activated via remote control, the following message is sent to the remote control terminal:

5.. Display Test ..... PASSED (no failure indication)

BIT automatically proceeds to "Test 6" upon completion of the ON/OFF display test. "Test 5" requires approximately 4.5 seconds to complete.

4.7 Loopback Data Test, Parameter Set #1 (Test 6):

BIT "Test 6" is a complete test of all low-speed modulator and demodulator signal processing circuits. To do these tests, the modulator output is internally connected to the demodulator input ("loopback") and a known data stream is sent through the modem. The demodulated data stream is bit-by-bit compared with the test data sent. "Test 6" fails if any single bit comparison fails. The parameters used for this test are:

MARK = 300 Hz
SPACE = 3000 Hz
BAUD = 100
MODULATOR LEVEL = 0 dBm
TEST DATA = 511 pseudo-random data elements

If BIT is activated via remote control, the following message is sent to the remote control terminal:

6.. Loopback Test #1 ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test 7". "Test 6" requires approximately 6.0 seconds to complete.

4.8 Loopback Data Test, Parameter Set #2 (Test 7):

BIT "Test 7" is the second loopback test of the low-speed demodulator. "Test 7" fails if any single bit comparison fails. The test parameters are:

MARK = 2000 Hz
SPACE = 2085 Hz
BAUD = 75
MODULATOR LEVEL = -20 dBm
TEST DATA = 511 pseudo-random data elements

If BIT is activated via remote control, the following message is sent to the remote control terminal:

7.. Loopback Test #2 ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test 8". "Test 7" requires approximately 7.0 seconds to complete.

4.9 Loopback Data Test, Parameter Set #3 (Test 8):

BIT "Test 8" is the third loopback test of the low-speed demodulator. "Test 8" fails if any single bit comparison fails. The test parameters are:

MARK = 1000 Hz
SPACE = 2000 Hz
BAUD = 300
MODULATOR LEVEL = -45 dBm
TEST DATA = 511 pseudo-random data elements

If BIT is activated via remote control, the following message is sent to the remote control terminal:

8.. Loopback Test #3 ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test 9". "Test 8" requires approximately 2.5 seconds to complete.

4.10 Loopback Data Test, Parameter Set #4 (Test 9):

BIT "Test 9" is the first loopback test of the high-speed demodulator circuit. "Test 9" fails if any single bit comparison fails. The test parameters are:

MARK = 1575 Hz

SPACE = 2425 Hz
BAUD = 650
MODULATOR LEVEL = -20 dBm
TEST DATA = 511 pseudo-random data elements

If BIT is activated via remote control, the following message is sent to the remote control terminal:

9.. Loopback Test #4 ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test A". "Test 9" requires approximately 2.0 seconds to complete.

4.11 Loopback Data Test, Parameter Set #5 (Test A):

BIT "Test A" is the final loopback test of the high-speed demodulator. "Test A" fails if any single bit comparison fails. The test parameters are:

MARK = 1400 Hz
SPACE = 2600 Hz
BAUD = 1200
MODULATOR LEVEL = 0 dBm
TEST DATA = 511 pseudo-random data elements

If BIT is activated via remote control, the following message is sent to the remote control terminal:

A.. Loopback Test #5 ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to "Test B". "Test A" requires approximately 1.5 seconds to complete.

4.12 Remote Port Test (Test B):

BIT "Test B" is a test of the Remote Control port of the ST-8000A. This test requires that the operator observe the output of a message sent by the ST-8000A to the remote control terminal. This message is always sent to the Remote Control port, even if BIT is accessed via the front panel keypad. This test requires observation to determine "PASS" or "FAIL". The text sent to the remote control terminal is:

B.. Remote Port Test .....
THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG'S BACK 0123456789
[0.5 second delay]
THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG'S BACK 0123456789
B.. Remote Port Test ..... PASSED

There is no failure message sent to the remote control terminal for Test B.

BIT "Test B" always proceeds to BIT "Test C". The time required to complete "Test B" varies with the data rate chosen for communications with the remote control terminal (via option switch U2SW3). At 300 baud, "Test B" requires approximately 6.0 seconds. At 9600 or 19,200 baud, "Test B" requires approximately 2.5 seconds.

4.13 Deadman Timer Test (Test C):

BIT "Test C" tests the automatic reset circuitry. The length of time required for the microprocessor system to reset is verified to be within acceptable limits. Note that BIT "Test C" causes a reset and will flicker the display. If "Test C" passes, the ST-8000A returns to BIT test mode without the loss of any modem parameters. "Test C" fails if the time-out period is outside of acceptable limits.

If BIT is activated via remote control, the following message is sent to the remote control terminal:

C.. Deadman Timer Test ..... PASSED (or repeated FAILED)

When this step passes, BIT automatically proceeds to display of the "Final BIT Report". "Test C" requires approximately 2.5 seconds to complete.

4.14 Final BIT Report:

This concludes the ST-8000A Built-In-Tests. If all tests have been successful, the word "PASS" appears on the BAUD display. If BIT was accessed via remote control, the phrase "ST-8000A PASSED ALL TESTS" is sent to the remote control terminal.

As noted in section 3.2, a failure of any BIT step will result in the display of the word "FAIL" on the BAUD display. If BIT was accessed via the remote control port, the word "FAILED" is also sent continuously to the remote control terminal.

The final report display of "PASS" on the BAUD display remains for approximately 4.0 seconds. After this delay, BIT proceeds to restore operational parameters.

4.15 Restore Parameters:

At the successful conclusion of all BIT steps, all parameters of the ST-8000A are restored to the same values that were in use prior to entering BIT. All input and output connections are restored and the ST-8000A modem is then "on-line" for normal data modulation and demodulation.

As noted previously, an in-process BIT sequence may be aborted at any time by pressing the CLEAR keypad or entering the DISABLE (T0) command from the remote port. The CLEAR or DISABLE commands immediately restore the ST-8000A to full operation using the previously set parameters.

5.0 BIT EXECUTION TIMES

Wherever necessary, the BIT procedure has included pauses to allow for comfortable viewing of the progression of the individual tests. The following is a list of times for each BIT step. Note that BIT requires a longer time to run when the remote terminal data rate is slow. Table 1 shows approximate BIT step times for front panel BIT activation, and remote control activation at 300 and 9600 baud.

TABLE 1
BIT STEP EXECUTION TIMES

		----- BIT ACCESS METHOD -----		
		FRONT	- REMOTE CONTROL --	
TEST	DESCRIPTION	PANEL	300 BD	9600 BD
"Test 0"	Microprocessor Alive:	0.5 sec.	4.0 sec.	0.5 sec.
"Test 1"	Internal Clock Test:	0.5 sec.	3.0 sec.	0.5 sec.
"Test 2"	ROM Checksum Test:	0.5 sec.	3.0 sec.	0.5 sec.
"Test 3"	RAM Test:	1.0 sec.	3.0 sec.	1.0 sec.
"Test 4"	EEPROM Test:	1.5 sec.	3.0 sec.	1.5 sec.
"Test 5"	Indicator Test:	4.5 sec.	6.0 sec.	4.5 sec.
"Test 6"	Loopback Test #1:	6.0 sec.	7.5 sec.	6.0 sec.
"Test 7"	Loopback Test #2:	7.0 sec.	9.5 sec.	7.0 sec.
"Test 8"	Loopback Test #3:	2.5 sec.	3.5 sec.	2.5 sec.
"Test 9"	Loopback Test #4:	2.0 sec.	3.0 sec.	2.0 sec.
"Test A"	Loopback Test #5:	1.5 sec.	2.5 sec.	1.5 sec.
"Test B"	Remote Port Test:	2.5 sec.	6.0 sec.	2.5 sec.
			to 6.0 sec.*	

"Test C" Deadman Timer Test:	3.0 sec.	4.0 sec.	3.0 sec.
BIT Final Report:	4.0 sec.	5.5 sec.	4.0 sec.
Total BIT Time:	38.0 sec.	63.5 sec.	38.0 sec.
	to 41.5 sec.*		

* Time varies with data rate set on remote control port.